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STUDY AND OPTIMIZATION OF FIELD EFFECT TRANSISTORS BASED ON GRAPHENE

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Περίληψη

Στην παρούσα εργασία σκοπός μας είναι η μελέτη και βελτιστοποίηση τρανζίστορ επίδρασης πεδίου από γραφένιο. Αρχικά, μελετήσαμε, επαφές παλλαδίου (Pd) σε γραφένιο και την επίδραση που είχαν στις επιδόσεις των τρανζίστορ, τον καθαρισμό της διεπιφάνειας παλλαδίου-γραφενίου με πλάσμα οξυγόνου για χρόνους έκθεσης 0, 5, 10, 15 και 20 δευτερολέπτων, πριν την εναπόθεση του μετάλλου, καθώς επίσης και την θερμική ανόπτηση υπό συνθήκες αέρα, κενού και ατμόσφαιρας υδρογόνου/αζώτου (H_2/N_2) μετά την ολοκλήρωση της κατασκευής των δειγμάτων. Τα μεγέθη που εξάγαμε από τον ηλεκτρικό χαρακτηρισμό ήταν η αντίσταση επαφής και η επιφανειακή αντίσταση του γραφενίου. Ακολούθως, μέρος της εργασίας ήταν η μελέτη του οξειδίου του Αφνίου (HfO_2) ως διηλεκτρικό πύλης. Ο ηλεκτρικός του χαρακτηρισμός έγινε κατασκευάζοντας δομές μετάλλου-οξειδίου-μετάλλου και εξετάστηκε η αξιοπιστία του ως προς την τάση κατάρρευσης, το ρεύμα διαρροής αλλά και της μεθόδου εναπόθεσης του διηλεκτρικού. Δύο μέθοδοι εναπόθεσης χρησιμοποιήθηκαν, η θερμική εξάχνωση με χρήση τηλεβόλου ηλεκτρονίων και η ατομική εναπόθεση στρώματος. Τέλος, η εργασίας ολοκληρώθηκε με τη μελέτη των τρανζίστορ επίδρασης πεδίου από γραφένιο ως ολοκληρωμένη πλέον ηλεκτρονική διάταξη. Διαγράμματα Dirac, χαρακτηριστικές εξόδου, ηλεκτρική αντίσταση μεταξύ πηγής-απαγωγού και η διαγωγιμότητα, όπως αυτά πρόεκυψαν από τον ηλεκτρικό χαρακτηρισμό, εξεταστήκαν με βάση το πλάτος της πύλης των τρανζίστορ, το μήκος πηγής-απαγωγού και καναλιού.

Abstract

The purpose of this thesis is the study and optimization of field effect transistors based on graphene. Initially, we studied, palladium (Pd)- graphene contacts and their impact on the transistors performance, the O_2 plasma cleaning of the Pd-graphene interface prior to metal deposition for exposure times of 0, 5, 10, 15, 20seconds, and the thermal annealing under air, vacuum and forming gas (H_2/N_2) conditions after the sample fabrication. The quantities that we extracted through the electrical characterization were the contact and graphene sheet resistance. Following, the second part of this thesis was the study of the hafnium oxide (HfO_2) as a gate dielectric. Its characterization was accomplished by fabricating metal-oxide-metal (MOM) structures and its reliability was tested according to the breakdown voltage, leakage current, and the dielectric deposition method. The e-gun evaporation and atomic layer deposition were utilized to deposit the dielectric films. Finally, the thesis was concluded with the study of the graphene field effect transistors as completed device. Dirac diagrams, the output characteristics, the electrical source-drain resistance and transconductance, as were extracted through the electrical characterization, were studied as a function of the gate width, the source-drain distance and gate length.

1. Graphene

1.1 Introduction

Graphene is the name given to the arrangement of carbon atoms on hexagonal honeycomb lattice that is exactly one atom thick [1]. In 2004 Andre Geim and Konstantin Novoselov, succeeded in obtaining graphene in the form of small flakes of the order of several microns through mechanical exfoliation of graphite using a common scotch tape [2],[3]. Because of its unusual and unique physical properties such as, high intrinsic carrier mobility, high thermal conductivity, transparency, strong field effect and flexibility, graphene is considered as a promising material and a possible alternative to silicon- based semiconductor devices [2].

1.2 Graphene Structure

Graphene is a two dimensional sheet of carbon atoms densely packed together into a hexagonal - honeycomb crystal structure, with two atoms in each unit cell bonded together with a carbon bond. The length of this σ-bond is 1.42Å [4],[5]. Each atom holds to its three nearest neighbors in a triangular planar structure of graphene, through strong covalent bonds arising from a sp^2 hybridization of the 2s and 2p orbitals. These σ-bonds are responsible for the mechanical properties of graphene. The p-orbitals of adjacent carbon atoms are normal to the planar structure, and can bind to form a half-filled π band where the electrons can move freely. This gives rise to graphene's unique electronic properties [4],[5].

The band structure gives information about the relationship between the energy and the momentum of the charge carriers. The band structure derivation within the Tight Binding Approximation was fist done by Wallance [6]. Considering interactions only between first nearest neighbors, the eigenvalues of energy may be expressed as

$$E(k) = \pm Vpp\pi\sqrt{3 + 2\cos(k \cdot a_1) + 2cos(k \cdot a_2) + 2cos\big(k(a_1 - a_2)\big)} \qquad (1.1),$$

where $\alpha_1 = \left(\sqrt{\frac{3}{2}}\alpha, \frac{\alpha}{2}\right)$, $\alpha_2 = \left(\sqrt{\frac{3}{2}}\alpha, \frac{\alpha}{2}\right)$ are the graphene lattice vectors and $Vpp\pi$ is the overlapping integral between pz-orbitals. The points where the conductance and valence bands intersect are called Dirac points. Close to these points, in the range of low energies, the relation between energy and momentum becomes linear. As one can see by expanding Eq.(1.1) around k=K+q, for $|q| \ll |K|$ obtaining [6]:

$E(q) = \pm\hbar v_F\,|q|$ (1.2),

where $v_F = \frac{3}{2}\frac{Vpp\pi a}{\hbar} \approx 1 \times 10^8$ cm/s is the Fermi velocity at which electrons or holes move.

The linear dispersion in contrast to the conventional parabolic dispersion, means that the charge carriers are massless, often called Dirac fermions, with a velocity that is independent of the energy.

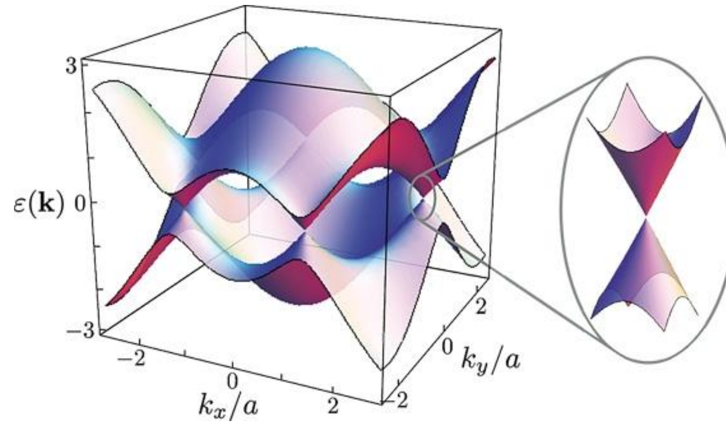

Fig.(1): *Graphene electronic band-structure and linear dispersion at low energies, adapted from* [4].

1.3 Density of States

The density of states gives the number of the allowed electron or holes states per unit volume at a given energy. It can be derived from basic quantum mechanics. In the case of a conventional 2D semiconductor with parabolic bands, the density of states per unit energy and per unit volume can be easily computed as follows:

Let us consider that electrons are restricted in a two dimensional plane of L×L in the two directions x,y and in the third z-direction the plane has zero thick. The solution of Schrödinger equation for free particles is plane waves in two dimensions

$$\psi_{\overrightarrow{k||}}\ (\vec{r}) = \sqrt{\frac{1}{S}}\, e^{i\overrightarrow{k||}\vec{r}} \qquad (1.3),$$

where $\overrightarrow{k||} = (k_x, k_y)$ and S= L^2 is the area, with corresponding energy of

$$E_{\overrightarrow{k||}} = \frac{\hbar^2 k_x^2}{2m} + \frac{\hbar^2\, k_y^2}{2m} = \frac{\hbar^2\, k_{||}^2}{2m} \qquad (1.4).$$

Applying the periodic conditions

ψ(x+L,y)=ψ(x,y) and ψ(x,y+L)=ψ(x,y)

the two components of $\vec{k} = (k_x, k_y)$ get discrete values

$$k_x = \frac{n_x\,(2\pi)}{L},\quad k_y = \frac{n_y\,(2\pi)}{L} \qquad (1.5)$$

Thus, every state in $\overrightarrow{k_{||}}$ - space occupies $\overrightarrow{k_{||}}$ - area $\delta S_k = (2\pi/L)^2$, where $S = L^2$ is the area of plane. As the constant energy curves in 2D space are cyclic we will consider the $\overrightarrow{k_{||}}$ - area, which is enclosed from two cyclic constant energy curves with a separation distance between them equal to dk in 2D $\overrightarrow{k_{||}}$ - space, with corresponding energy difference of dE.

So, one can obtain the number of states by dividing the area $2\pi k_{||} dk_{||}$ between the two cycles with the area of one state,

$$dN = 2\,\frac{2\pi k_{||} dk_{||}}{(2\pi/L)^2} = \frac{S}{\pi} k_{||} dk_{||} \quad (1.6)\ .$$

Finally the density of states per unit energy and per unit area can be expressed as,

$$D_{2d}(E) = \frac{dN}{S\,dE} = \frac{S}{\pi} k_{||} dk_{||} \frac{1}{SdE} = \frac{1}{\pi}\frac{k_{||} dk_{||}}{dE} = \frac{m}{\pi\hbar^2} \quad (1.7).$$

The equation (1.7) is valid for the case of parabolic bands. In order to find the right expression for the graphene density of states, we follow the above steps using

the fact of the linear relation between energy and momentum. Here the relation between energy and momentum of electron is given by equation (1.2) and the finally expression for the graphene density of states is

$$DOS_{graphene} = \frac{2E}{\pi\hbar^2 v_F^2} \quad (1.8)$$

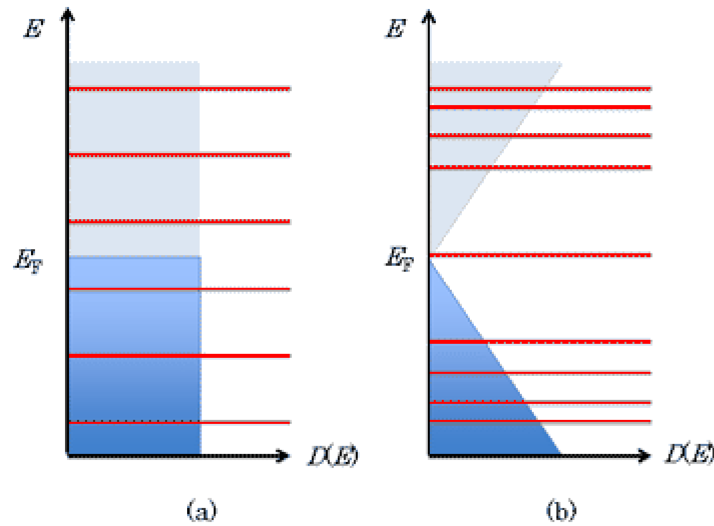

Fig.(2): *(a) the density of states in a conventional 2DEG with parabolic bands, (b) the density of states in graphene with linear dispersion. As we can see in the second case there is a linear relation between density of states and energy that goes all the way to zero, whereas in conventional 2Degs with parabolic bands the density of states is independent and constant over energy. Image adapted from* [7].

1.4 Graphene Synthesis Methods

Today there are several methods for the preparation of graphene. In the following sections, some of these methods will be briefly presented and discussed. They will be compared according to the quality of graphene and the purpose of its use.

1.4.1 Mechanical exfoliation

Since graphite consists of sheets of graphene kept together by weak Van Der Waals energy of the order of 2eV/nm^2 and the force of about 300nN/µm^2[8], graphene can be detached from a graphite crystal using adhesive tape. Continuation of the peeling process can lead to multilayer and even single-layer graphene as it was done for its discovery. Afterwards, graphene from adhesive tape can be transferred to

SiO_2/Si substrate. The oxide thickness plays an essential role in order to distinguish the graphene flakes. An appropriate oxide thickness is 90nm or 300nm as in that range of thicknesses the optical contrast in visible light increases [9],[10]. Graphene obtained by this method has shown properties very close to theoretical predictions e.g. mobility of the order of 10^6 cm^2/Vs. The drawbacks of this method are that the adhesive tape leaves residues on graphene that can result in degradation of mobility, and also this method cannot provide large scale graphene [11].

1.4.2 Graphitization of silicon carbide SiC

In this method graphene can be synthesized by sublimation of silicon at the temperature of about 1300 ℃ in an ultrahigh vacuum environment [12]. The advantages of this method are that the silicon carbide provides an insulating substrate and no further transfer of graphene layer is needed and we can obtain graphene flakes in larger scale than that of mechanical exfoliation method. But, high temperature and high cost of production are considered as obstacles to applying this method.

1.4.3 Chemical vapor deposition

Chemical vapor deposition (CVD) is a well known process in which a substrate is exposed to gaseous compounds. Also, it is compatible with existing semiconductor industry processes [13]. In this technique graphene can be grown by exposing a transition metal film such as Ni, Cu, Co, Pt, Ir or Ru to a gas mixture of H_2, CH_4 (or any other hydrocarbon) and Ar at various temperatures and pressures depending on the type of metal film and gas type. In the case of a Ni film, the metal substrate is exposed at 1000℃, in which the methane decomposes on the surface, so that the hydrogen evaporates. The carbon diffuses into the nickel, and after cooling down in Ar atmosphere, a graphene layer grows on the surface. One of the benefits of CVD method, is that the number of the graphene layers depends on the substrate thickness, that is why CVD method is considered as a controllable synthesis method of graphene. Although, CVD provides graphene in large scale, graphene layers need to be transferred to a substrate, which results in degradation of its carrier mobility due to the polymeric residues [14].

2. Metal-Graphene junction

2.1 Introduction

Since all semiconductor devices have contacts and all contacts have contact resistance, it is important to characterize such contacts. Contacts are generally formed when a metal and a semiconductor are joined together, but they may be formed by semiconductor-semiconductor junction, where both semiconductors can be single crystal; polycrystalline, or amorphous. Two possible types of contacts can result depending on the combination of materials used. The contacts may be ohmic or Schottky barrier contacts. In the case of ohmic contacts, the most common contacts are these of metal-semiconductor contacts [15].

Ohmic contacts have linear or quasi-linear current-voltage characteristics. It is not necessary, however, that ohmic contacts have linear I-V characteristics. The contacts must be able to supply the necessary device current, and the voltage drop across the contact should be small compared to the voltage drop across the active device regions. An ohmic contact should not degrade the device to any significant extent, and it should not inject minority carriers. On the other hand, Schottky barrier contacts have no linear I-V characteristics. Devices based on Schottky barrier contacts are usually referred to as Schottky barrier devices. This name denotes the use of these devices as rectifiers [15].

2.2 Metal-Semiconductor Contacts

Since ohmic contact is generally modeled as a heavily doped Schottky contact, it is useful to begin the theoretical background with the Schottky model of the metal-semiconductor barrier as it is shown in Fig.(3).

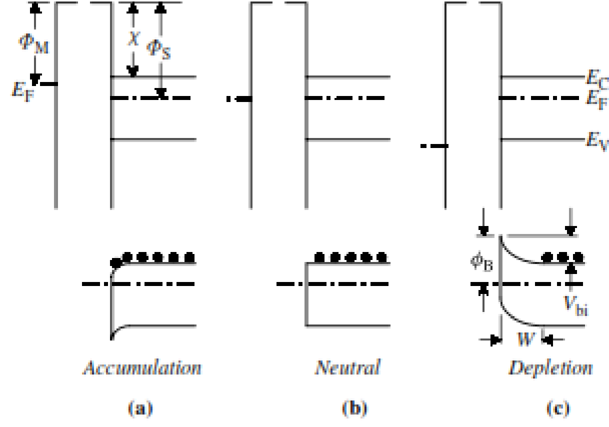

Fig.(3): *Metal-semiconductor contacts according to the simple Schottky model. The upper and lower parts of the figure show the metal-semiconductor system before and after the contact, respectively. The image is adapted from* [15].

We assume intimate contact between the metal and the semiconductor with no interfacial layer. The upper part of the figure represents the energy bands before the contact while the lower part represents the energy bands after the contact. The ideal barrier height after contact for this model is given by

$$\Phi_B = \Phi_M - \chi \quad (2.1)$$

where Φ_M is the work function of the metal,(Φ_S is the work function of the semiconductor respectively, and χ is the electron affinity. The work function of a solid is defined as the energy difference between the vacuum level and the Fermi level while the electron affinity is defined as the potential difference between the bottom of conductance band and the vacuum level at the semiconductor surface. According to the Schottky theory, the barrier height depends only on the metal work function and on the semiconductor electron affinity and is independent of the semiconductor doping density. After contact three types of barrier are possible. We have named them accumulation, neutral, and depletion contacts according to the behavior of the majority carriers [15].

As is evident from Fig.(3) an accumulation – type contact is the preferred ohmic contact because electrons in the metal encounter the least barrier to their flow into or out of the semiconductor. In practice it is difficult to alter the barrier height by using metals of varying work functions. The barrier height with various work

functions metals is many times relatively unaffected due to surface Fermi level pinning, where the Fermi level in the semiconductor surface is pinned at some energy in the band gap to create a depletion type contact [15].

Even though barrier height is independent of the doping density, the barrier width depends on the doping density. Heavily doped semiconductors have narrow space-charge region width W ($W \sim N_D^{-1/2}$). In this case, electrons can tunnel from the metal to the semiconductor and vice versa. Holes tunnel for p-type semiconductor [15].

2.3 Conduction Mechanisms for Metal/Semiconductor Contacts

The conduction mechanisms for a metal n-type semiconductor are illustrated in Fig.(4)

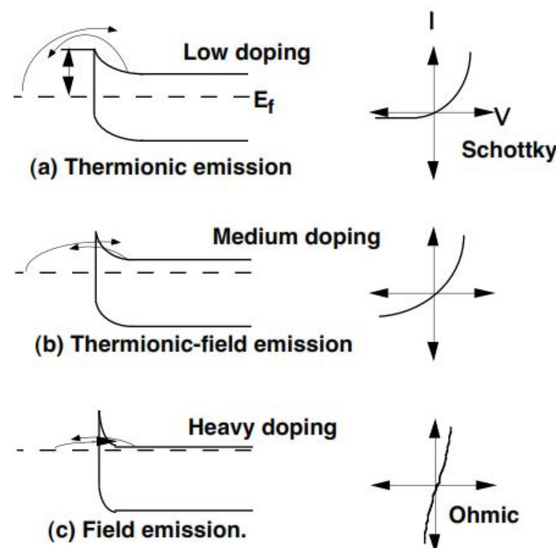

Fig.(4): *Conduction mechanisms for metal/n-semiconductor contacts as a function of the barrier height and width. (a) Thermionic emission; (b) thermionic field-emission; (c) field emission* [16].

For lightly-doped semiconductors the currents flows as a result of thermionic emission (TE) with electrons thermally excited over the barrier. In the intermediate doping range thermionic-field emission (TFE) dominates with carriers thermally excited to an energy where the barrier is sufficiently narrow for tunneling to take place. Finally, for high doping densities the barrier is sufficiently narrow at or near the bottom of the conduction band for the electrons to tunnel directly, known as field

emission (FE).The last mechanism is the preferred transport mode in ohmic contacts [16].

Considering the characteristic energy E_{00} and comparing it to the thermal energy kT , where E_{00} is define by

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{K_s \varepsilon_o m^*_{tun}}} = 1.86 \times 10^{-11}\sqrt{\frac{N(cm^{-3})}{K_s(m^*_{tun}/m)}}[eV] \quad (2.2)$$

where N is the doping density, m^*_{tun} is the tunneling effective mass, and m the free electron mass we can find which of the above conduction mechanisms dominate. Thermionic emission (TE) dominates for kT>>E_{00}, thermionic-field emission dominates for kT≈E_{00}, and field emission occurs for kT<<E_{00} [16].

2.4 Contact resistance

The quantity that evaluates the quality of the metal-semiconductor interface in ohmic contacts is the contact resistance and gives a measure of the ease with which current can flow across this interface. Metal-semiconductor contacts fall into two basic categories. Vertical and horizontal or lateral contacts can behave quite differently, because the effective contact area may differ from the true contact area [15].

Let us consider the resistance between points A and B of the sample having metallic conductors lying on an insulator and making ohmic contacts to an n-type layer in a p-type substrate in Fig.(5)

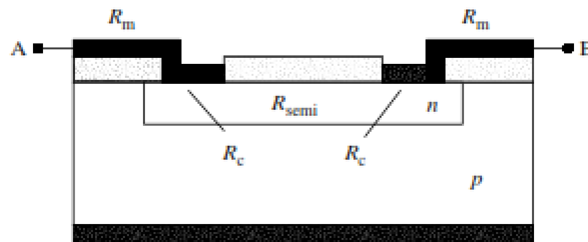

Fig.(5): *A schematic diagram showing two contacts to a diffused semiconductor layer, with the metal resistance, the contact resistances and the semiconductor resistance indicated. The image is adapted from* [15].

The total resistance R_T is defined by the following equation

$$R_T = 2R_c + 2R_m + R_{semi} \qquad (2.3)$$

where R_c represents the contact resistance, R_m represents the metallic conductor resistance and R_{semi} represents the resistance of the semiconductor which is defined by the sheet resistance. Even though the resistance of the semiconductor is well defined we cannot say the same for the contact resistance. Contact resistance certainly includes the resistance of the metal-semiconductor contact, a portion of the metal immediately above the metal-semiconductor interface, a part of the semiconductor below the interface, current crowding effects, and any interfacial oxide or other layer that may be present between the metal and semiconductor [15].

2.5 Definition of contact resistance

The current density J of a metal-semiconductor contact depends on the applied voltage V, the barrier height φ_B and the doping density N in manner that varies for each of the three conduction mechanisms. The contact resistance is characterized by two quantities: the contact resistance R_c (ohms) and the specific contact resistivity ρ_c (ohm cm^2). The specific contact resistivity includes not only the actual interface but the regions above and below the interface [15].

The specific interfacial resistivity ρ_i (includes the resistance of the metal-semiconductor interface) is defined by

$$\rho_i = \frac{\partial V}{\partial J} |V = 0 \qquad (2.4)$$

Since the contact area also plays a role in the behavior of the contact, it must be noted that specific interfacial resistivity is also defined by

$$\rho_i = \frac{\partial V}{\partial J} |A \to 0 \qquad (2.5)$$

where A is the contact area. This specific interfacial resistivity is a theoretical quantity referring to the metal-semiconductor interface only. It is not actually measurable because of the effects referred above. The parameter that is determined from the

measured contact resistance is the specific contact resistivity ρ_c (ohm cm^2). It is a very useful term for ohmic contacts because it is independent of contact area [15].

The current density J of a metal-semiconductor contact, dominated by thermionic emission, is given by

$$J = A^* T^2 e^{-q\varphi B/kT}\left(e^{qV/kT} - 1\right) \quad (2.6)$$

where $A^* = \frac{4\pi q k^2 m^*}{h^3} = 120\left({m^*}/{m}\right) A/cm^2K^2$ is Richardson's constant, m is the free electron mass, m^* the effective mass, and T the absolute temperature. With equations (4),(6) we find the specific interfacial resistivity for

Thermionic emission $\rho_i(TE) = \frac{k}{qA^*T} e^{q\varphi B/kT}$ (2.7)

Thermionic-field emission $\rho_i(TFE) = C_1 \frac{k}{qA^*T} e^{q\varphi B/E_0}$ (2.8)

Field emission $\rho_i(FE) = C_2 \frac{k}{qA^*T} e^{q\varphi B/E_{00}}$ (2.9)

where C_1,C_2 are functions of N,T and φ_B. E_0 in Eq.(2.8) is related to E_{00} by

$$E_0 = E_{00} \coth(E_{00}/kT) \quad (2.10)$$

Substituting for E_{00} in Eq.(9) leads to

$$\rho_i(FE) \sim \exp\left(\frac{C_3}{\sqrt{N}}\right) \quad (2.11)$$

where C_3 is a constant and N the doping density under the contact. Finally, we have to say that specific interface resistivity, primarily depends upon the potential barrier height φ_B, as Eq.(2.11) indicates it is dependent on doping density N [15].

2.6 Measurement Techniques

Contact resistance measurement techniques fall into four main categories: two-contact two-terminal, multiple-contact two-terminal, four-terminal, and six terminal methods. All these methods are capable of determining the specific contact resistivity ρ_c, which is a practical quantity describing the real contact and not only the metal-semiconductor interface [15].

2.6.1 Two-contact Two-terminal Method

The two-contact two-terminal method is the earliest method. For an homogeneous semiconductor of resistivity ρ and thickness t with two contacts as shown in Fig.(6a) , the total resistance R_T=V/I, measured by passing a current I through the sample and measuring the voltage V across the two contacts, is

$$R_T = R_c + R_{sp} + R_{cb} + R_p \quad (2.12.a)$$

For Fig.(6b) with both contacts on the top surface

$$R_T = 2R_c + 2R_{sp} + 2R_p \quad (2.12.b)$$

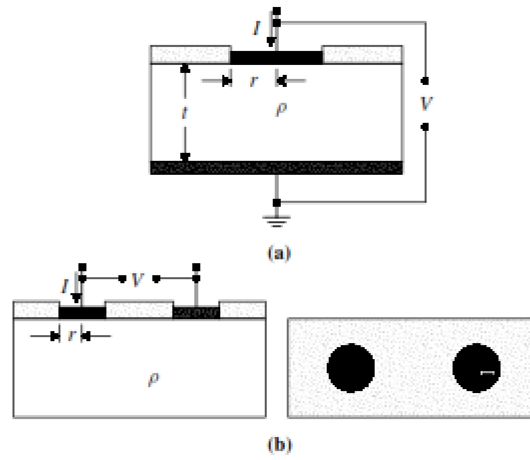

Fig.(6): *(a) A vertical two-terminal contact resistance structure, (b) a lateral two-terminal contact resistance structure. The image is adapted from* [15].

where R_c is the contact resistance of the top contact, R_{sp} the spreading resistance in the semiconductor directly under the contact, R_{cb} the contact resistance of the bottom contact, and R_p the probe or wire resistance. R_{cb} is often neglected because the bottom contact has a large contact area. Similarly, the probe or wire resistance is usually negligible [15].

The spreading resistance of a flat, non indenting circular top contact or radius r on the surface of a semiconductor of resistivity ρ, thickness t, and a large bottom contact can be approximated by

$$R_{sp} = \frac{\rho}{2\pi r} \arctan(2t/r) \quad (2.13)$$

For 2t>>r Eq.(2) can be expressed by

$$R_{sp} = C\frac{\rho}{4r} \quad (2.14)$$

where C is a correction factor that depends on ρ,r and on the current distribution. For widely separated contacts for the structure in Fig.6b, on an uniformly-doped, semi-infinite substrate the correction factor C=1. With the current flowing vertically into the top contact as in Fig.6a , the contact resistance is [15]

$$R_c = \frac{\rho_c}{A} = \frac{\rho_c}{\pi r^2} \quad (2.15)$$

For small R_{cb}, Eq.(2.12) shows the contact resistance to be the difference between the total resistance and the spreading resistance. The spreading resistance cannot be measured independently and small errors in R_{sp} can lead to large errors in R_c. The two-terminal method, therefore works better when $R_{sp} \ll R_c$, approximated by using small radius contacts [15].

The two-terminal method is more commonly implemented with the lateral structure of Fig.7. This test structure differs from Fig.6b by confining the current to the n-island [15].

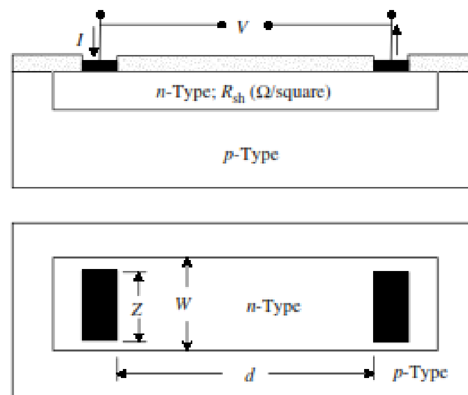

Fig.(7): *A lateral two-terminal contact resistance structure in cross section and top view. The image is adapted from* [15].

The test structure consists of two contacts separated by spacing d. To confine the current flow, the region on which the contact is located must be isolated from the remainder of the substrate, by either confining the implanted or diffused region (n-type on p-type or p-on-n). by planar techniques or by etching the region surrounding the island, leaving it as a mesa. The n-type island in this example has width W and

ideally the contacts should also be W wide. That is difficult to implement and the contact width Z generally differs slightly from W. The analysis becomes more complex due to lateral current flow, current crowding at the contacts, and sample geometry. For the geometry of Fig.7, the total resistance is [15]

$$R_T = R_{sh}\frac{d}{W} + R_d + R_w + 2R_c \quad (2.16)$$

where R_{sh} is the sheet resistance of the semiconductor layer, R_d the resistance due to current crowding under the contacts, R_w a contact width correction if Z<<W, and R_c the contact resistance assuming it is identical for the two contacts. Finally, for a contact string consisting of N islands and 2N contacts, with contacts separated from each other by spacing d and width W and neglecting the metal resistance, the total resistance is given by [15]

$$R_T = N\frac{R_{sh}}{W}d + 2NR_c \quad (2.17)$$

2.6.2 Multiple – Contact Two-Terminal Methods

The multiple-contact, two-terminal contact resistance measurement technique, shown in Fig.8, was developed to overcome the deficiencies of the previous measurement technique [15].

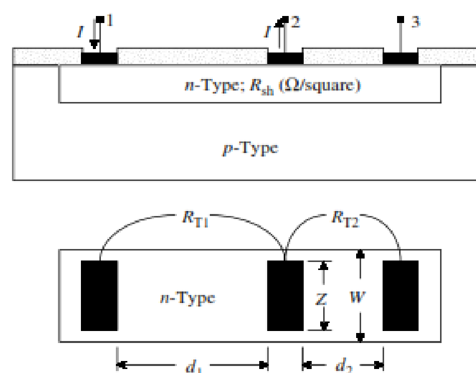

Fig.(8): *Multiple-contact, two-terminal contact resistance test structure. The contact width and length are Z and L and the diffusion width is W. The image is adapted from [16].*

Three identical contacts are made to the semiconductor with contacts spacing d_1 and d_2. Assuming identical contact resistances for each of three contacts allows the total resistance to be written as

$$R_{Ti} = \frac{R_{sh} d_i}{W} + 2R_c \quad (2.18)$$

where i=1 or 2. Solving for Rc gives

$$R_c = \frac{(R_{T2} d_1 - R_{T1} d_2)}{2(d_1 - d_2)} \quad (2.19)$$

The test structure shown in the above figure, Fig.8, seems to overcome the ambiguities of the simpler two-terminal structure, due to the fact that neither the bulk resistance nor the layer sheet resistance need be known, but only the contact resistance and not the specific contact resistivity can be determined. Possible sources of inaccuracy in the determination of contact resistance should be the assumption that all the contacts have identical contact resistances, the fact that the contact resistance is obtained by taking the difference of two large numbers and finally the way that the lengths d_1, d_2 are determined. The last issue occasionally leads to negative contact resistances [15].

2.6.3 Transfer length Method

Since with the above method the specific contact resistivity cannot be determined, this method (TLM) by taking the current crowding into account allows us to extract the specific contact resistivity, considering both the contact and sheet resistance [15].

As the current flowing from the semiconductor to the metal and vice versa, it chooses the path of least resistance, but always encounters the contact and sheet resistance. The potential distribution under the contact is described by the following mathematical formula

$$V(x) = \frac{I\sqrt{R_{sh}\rho_c}}{Z} \frac{\cosh\left[\frac{L-x}{L_T}\right]}{\sinh\left(\frac{L}{L_T}\right)} \quad (2.20)$$

where L is the contact length, Z the contact width, L_T the transfer length, and I the current flowing into the contact [15].

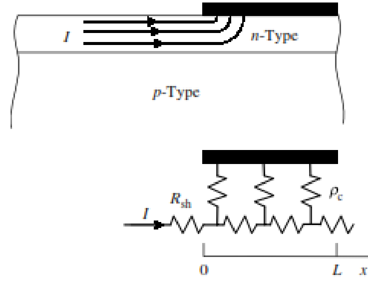

Fig.(9): *Current transfer from semiconductor to metal represented by the arrows. The semiconductor/metal contact is represented by the ρ_c-R_{sh} equivalent circuit with the current choosing the path of least resistance. The image is adapted from* [15].

For x=0, near the contact edge, the voltage has its highest value and diminishes nearly exponentially with the distance x, as the current transfers far from the contact edge. The distance over which most of the current transfers from the semiconductor

$$L_T = \sqrt{\rho_c / R_{sh}} \quad (2.21)$$

to the metal and vice versa, it is called transfer length (L_T). At this distance the voltage drops to the 1/e of its highest value [15].

Let us consider the three contact configurations in Fig.10, with the current flowing from contact 1 to 2. In Fig.10a we have the contact front resistance (≡TLM structure) where both the voltage and current are measured between the same contacts. In fig.10b the contact end resistance test structure is illustrated, where the voltage is measured across the contacts 1 and 2. Finally, in Fig.10c we have the cross bridge Kelvin resistance test structure, in which the voltage is measured at right angles to the current [15].

When V measured between contacts 1 and 2 at x=0, Eq.(2.20) gives the contact front resistance as

$$R_{cf} = \frac{V}{I} = \frac{\rho_c}{L_T Z} \coth\left(\frac{L}{L_T}\right) \quad (2.22)$$

Provided Z=W. Eq.(2.22) is only an approximation when the sample is wider than Z, because this equation does not consider the current flow around the contacts [15].

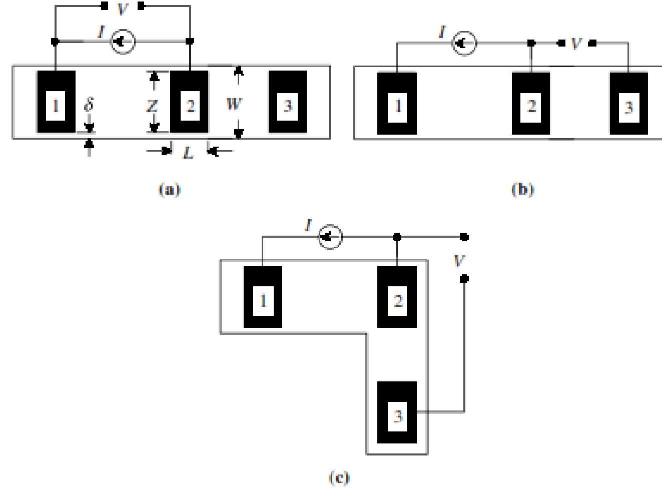

Fig.(10): *(a) Conventional contact resistance test structure, (b) contact end resistance test structure and (c) cross bridge Kelvin resistance test structure. The image is adapted from* [15].

The expression $R_{cf} \equiv R_c$ given by Eq.(2.22), could be simplified according to the following conditions:

For $L \leq 0.5\ L_T$, $\coth(L/L_T) \sim L_T/L$

$$R_c \sim \frac{\rho_c}{LZ} \quad (2.23a)$$

For $L \geq 1.5\ L_T$, $\coth(L/L_T) \sim 1$

$$R_c \sim \frac{\rho_c}{L_T Z} \quad (2.23b)$$

The effective contact area is the actual contact area A_c=LZ for the first case. But in the second case the effective contact area is $A_{c,eff}=L_T Z$. In other words, the effective contact area can be smaller than the actual contact area [15].

In the case of Fig.10b, where the voltage is measured across the contact 2 and 3, at x=L the equation 2.20 leads to the contact end resistance

$$R_{ce} = \frac{V}{I} = \frac{\rho_c}{L_T Z} \frac{1}{\sinh\left(\frac{L}{L_T}\right)} \quad (2.24)$$

The accuracy of the method is limited for short contacts where variations of contact length strongly affect the determination of the R_{ce}. For long contacts, R_{ce} becomes very small and the accuracy is limited by instrumentation, seen by looking at the ratio

$$\frac{R_{ce}}{R_{cf}} = \frac{1}{\cosh{(L/L_T)}} \quad (2.25)$$

which obviously becomes very small for $L \gg L_T$ [15].

For the cross-bridge Kelvin resistance test structure in Fig.10c, the voltage contact 3 is located at the side of contact 2. The measured voltage is thus the linear average of the potential over the contact length L. Integrating Eq.(2.20)

$$V = \frac{1}{L}\int_0^L V(x)dx \quad (2.26)$$

gives the contact resistance as

$$R_c = \frac{V}{I} = \frac{\rho_c}{LZ} \quad (2.27)$$

In equation 2.24 the measured resistance obtained by assuming that the contact width Z to be identical to the sheet width W. in practice this assumption is not valid and $Z<W$. Under the last condition the measured contact end resistance leads to erroneously high ρ_c. The error is attributed to the potential difference between the front and the near edge of the contact allowing the current to flow around the contact edges. For large δ, the measured resistance is proportional to the sheet resistance but independent on the contact resistance. The one-dimensional analysis is valid only if the following condition: $L \ll L_T$, $Z \gg L$ and $\delta \ll Z$ are met. However, accurate extraction of ρ_c, is possible by fitting numerical simulations to measured data [15].

The difficulty of deciding where to measure the voltage in the configuration of Fig.10a.10b.10c has led to a test structure shown in Fig.11a and a measured technique known as the transfer length method originally proposed by Shockley. The TLM test structure consists of more than three contacts. The first and last contacts in the test structure served as entry and exit point for the current in the original ladder structure and the voltage was measured between one of the large contacts and each of the successive narrow contacts in Fig.11a. Later the test structure had unequal spacing between contacts as in Fig.11b, with the voltage measured between adjacent contacts [15].

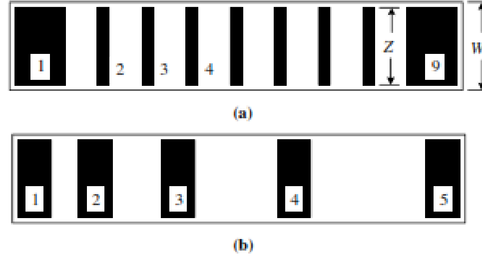

Fig.(11): *Transfer length method test structures. The image is adapted from* [15].

The test structure illustrated in Fig.11b is more advantageous than that of illustrated in Fig.11a., because the effects of the contacts 2 and 3 may be eliminated, when the voltage is measured across the contacts 1 and 4. Concerning the contact length, L, and the transfer length, L_T, we can say that for $L \ll L_T$, the current does not penetrate essentially into the contact metal and thus the contact 2 and 3 have no effects on the measurement. But, in the opposite case where $L \gg L_T$ the current flows into the contact metal and the contact can be thought of as two contacts, each of length L_T joined by the contact metal itself. It is for this reason that the structure in Fig.11b is preferred, because there is only bare semiconductor between any two contacts [15].

For contacts $L \geq 1.5\ L_T$ and for a front contact resistance measurement of the structure in Fig.11b, the total resistance between any two contacts is

$$R_T = \frac{R_{sh} d}{Z} + 2R_c \sim \frac{R_{sh}}{Z}(d + 2L_T) \quad (2.28)$$

The total resistance is measured for various contact spacings and plotted versus d as illustrated in Fig12. Three parameters can be extracted from such a plot. The slope $\Delta(R_T)/\Delta(d)=R_{sh}/Z$ leads to the sheet resistance with the contact width Z independently measured. The intercept at d=0 is $R_T=2R_c$ giving the contact resistance. The intercept at $R_T=0$ gives $-d=2L_T$, which leads to the specific contact resistivity with R_{sh} known from the slope of the plot. The transfer length method gives a complete characterization of the contact by providing the sheet resistance, the contact resistance, and the specific contact resistivity [15].

Even though the transfer length method is commonly used to characterize the quality of contacts, it has its own problems. These problems arise from the assumptions we have made. First, the transfer length obtained from the intercept at R_T=0 is sometimes not very distinct, leading to incorrect ρ_c values. Second, equation 2.28 presupposes that the sheet resistance under the contact and between the metal contacts to be identical. But, in practice the latter is not valid, due to the effects of the contact formation between the contact metal and the semiconductor sheet. In this case we have a modification in the expression for front contact and total resistance [15].

$$R_{cf} = \frac{\rho_c}{L_{Tk} Z} \coth\left(\frac{L}{L_{Tk}}\right) \quad (2.29)$$

and

$$R_T = \frac{R_{sh} d}{Z} + 2R_c = \frac{R_{sh}}{Z}[d + 2\left(\frac{R_{sk}}{R_{sh}}\right) L_{Tk} \quad (2.30)$$

where Rsk is the sheet resistance under the contact and $L_{Tk}=(\rho_c/R_{sk})^{1/2}$. The slope of the R_T versus d plot still gives R_{sh}/Z and the intercept at d=0 gives $2R_c$. However, the intercept at R_T=0 now yields $2L_{Tk}(R_{sk}/R_{sh})$ and it is no longer possible to determine ρ_C since R_{sk} is unknown. Nevertheless, by determining R_{cf} from the transfer length method and R_{ce} from the end resistance method, where

$$\frac{R_{ce}}{R_{cf}} = \frac{1}{\cosh\,(L/L_{Tk})} \quad (2.31)$$

one can determine L_{Tk} and ρ_c. In this way it is possible to find the contact resistance and the specific contact resistivity in addition to the sheet resistance between and under the contacts. Third, the TLM gives reliable results for samples that the electrical and geometrical characteristics are homogeneous and the specific contact resistivity does not scatter across the sample wafer. Fourth, another parameter that it has been reasonably ignored is the resistance of the contact metal itself, but in the case of metal aging the metal resistance increases and can no longer be neglected. Finally, the gap δ is assumed to be zero, otherwise for non uniformed samples these factor must be taken into account and a modification of the contact resistance equation is necessary [15].

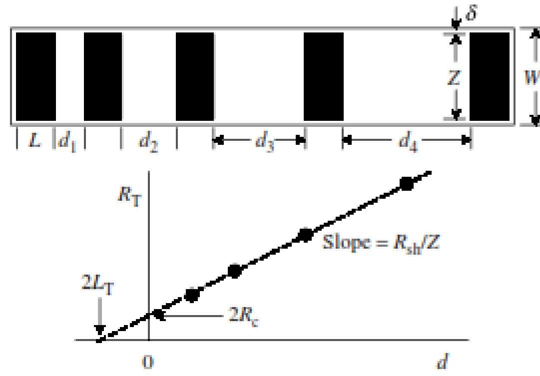

Fig.(12): *A transfer length method test structure and a plot of total resistance as a function of contact spacing d. The image is adapted from* [15].

2.6.4 Four-Terminal Contact Resistance Method

The four-terminal Kelvin test structure also known as the cross-bridge Kelvin resistance is the method that allows the extraction of the contact resistance or the specific contact resistivity without any requirement for the semiconductor bulk resistivity or the semiconductor sheet resistance to be known [15].

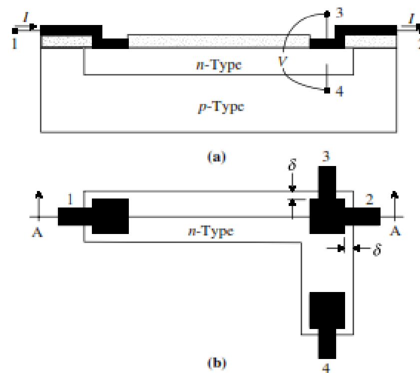

Fig.(13): *A four-terminal or Kelvin contact resistance test structure. (a) Cross section through section A-A, (b) top view of the structure. This image is adapted from* [15].

In the above figure, Fig.13, the principle of this method is illustrated. Contact pads 1 and 2 served as the entry and exit points where the current is forced, while the voltage is measured between the pads 3 and 4. Across the entry and exit points there are three voltage drops. The first occurs between pad 1 and the semiconductor layer, the second along the semiconductor sheet, and the third between the n-layer and the pad 2/3. The measured voltage V_{34}=V_3-V_4 is ascribed to the voltage drop across the

contact metal-semiconductor interface. The existence of a high input resistance voltometer ensures a very low current flow between the pads 3 and 4 and hence the potential at the pad 4 is the same as the potential under the 2/3 pad [15].

The contact resistance is given by

$$R_c = \frac{V_{34}}{I} \quad (2.32)$$

And specific contact resistivity is defined as

$$\rho_c = R_c A_c \quad (2.33)$$

where A_c is the contact area [15].

The specific contact resistivity calculated with equation (2.33) is an apparent specific contact resistivity differing from the true specific contact resistivity by lateral current crowding for contact windows smaller than the diffusion tap, shown as $\delta>0$ in Fig.14. Contact window to diffused layer misalignment and lateral dopant diffusion account for $\delta>0$. In the ideal case, $\delta=0$ as illustrated in Fig.14a. In an actual contact, some of the current, indicated by the arrows in Fig.14b, flows around the metal contact. In the ideal case with $\delta=0$, the voltage drop is $V_{34}=IR_c$. For $\delta>0$, the lateral current flow gives an additional voltage drop that is included in V_{34}, leading to a higher voltage. According to equation (2.33) ρ_c is higher if the actual contact area A_c is used. In any case, for larger δ the obtained resistance is in error. The true resistance is obtained by extrapolating to $\delta=0$ but it is difficult to fabricate test structures with $\delta=0$ [15].

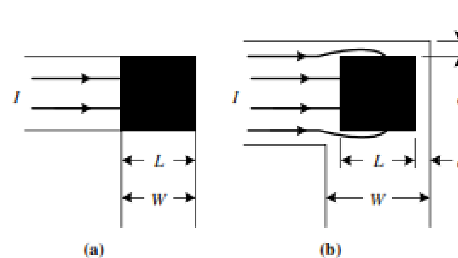

Fig.(14): *Four-terminal contact resistance test structures. (a) Ideal with only lateral current flow, (b) showing current flowing into and around the contact. The black area is the contact area. The image is adapted from* [15].

2.6.5 Six-Terminal Contact Resistance Method

The six-terminal contact resistance structure is very similar to the four-terminal Kelvin structure with two more contacts. By implementing this test structure the contact resistance, the specific contact resistivity, the contact end resistance, the contact front resistance and the sheet resistance under the contact can be determined. The structure of this technique is illustrated in Fig.(15) [15].

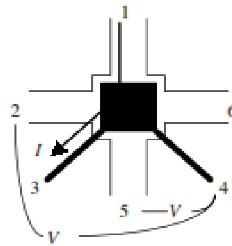

Fig.(15): *Six-terminal Kelvin structure for the determination of R_c,R_{cf},R_{ef} and R_{sk}. The image is adapted from* [15].

By using the conventional Kelvin test structure as illustrated in the Fig.(15) the contact resistance is given by

$$R_c = \frac{V_{24}}{I} \quad (2.34)$$

and the specific contact resistivity is

$$\rho_c = R_c A_c \quad (2.35)$$

Where the voltage is measured across the contacts 2 and 4 and the current is forced between the contacts 1 and3. All the two-dimensional complications, not reflected in Eq.(2.34) and Eq.(2.35), manifest themselves in the six-terminal structure also [15].

To measure the contact end resistance R_{ce}=V_{54}/I, current is forced between contacts 1 and 3 and the voltage is sensed across contacts 5 and 4. The contact resistance and the specific contact resistivity can be determined from the Kelvin part of this structure while the sheet resistance under the contact can be determined from the end resistance using Eq.(2.31) and the contact front resistance [15].

2.7 Comparison of measurement techniques

Two-terminal methods:

The two-contact two-terminal method is the least detailed technique. Contact resistance is corrupted by either the semiconductor bulk or sheet resistance [15].

Two-terminal contact string is a technique which does not give detailed R_c information nor can the specific contact resistivity be reliably extracted [15].

Multiple-contact, two-terminal is usually employed in its transfer length method implementation, where the effect of the semiconductor sheet resistance is separated from the contact resistance and both contact resistance and specific contact resistivity can be determined. Problems appear when the sheet resistance under the contacts differs from the sheet resistance in the channel region and when current flows laterally around the contacts [15].

Four- terminal:

The four-terminal or Kelvin structure is preferred over the two- and three-terminal because contact resistance is measured directly, without metal or semiconductor sheet resistance entering into the R_c determination. Nevertheless, lateral current flow obscures the interpretation [15].

Six terminal method:

The six-terminal method is very similar to the four-terminal technique. It incorporates the Kelvin structure, but additionally allows measurements of the front and end contact resistance as well as the contact sheet resistance [15].

2.8 Carrier transport from metal into graphene

A high quality junction between metal and graphene is crucial in the creation of high performance graphene transistors. In the case of metal-graphene junctions, in contrast to conventional metal-semiconductor junctions, carriers transfer from a three dimensional metal to a two dimensional graphene sheet, which have very different density of states [17]. So it is obvious, in order to achieve the highest device performance an appropriate metal for contact electrodes must be chosen. The injection of charge carriers into graphene from the contact electrodes is necessary to establish a current in the device.

As the charge carriers transfer from the metal contact into graphene, they confront two types of barriers. The first type is referred to the electrostatic barrier that is formed as a dipole layer at the metal-graphene interface. The second type is referred to the electrostatic barrier that is formed at the region between the graphene under the electrode and the graphene in the channel region, due to charge transfer doping inhomogeneity and an effective p-n junction that may be formed there [17]. In the first case the transmission is related with a transmission coefficient T_{MG} and in the second with T_k respectively Fig.(16).

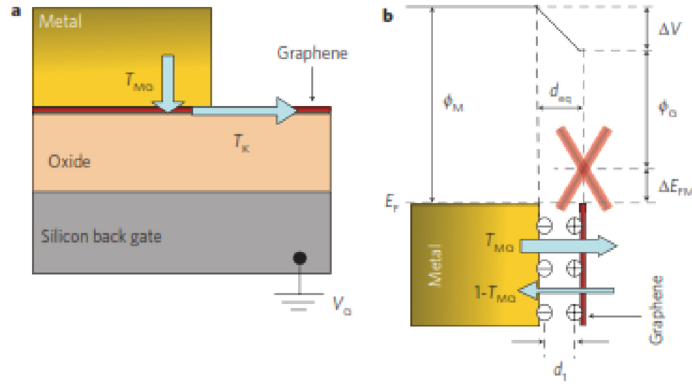

Fig.(16): *Carrier transport processes at the palladium-graphene junction. (a) Schematic view of two cascaded carrier transport processes at the metal-graphene junction, with transmission efficiencies T_{MG} and T_K, respectively. (b) Schematic view of the band profile and dipole formation at the metal-graphene interface, φ_M is the palladium work function, φ_G is the work function of monolayer graphene. ΔE_{FM} is the difference between the Dirac-point and Fermi-level energies in the metal-doped graphene (graphene channel), ΔV is the total built in potential difference, d_{eq} is the equilibrium distance, and d_1 is the effective distance between the charge sheets in the graphene and metal. The red cross represents the Dirac cone, and thick red lines are used to denote the broadening of electronic states* [18].

Carriers in the graphene under the metal can move ballistically or diffusively. In the ballistic regime, the only scattering process is that induced by coupling to the metal, which can be described by an effective coupling length $\lambda_m = \hbar v_F/\pi n$. On the other hand in the diffusive regime, we introduce a scattering mean free path λ with the contacted graphene segment. Here, this mean free path is defined as $\lambda = \pi v_F \tau/2$, where τ is the scattering time. When $\lambda >> \lambda_m$ the contact acts ideally otherwise in the diffusive regime where $\lambda << \lambda_m$ we would expect a much reduced transmission probability. The transmission probability is defined as $T_{MG} = \sqrt{\lambda/\lambda_m + \lambda}$ [17]. The transmission through the p-n junction with a coefficient of T_K is based on Klein tunneling. The efficiency of the tunneling depends on whether the barrier potential is sharp or smooth, and the angle of incidence of the particle to the potential barrier.

Perfect transmission exists when we have normal incidence $\theta=0$ and $T(\theta)=1$, otherwise the transmission coefficient has a $\cos^2(\theta)$ angular dependence and $T(\theta)< 1$ [18].

2.9 The origins of metal-graphene contact resistance

As we have mentioned above, the contact resistance between graphene and metal electrodes is of crucial importance for achieving high performance of graphene devices [19]. Taking into account that high values of contact resistance are observed because of dipole formation at the interface due to charge transfer, perturbation of the graphene beneath the metal and contamination of the metal-graphene interface, many efforts have been done in order to overcome these obstacles.

2.10 Optimization of metal-graphene junctions

2.10.1 Metal choice

In 2011 Fengnian Xia et al, they concluded that to approach an ideal contact with the maximum transmission coefficient, one may choose a higher quality graphene which means choosing graphene with higher mobility can lead to a larger mean free path and therefore better carrier injection efficiency from metal to graphene, even at room temperature. Also, other metal deposition methods can be used to improve the morphology of the metal, which may lead to a smaller metal-graphene coupling length. In their study, they found that the contact resistance in palladium-graphene junction was 110±20 Ω μm, nevertheless other metals can be chosen, which can lead to a higher metal-induced doping concentration in the graphene under the metal [17].

Beginning with the effort of the most appropriate choice of metal, in 2012 Eiichiro Watanabe et al, [20], measured the contact resistance between various metals such as Ti, Ag, Co, Cr, Fe, Ni and Pd in contact with graphene. The metals were deposited through e-beam evaporation onto graphene obtained via micromechanical cleavage of Kish graphite. The R_c value as small as 700±500 Ω μm for Ti contact was obtained.

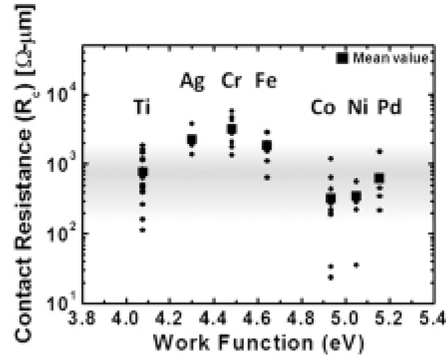

Fig.(17): *Contact resistance as a function of metal work function. Circle marks depict the experimental data of the R_c at Dirac point for various contact metals (Ti, Ag, Co, Cr, Fe, Ni and Pd). Square marks depict mean values of the experimental data* [20].

From their results they concluded that the contact resistance did not strongly depend on the metal work function but was significantly affected by the microstructure of the contact metals.

These results indicated that the fabrication process which provided the uniform metals with the small grains and the uniform interface is essential for obtaining the lower values of contact resistance.

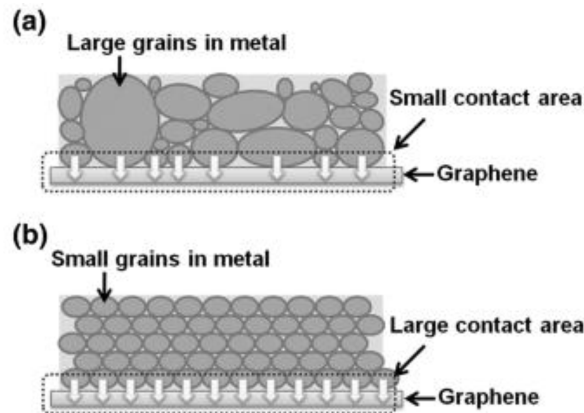

Fig.(18): *Schematic model of metal contact to graphene. (a) and (b) depict a schematic model of the metal/graphene junction for the large and small R_c values respectively. The model shows that R_c becomes smaller with increasing contact area between the metal grain and the graphene* [20].

Remaining in the field of metal choice, in 2009 Ran et al., [21], and in 2013 X. Ji et al., [19], they investigated the physics of the metal-graphene contact based on the interaction that occurs between metals and graphene surface. X.Ji et al. in their report they performed density-functional theory (DFT) and non-equilibrium Green's function (NEGF) methods to study a series of metal/graphene complexes, including

both single-side contacts (Al, Cu, Ag, Au, Pt, Pd, Ti/Gr) and double-side contacts (Pd/Gr/Pd). Their results indicate that the Rc is co-determined by vertical injection rate T_B and lateral transport current I_s. The tunneling barrier between metal and graphene vanishes for chemisorption metal/graphene interface of both single- and double-sided contacts. While the chemisortion metals would have advantages on T_B, the physisorption metals have advantages on electron transport in graphene for preserving its conical electronic structure and high Fermi velocity. Considering both factors together, chemisorption metals would have smaller R_c than physisorption metals, and double-sided contacts would lead to a significant reduction of R_c for double-injecting electrons at high efficiency. For Pd which has the smallest R_c of all sampled metals, R_c for double-side contact was 210 Ω μm and for single-side was 403 Ω μm respectively. Ran et al. in their study they found through first-principles calculation of contacts between graphene and 12 different metals that there exist two types of contacts depending on the strength of interaction between d-orbitals in metals and p_z-orbitals in graphene. The carrier transport through these contacts is calculated using the extended Huckel theory-based non-equilibrium Green's function formalism. According to the Pd/graphene relaxed structure shown in Fig.18, the Pd/graphene distance increased from 2.3Å at the edges to 3.4Å at the center. This suggests that Pd/graphene contact is a combination of chemical and physical types of contacts. Pd atoms at the center are hard to form covalent bond since their fully filled 4d orbital are stable. However, Pd atoms at the edge suffer disorders to make an electron easier to be excited to the 5s orbital, then 4d orbital can interact with graphene's p_z-orbital because the 4d orbital of graphene is barely below the Fermi level [19], [21].

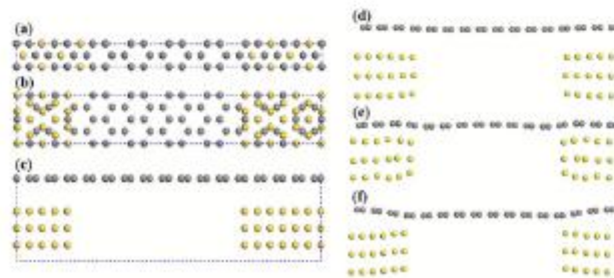

Fig.(19): *(a)-(c) calculated structure. (d)-(f) Contact structure after relaxation.(a) The x-y plane view of graphene contact with Cu, Co, and Ni. (b) The x-y plane view of graphene contact with Al, Ti, Au, Pd and Pt. (c) The x-z plane view of (b), (d), (e), and (f) are for Au/graphene, Ti/graphene, and Pd/graphene structure, respectively* [21].

Except for the metal used for electrodes, the value of contact resistance depends on the synthesis method of graphene. To date the best reported R_c for lithographically defined contacts deposited onto exfoliated graphene flakes ranges from 200 Ω μm to 500 Ω μm. Contact resistance for contacts formed to epitaxial graphene on SiC has been reported to be less than 100 Ω μm and with specific contact resistivity (ρ_c) of order 10^{-7} Ω cm^2. Finally, the minimum values of contact resistance for chemical vapor deposition (CVD) graphene typically range from 500 Ω μm to several thousand Ω μm [22].

2.10.2 Cleaning methods

As was discussed earlier, residue contaminations come from graphene transfer onto a substrate (PMMA) or due to photolithography (photo-resist) and they increase the contact resistance. Many methods have been applied to eliminate these contaminations such as thermal annealing, O_2 plasma cleaning, CO_2 cluster and ultraviolet/ozone treatment. In the following sections we give a description of these methods.

2.10.2.1 Thermal annealing

Thermal annealing is process used for removing any residue contaminations from the surface of a material, for intrinsic stress liberation, structural improvement and surface roughness control [23]. Since in this thesis graphene is studied, we chose to focus on the influence of thermal annealing on graphene. As it is mentioned in Chapter 1, graphene may be fabricated by mechanical exfoliation from bulk graphite, SiC sublimation from bulk silicon carbide, and chemical vapor deposition (CVD) on catalytic metal films. To be promising for commercial or bulk production, graphene must be grown over large areas, for which CVD growth is most promising due to its high yield and quality. However, the large-area CVD graphene must be transferred from the catalyst growth metal to desired substrates such as SiO_2. A common method for graphene transfer involves spin-coating a polymer, typically poly(methyl methacrylate) (PMMA) to support the graphene during etching of the catalyst metal and transfer to substrate. Once the graphene-PMMA stack is transferred, the polymer is removed either through solvent rinses, thermal annealing or a combination of two. The solvent rinses leave a layer of polymeric residue, and that can be partially removed by thermal annealing in gaseous atmospheres such as Ar, H_2, H_2/Ar, N_2,forming gas (H_2/N_2) or in vacuum. Each of these gaseous atmospheres has

different effects on graphene. For instance, it has been shown that ultra-high vacuum annealing can increase CVD graphene carrier mobility to approach what is measured in mechanically exfoliated graphene. Furthermore, the alternate annealing under hydrogen and oxygen atmospheres removes the majority of PMMA residues; however oxygen annealing introduces defects in the graphene lattice while annealing in H_2/Ar atmosphere strongly dopes and strains graphene. In order to achieve the desirable effect of thermal annealing, an ideal combination of gas atmosphere and annealing temperature is required [23], [24].

2.10.2.2 Plasma Cleaning

Plasma cleaning is suitable for removing organic contaminants, which remain after conventional cleaning [25]. It works primarily by bombarding the material surface with ions that dislodge surface impurities. Once liberated from the surface the impurities are drawn away under vacuum in a low pressure plasma system or ejected into the air through a pump [26]. Even though many gases can be used in this method of cleaning such as O_2, H_2, and Ar, it is essential to choose the correct plasma gas as gases react and work in different ways at removing contaminants [25]. For the scope of this thesis O_2 plasma is used prior to metal deposition because oxygen plasma cleaning prepares surface for subsequent processing by removing polymeric contaminants. Residue contaminants on the sample surface will be removed in two ways. First, the energy ions mechanically break up molecular bonds of the surface molecules and effectively blast the molecular particles off the sample surface. Second, atomic oxygen in the plasma readily reacts with the surface contaminants, breaking them up into smaller and more volatile pieces which easily evaporate off the surface. [27]. In 2011 Robinson et al. presented a method for forming high quality ohmic contacts to grahene, which improves the contact resistance by nearly 6000 times compared to untreated metal/graphene interfaces. In their report they evaluated the specific contact resistivity ρ_c using T_i(10nm)/Au(50nm) metal contacts on epitaxial graphene which were fabricated via standard UV lithography. The processing steps and treatments are illustrated in Fig.20. Specific contact resistivity continually decreases as the O_2 plasma treatment time increases from 30 to 90s to 4×10^{-7} Ω cm^2. Upon reaching 120s, ρ_c begins increasing again suggesting the degradation of graphene. Post-processing heat treatments of contacts following a 90 s O_2 plasma

continues to improve ρ_c. Thermal treatments >450 ^oC are explored to remove the contaminations that may remain on the graphene layer following metal lift off. This combination of O_2 plasma treatment and thermal annealing at 450 ^oC -475 ^oC for 15min resulted in optimum specific contact resistivity values of 7.5×10^{-8} Ω cm^2 [28].

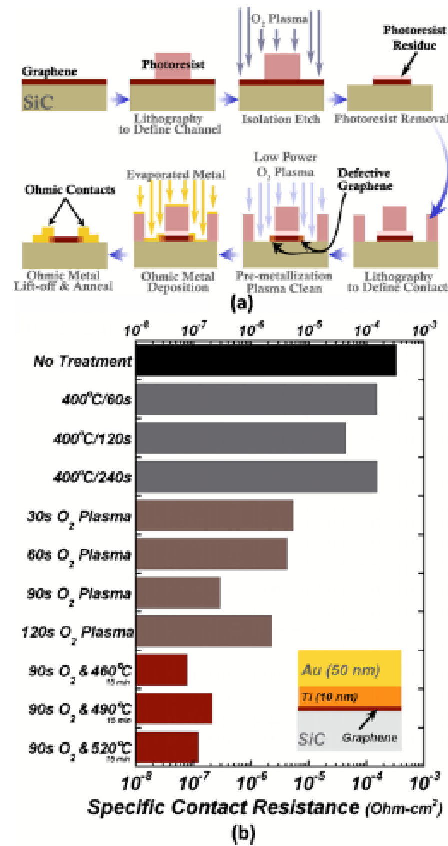

Fig.(20): *(a) Process development (b) the specific contact resistance of a T_i/Au contact is improved to 4×10^{-7} Ω cm^2 when a "gentle" O_2 plasma is employed and to 7.5×10^{-8} Ω cm^2 when the O_2 plasma treatment is combined with a 15 minutes furnace anneal in nitrogen forming gas* [28].

2.10.2.3 Ultraviolet/ozone treatment

UV/ozone treatment is another dry surface treatment technology which uses ultraviolet light and ozone to both clean and modify the surface of solids. Low-pressure UV lamps are used to generate a unique combination of wavelengths that both cleans the surface organic contaminants and improves the bond strength of the surface atomic layer [29]. UV rays cause organic compounds to be converted into volatile substances by decomposition and by strong oxidation during the formation and decomposition of O_3. Organic compounds can be decomposed by irradiating them

with energy stronger than the bond energy. These excited contaminants, or the free radicals of the contaminants react with O_3 to form simple molecules such as CO_2, H_2O, N and O_2 which are removed from the surface [30]. In 2013 Li et al. reported on the influence of ultraviolet/ozone on metal-graphene contact. They found that UV/ozone treatment removes resist residue prior to metallization and leads to a contact resistance between Ti(20nm)/Au(80nm) and CVD graphene of less than 200 Ω µm [22].

2.10.2.4 CO2 cluster cleaning

This cleaning method uses a gas cluster as a physical removal medium of contaminants for cleaning CVD graphene. Since the freezing temperature of CO_2 is relatively high at 194,5 K, CO_2 clusters can be formed very effectively by adiabatic expansion through converging-diverging nozzle in a short time. The gas clusters are introduced to the surface of the contaminants, cooling and removing the contaminants without leaving secondary contaminants behind. This cooling or freezing of polymeric residues causes a difference in the thermal expansion coefficients between the contaminant and the substrate, and rapid volume shrinkage of the residues induces the contaminant to easily detach from the surface. In 2014 Gahng et al. applied this technique to improve the resistance between Cr(5nm)/Au(50nm) contact and CVD graphene. They found that the optimum value of the contact resistance was 1.69 kΩ µm at a flow rate of 201/min [31].

3. Dielectrics

3.1 Introduction

Dielectrics are materials that are widely used in semiconductor devices, due to their high electrical resistance. In integrated circuits dielectric materials are used as insulating layers between conducting layers, diffusion and ion implantation masks, capping material for doped films to prevent loss of dopants, passivation layers to protect devices from impurities, moisture and starches, as interlayer films between the plates of a capacitor, and gate oxides [32].

3.2 Definition of dielectrics

With the term 'dielectrics' we refer to these materials in which electrostatic fields could persist for a relatively long time without any charge flowing through them. [32]. When a dielectric material is placed in an external electric field, electric charges have an extremely different behavior compared to that in conductors. The external applied field causes the charges of dielectric materials to slightly shift from their equilibrium positions, and this shift causes the dielectric polarization. The positive charges follow the direction of the external applied field while the negative charges are displaced to the opposite direction. This orientation of the charged particles results in the generation of an internal electric field, smaller in magnitude compared to the external electric field, which partially counteracts the external electric field. The quantity that gives a measure of the dielectric polarizability is the relative permittivity or dielectric constant and is denoted as k [32], [33].

3.3 Parallel plate Capacitor

The capacitance of a flat capacitor with free space as an insulator between the two electrodes is given by the following equation, Eq.3.1,

$$C = \frac{\varepsilon_o A}{d} \quad (3.1)$$

where C is the capacitance, ε_o is the absolute permittivity, A is the plate area and d is the separation distance between the electrodes/plates. As we observe from the Eq.3.1, the capacitance density, which is equal to the capacitance given by Eq.3.1 divided by A, is directly proportional to the absolute permittivity and inversely proportional to the distance d [33].

Let us consider now the parallel plate capacitor as it is shown in the following figure, Fig.21.

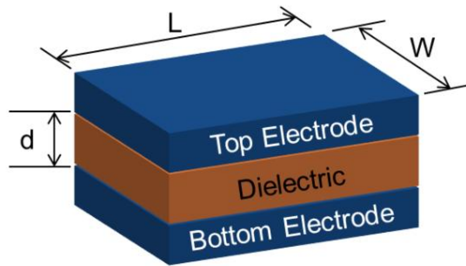

Fig.21: *A basic parallel plate capacitor of length (L) and width (W) with spacing between the electrodes/plates (d). The image is adapted from* [34].

In this case we can see that between the electrodes/plates there is a dielectric material and not air, therefore the capacitance density (the charge storage ability per unit voltage per unit area) increases by a factor k, where k is the dielectric constant of the medium that is placed between the electrodes/plates. So the equation Eq.3.1, is now transformed to equation, Eq.3.2 [33],

$$C = \frac{k\, \varepsilon_o A}{d} \quad (3.2)$$

From the last equation we can see that the higher dielectric constant k the higher the capacitance density is achieved. On the other hand the lower the separating distance between the electrodes/plates which corresponds to the thickness of the dielectric film the higher the capacitance density is achieved. This increase in

capacitance or capacitance density is due to the polarization of the dielectric material in which the negative and positive charges are displaced with respect to their equilibrium positions with the presence of an external electric field. More specifically, in the following figure, Fig.22a we see a parallel plate capacitor with vacuum as the dielectric material between the electrodes/plates. The plates are connected to constant voltage supply V. Let Q_o be the charge on the capacitor plates. For a given V and Q_o the capacitance C_o is given by the following equation, Eq.3.3 [33]

$$C_o = \frac{Q_o}{V} \quad (3.3)$$

The electric field between the plates can be calculated as follows

$$\boldsymbol{E} = -\frac{dV}{dx} = \frac{V}{d} \quad (3.4)$$

with a direction from high to low potential as it shown in Fig.22. When a dielectric film is placed between the plates while keeping the same voltage V, an additional charge is stored on the plates because of an external current flow. Thus, the charge on the plates increases from Q_o to Q as shown in Fig22b,c. This charge increase results in a capacitance increase given by the following equation, Eq.3.5 [33]

$$C = \frac{Q}{V} \quad (3.5)$$

Using the fact that the dielectric constant k has been defined as the reflection of the capacitance increase or the charge storage ability by virtue of having a dielectric material we can define the dielectric constant as follows [47]

$$k = \frac{Q}{Q_o} = \frac{C}{C_o} \quad (3.6)$$

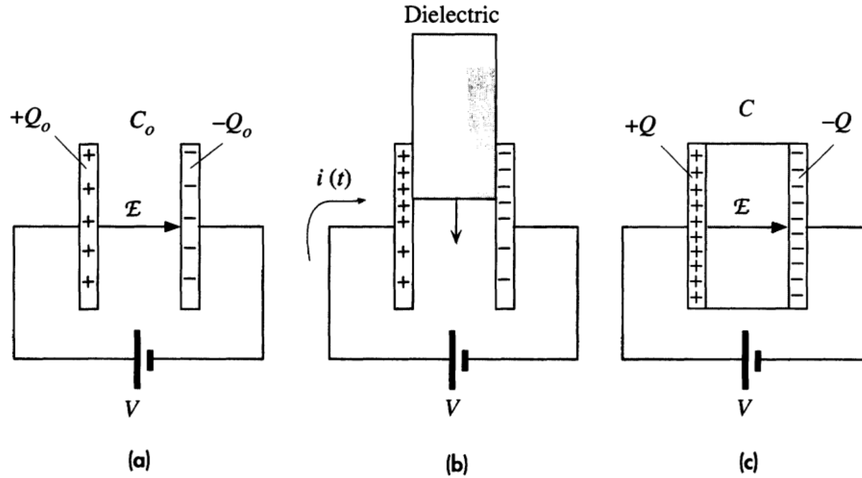

Fig.22: *a) Parallel plate capacitor with free space between plates, b) as a slab of a dielectric material is inserted between the plates, there is an external current flow indicating that more charge is stored on the plates, c) the capacitance has been increased due to the insertion of the dielectric film. The image is adapted from* [33].

As it is mentioned above this charge increase is due to the polarization which is caused by the external applied field. More specifically, when a dielectric material is placed in an external applied field their atoms and molecules are polarized and as a result positive and negative charges there are at the edges of the material while the total charge of the material remaining zero. These bound charges at the dielectric surfaces are called surface polarization charges. The polarization is denoted as **P** and is defined as follows [33]

$$\boldsymbol{P} = \frac{1}{Volume}[\boldsymbol{p}_1 + \boldsymbol{p}_2 + \cdots + \boldsymbol{p}_N] \quad (3.7)$$

Where $\boldsymbol{p}_1, \boldsymbol{p}_2, \dots, \boldsymbol{p}_N$ are the dipole moments induced at N molecules in the volume [47]. To calculate the polarization of the polarized dielectric we regard the dielectric as a system which has a dipole moment p_{total} that is directed from the negative to the positive surface polarization charges. The p_{total} is given by the following formula

$$p_{total} = Q_p d \quad (3.8)$$

where Q_p represent the surface charges that are separated by distance d. Thus, the magnitude of the polarization that defined as the total dipole moment per volume (=Ad) is calculated as [33]

$$P = \frac{Q_p d}{Ad} = \sigma_p \quad (3.9)$$

Where σ_p is the surface polarization charge density. The last equation gives only the magnitude of polarization. The charge per unit area that created on the surface of a polarized material is equal to the component of the polarization vector normal to this surface [47]. At this point it is necessary to define the relation between polarization and electric field using the quantity of the electrical susceptibility χ_e, [33]

$$P = \chi_e \varepsilon_o E \quad (3.10)$$

As we can see the above equation, Eq.3.10, gives the dependence between the polarization and the electric field. So, the next step is to find a relation between the electric field (or polarization) and dielectric constant k. The electric field absence of the dielectric layer between the two electrodes/plates is [33]

$$E = \frac{V}{d} = \frac{Q_o}{C_o d} = \frac{\sigma_o}{\varepsilon_o} \quad (3.11)$$

where σ_o is the surface charge density of the free charges that are stored on the capacitor plates. Presence of the dielectric layer the electric field remains the same and is equal to $V/_d$. But as we discussed above due to the dielectric layer the charge increases from $Q_o \; to \; Q$, and the new charge is equal to $Q = Q_o + Q_p$. Using the definition of the free surface charge density and the definition of the surface polarization charge density, we can rewrite the expression for the new charge as follows [33]

$$\sigma = \varepsilon_o E + \sigma_p \quad (3.12)$$

Now, we are ready to extract the expression for the dielectric constant. In the above equation, Eq.3.12, we constitute $\sigma_p = P$ and $P = \chi_e \varepsilon_o E$ and we obtain that [33]

$$k = \frac{Q}{Q_o} = \frac{\sigma}{\sigma_o} \quad (3.13)$$

The last equation, Eq.3.13, gives the relation between the dielectric constant and the surface charge density on the plates of capacitor, and now is completely

understood how high values of dielectric constant imply capacitance density increase [33].

3.4 Dielectric strength

A major issue that we face with dielectrics is their strength. The dielectric strength is defined as the upper limit of the electric field without causing dielectric breakdown. This critical value of the electric field is denoted as E_{br}. When the value of the applied electric field exceeds this critical value, E_{br}, the current between the electrodes increases dramatically (exponentially) and charge particles flow through the medium since the dielectric has lost its insulating property. The dielectric strength of solid dielectrics besides simply molecular structure depends on several factors such as the impurities in the material, microstructural defects, sample geometry, thickness, aging effects, nature of electrodes, temperature and other environmental conditions as well as the duration and the frequency of the applied field [33].

3.5 Dielectric breakdown in solids

In the following paragraphs we introduce some of the major mechanisms that lead to breakdown in solid dielectrics.

3.5.1 Intrinsic breakdown or Electronic breakdown

In the presence of a strong electric field, an electron that is in the conduction band is accelerated and gains sufficiently large energy that when collides with an electron that is in turn excited and is transmitted from the valence to the conduction band. Thus, in the conduction band there are two free electrons the initial one and the electron that is caused from the broken bond. These two electrons can ionize other host atoms and thereby generate an electron avalanche effect that leads to a substantial current. The initial conduction electrons are either present in the conduction band or are injected from the metal in the conduction band as a result of field-assisted thermal emission from the Fermi energy in the metal to the conduction band in the dielectric [33].

3.5.2 Thermal breakdown

Any charge transfer or dielectric leakage induces heat in the dielectric material. If this heat cannot be removed from the dielectric quickly enough then the temperature of the dielectric will increase. This increase corresponds to a conduction increase of the insulating medium and an increase to the current until a discharge takes place. The inhomogeneities of the sample result in local overheat which leads to the physical and chemical erosion of the material because of the local melting. Therefore, the local breakdown generates a conducting channel connecting the opposite electrodes and hence to dielectric breakdown. The time needed to thermal dielectric breakdown to occur depends on E^2, and the dielectric strength E_{br} is inversely proportional to the temperature [33].

3.5.3 Insulator Aging

The term of aging is used to describe generally the degradation of the dielectric properties and the material life time. This degradation is due to physical and chemical aging of the dielectric even in the absence of the applied electric field or due to the presence of an electric field. For instance, dc fields can disassociate and transport various ions in the structure and thereby slowly change the structure and properties of the dielectric. Additionally, the electrical aging causes the generation of electrical treeing that are formed due to the application of an ac electric field. Ac fields create continual partial discharges in an internal or surface microcavity which then erodes the region around it and slowly grows like a branching tree [33].

3.6 High-k materials

The rapid development of microelectronics technology has been accompanied by the scaling down of the semiconductor device sizes [35]. This minimization of the device feature sizes offers lower power consumption, lower fabrication cost since more chips are present in a given wafer, higher capacitance densities and higher performance speeds. Taking into account equation, Eq.3.2, we can see that higher capacitance density is achieved either by reducing the dielectric thickness or by using a dielectric material with higher dielectric constant [36].

3.6.1 From SiO_2 to high- k dielectrics

As we discussed above, higher capacitance density is achieved by reducing the thickness of the dielectric film. Based on experimental data and calculations it was deduced that the lower limit of the SiO_2 thickness, which is used for more than 40 years as dielectric material, was 3nm to prevent high leakage currents. Thirty years ago, the gate oxide thickness was 120nm and nowadays is about 1.2 nm which is much thinner than the direct tunneling limit for SiO_2 , so it is obvious that we cannot reduce the thickness of the SiO_2 without a limited because such reduction leads to unacceptable values of leakage current [36]. Except for the thickness which is inversely proportional to the capacitance density, another parameter which can alter the value of the capacitance density is the dielectric constant k. The directly proportional relation between capacitance density and dielectric constant imposes that higher values of dielectric constant imply higher capacitance density. The implementation of higher – k materials therefore ensures high capacitance density and low leakage currents since physically thicker films are used [36].

3.6.2 Candidate high- k materials

The high-k dielectrics need to be used to prevent the tunneling effects which increase the leakage currents. In this way the candidate high-k materials which potentially replace the conventional SiO_2 should meet the following requirements such as high dielectric constant and large band gap, high band offset with electrodes, thermally and chemical stability with the semiconductor substrate, density of interface states comparable to SiO_2, low lattice mismatch and similar thermal expansion

coefficient with the substrate, high breakdown voltage, and negligible capacitance-voltage hysteresis [37]. Materials which have received considerable attention and are now being used or are under investigation are silicon oxinitride, alkali halides, lithium fluoride, barium titanate and metal oxides [38]. There are many problems associated with the implementation of high-k materials. For instance TiO_2 and barium strontium titanate (BST) show higher permittivity but their thermal stability with the semiconductor substrates should be tested. Extremely high-k materials such as BST cause field induced barrier lowering which degrades short channel effects of MOS transistor [35]. To overcome all these problems and reconstructions an examination of each factor is required. The most common used of them (some examples) are summarized in the following table, Table 1 [37].

Table 1: *In the following table the most common used dielectrics materials with their dielectric constant are summarized. The table is adapted from* [37].

<table>
<tr><th>Material</th><th>Dielectric constant k</th><th>Comments</th></tr>
<tr><td>SiO_2</td><td>3.9</td><td rowspan="2">Too low k</td></tr>
<tr><td>Si_3N_4</td><td>7.5</td></tr>
<tr><td>Al_2O_3</td><td>~10</td><td>High density of surface states</td></tr>
<tr><td>ZrO_2</td><td>~22</td><td rowspan="2">Promising</td></tr>
<tr><td>HfO_2</td><td>~25</td></tr>
<tr><td>La_2O_3</td><td>~30</td><td>Reactive with water vapor and small band offset with some substrates (i.e. Si)</td></tr>
<tr><td>Ta_2O_5</td><td>~25</td><td rowspan="2">Reactive with some substrate (i.e. Si)</td></tr>
<tr><td>TiO_2</td><td>~80</td></tr>
<tr><td>BST</td><td>~300</td><td>Reactive with some substrates (i.e. Si) and causes field induced barrier lowering.</td></tr>
</table>

3.7 Leakage current

Except for high dielectric constant, high- k materials should ensure low leakage currents. The main quantity that describes the amount of the leakage current is resistivity. Even though the measured resistivity is not an intrinsic property of the dielectric material it can be controlled by the purity, stoichiometry and crystallinity of the material. More specifically, impurities can create defect sites or act as mobile ions. Even any small deviation from the ideal stoichiometry can effectively dope the material causing an increase in the conductivity of the dielectric as it happens in the case of the grain boundaries in polycrystalline materials. Finally, a large barrier height at the interface between the electrode and the dielectric is required because this barrier avoids high leakage currents [35].

3.7.1 Conduction mechanisms in dielectric films

As we discussed above dielectric is a material that has a large band gap and a low conductivity, but under an external applied electric field carrier transport occurs through it, leading to electrical conduction. The carrier transport in dielectric materials not only depends on the dielectric itself but also on the electrode-dielectric contact. Thus, the most commonly found mechanisms that lead to conduction are classified into two categories, the electrode-limited mechanisms and the bulk-limited mechanisms, as shown in the following figure, Fig.23 [39].

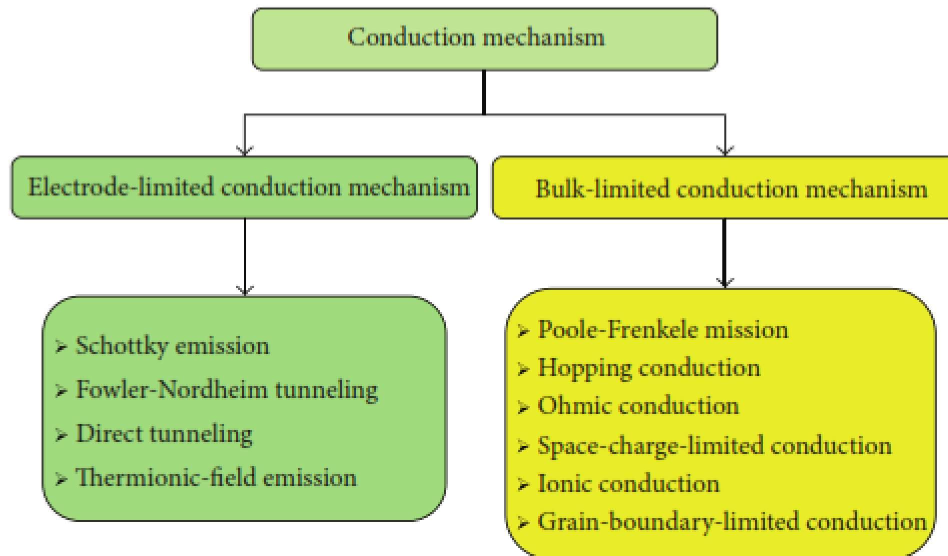

Fig.23: *Classification of conduction mechanisms in dielectric films. The image is adapted from* [39].

Electrode-limited mechanisms

The electrode-limited mechanisms depend on the electrical properties at the dielectric-electrode contact, such as the barrier height at the dielectric-electrode interface and include (1) Schottky emission, (2) Fowler-Nordheim tunneling, (3) direct tunneling, and (4) thermionic- field emission [39].

Schottky Emission: The electrons in the metal will obtain enough energy provided by thermal activation to overcome the energy barrier at the electrode-dielectric contact to go to the dielectric. This kind of emission is the most often observed mechanism in dielectrics films, especially at high temperatures [39].

Fowler-Nordheim Tunneling: F-N tunneling occurs when the applied electric field is large enough and the thickness of the barrier is thin enough (<100Å), so that the electrons pass through a triangular potential barrier into the conduction band of the dielectric. The tunneling current dominates at very low temperatures where the thermionic emission (Schottky emission) is suppressed [39].

Direct Tunneling: Except for F-N tunneling there is also another type of tunneling, the direct tunneling. The F-N mechanism dominates when the voltage across the dielectric is high and the dielectric thickness is above 4-5nm. On the other hand, the

direct tunneling dominates when the voltage across the dielectric is small and the dielectric thickness is less than about 3.5nm. In the last case, carriers flow from one electrode directly to the other through the dielectric film [39].

Thermionic-field emission: This condition, is similar to field and Schottky emission. The fundamental difference is that in the thermionic-field emission the tunneling electrons should have the energy between the Fermi level of metal and the conduction band edge of the dielectric. A comparison of thermionic, field and thermionic-field emission is illustrated in the following figure, Fig.24 [39].

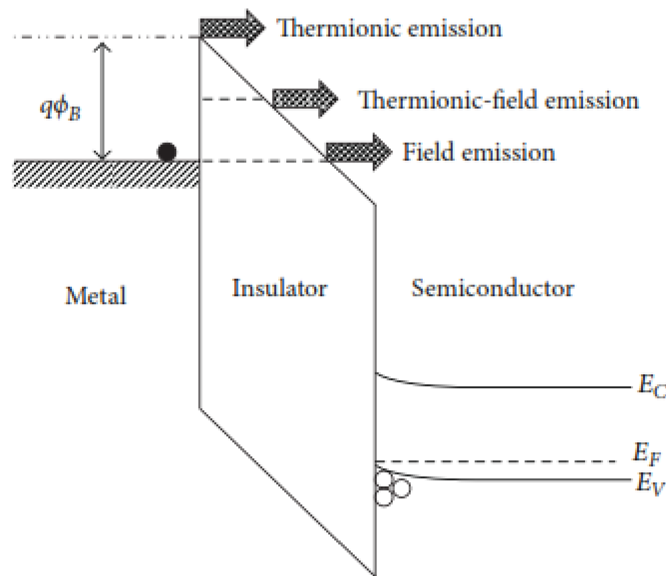

Fig.24: *Comparison of thermionic-field emission, thermionic emission, and field emission in metal-insulator-semiconductor structure. The image is adapted from* [39].

<u>Bulk-limited mechanisms</u>

The bulk-limited conduction mechanisms depend on the electrical properties of the dielectric film itself and include (1) Poole-Frenkel emission, (2) hopping conduction, (3) ohmic conduction, (4) space-charge-limited conduction, (5) ionic conduction, and (6) grain-boundary-limited conduction [39].

Poole-Frenkel Emission: In this condition, the thermal excited electrons are emitted from the traps into the conduction band of the dielectric. The trap when filled with an electron is neutral while when empty is positively charged. Thereby, a Coulomb force is generated between the trap and the electron [40]. The Coulomb potential energy of

the electron can be reduced by an applied electric field across the dielectric film. This reduction increases the probability of an electron being thermally excited out of the trap. This conduction mechanism is often observed at high temperature and high electric field [39].

Hopping Conduction: This conduction mechanism is based on the tunneling effect of a trapped electron from one trap to another. In this condition the carrier energy is lower than the maximum energy of the potential barrier between two trapping sites and any transit may occur due to tunnelling mechanism [39].

Ohmic Conduction: Ohmic conduction is based on the movement of mobile electrons in the conduction band and holes in the valence band, respectively. The electrons in the conduction band come from excitation processes. The electrons are excited from the valence band leaving a hole behind or from the impurity levels. The probability of electron existence in the conduction band due to this conduction mechanism is very small, consequently the current density is small as well, but not zero. This current mechanism can be observed at very low voltage in the I-V characteristics, and the ohmic current is linearly dependent on the voltage [39].

Space-Charged-Limited Conduction: This conduction mechanism is similar to the transport conduction of electrons in a vacuum diode. In solid materials, the current that is based on this mechanism is caused by the injection of electrons from an ohmic contact. At low voltages an ohmic behavior between current and voltage is observed indicating that the number of the thermally generated free carrier is larger than the number of the injected carriers. On the other hand, at high voltages (larger than the voltage of the traps-filled limit) where the traps are filled up the density of the injected carriers exceeds the density of the thermally generated carriers and a space charge layer is formed in the dielectric. This layer controls the space-charged current and limits the further carrier injection [39].

Ionic Conduction: In this condition the conduction is carried out by the ions when an external electric field is applied. The influence of the electric field results in the jump of the ions over a potential barrier from one defect site to another [39].

Grain-Boundary-Limited Conduction: In this case the conduction current could be limited by the electrical properties of the grain boundaries via a potential energy

barrier that these build. A major factor that affects the potential barrier is the dielectric constant, which is inversely proportional to the potential barrier height [39].

3.8 Deposition of Dielectric Thin Films

3.8.1 Atomic Layer Deposition (ALD) of Dielectric Films on Graphene

Even though we will talk about the atomic layer deposition technique in Chapter 5, it is necessary to refer to this technique and discuss in detail about this method and its applicability on graphene, since this thesis is engaged with the implementation of the graphene as a channel material in graphene field effect transistors. It is well known that ALD method is the preferred technique to achieve high quality, conformal, ultrathin dielectric films with precise thickness control at low deposition temperatures, however, restrictions such as the lack of dangling bonds and the hydrophobic nature of the graphene surface inhibits direct deposition of uniform ALD dielectrics. To overcome these restrictions many different methods have been developed including: deposition of an e-beam metal seed layer, ozone pretreatment, a low k-polymer seed layer, and a wet pretreatment [41].

Ozone Treatment: It is about a gas pretreatment that results in the increase of the number of the nucleation sites on the basal plane of the graphene prior to dielectric deposition. This functionalization occurs mainly through an increase in the concentration of epoxide functional groups after the ALD oxides, with little disturbance on the sp^2 arrangement or etching effect on the graphene. Any defects introduced by the ozone pretreatment can be reduced by lowering the exposure temperature and by reducing the number of ozone pulses [41].

Wet Treatment: In this case the sample is immersed in DI water to fabricate ALD nucleation by removing any residues from the graphene surface and by altering the graphene bonding without compromising the electrical or structural properties of graphene. A combination of DI water rinse and a dry clean with N_2 leads to conformal oxide coverage on both terraces and step edges with minimal impurity incorporation [41].

Polymer Buffer Layer: In this treatment a low-k polymer buffer layer is used in order to obtain a uniform high-k dielectric. PTCA (perylene- tetracarboxylic acid) is

considered as a perfect seed layer candidate for ALD of Al_2O_3 providing suitable reaction sides for ALD resulting in turn to a dense uniform coating on the graphene surface due to its negatively charged terminal carboxylates and its highly separation of the methanol . On the other hand, NFC 1400-3CR which contains methyl and hydroxyl groups, has been used as a low-k polymer buffer prior to HfO_2 deposition providing a uniform coating of the entire gated area of the graphene channel. Finally, a disadvantage of this treatment is the high doping that causes to graphene film resulting in large shifts on the Dirac voltage point, but an annealing in O_2 plasma atmosphere may reduce these shifts [41].

Metal Seed Layers: In this case fully oxidized e-gun evaporated seed layers are used to obtain uniform high-k dielectric films on graphene. These layers are located between the dielectric film and the graphene surface. The metal seed layer/graphene stack before being transferred to the ALD chamber, is exposed to air and an additional H_2O oxidizing cycle is carried out to ensure complete oxidization. In order to exploit the advantages that this treatment offers to us, an appropriate choice of the seeding layer and a preparation of the graphene surface prior to seeding layer deposition are required to prevent any degradation of the electrical properties of the graphene that arise from the interaction between the seeding layer and graphene [41].

4. Graphene Field Effect Transistors

In this chapter of the thesis, we will describe the first principles of graphene field effect transistors (GFET). Many of the terms that we are going to use in order to describe the behavior of such transistors are well known from the Si- MOSFETs devices, but some of them need a modification due to the two- dimensional nature of graphene which is used as the channel material.

4.1 Structure of a GFET

The basic structures of a GFET are illustrated in the following figure, Fig.25, where all the structures consist of the metal-oxide-graphene structure. The graphene layer plays the role of the channel which extends between two junctions. When a voltage is applied between the junctions, electrons can enter the channel at one junction, called the source, and leave at the other, called the drain [42]. In the following figure, Fig.25, we have three different structures of GFETs, the first one, Fig.25a, corresponds to a back-gated graphene transistor, where the substrate which is usually a highly doped Si acts as a back gate covered by a dielectric layer, and above the dielectric film the graphene is contacted to form the source and drain electrodes. The second one, Fig.25b, corresponds to a dual-gate graphene transistor resulting after the deposition of a top dielectric layer above the graphene layer allowing a top gate electrode to be deposited. In this case we are able to control the conductivity (charge concentration) of the channel by applying biases both on top and back gate electrodes. And the last one, Fig.25c, corresponds to a graphene transistor structure, in which the graphene is epitaxially synthesized on silicon carbide (SiC) wafers covering the entire substrate while above graphene there is a dielectric film that is deposited allowing the formation of a top gate electrode [43]. Summarizing, carriers enter the graphene channel from the source pad, leave from the drain pad while their concentration into the channel is controlled by the gate pad. The dielectric layer plays the role of the separating barrier between the gate pad and the graphene channel.

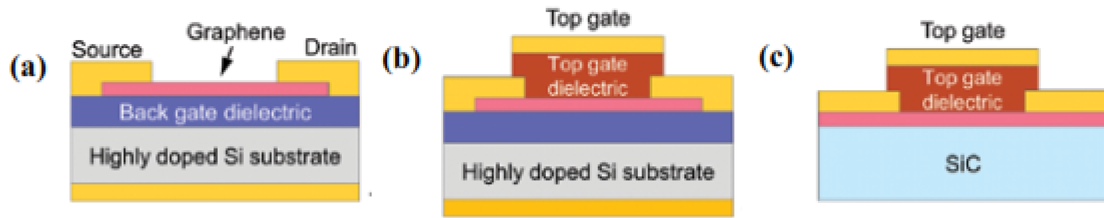

Fig.25: a) *Back-gated graphene transistor; b) dual-gate graphene transistor; c) epitaxial graphene from SiC and transistor structure. The image is adapted from* [43].

4.2 Electric field effect in graphene

The electric field that is generated by an externally applied voltage can modify the electronic properties of a material, such as the electric current through graphene. The graphene sheet resistivity ρ, exhibits a sharp peak when the gate voltage varies within a range of applied biases. This gate voltage which corresponds to the peak of resistivity indicates the minimum but non zero conductivity point. As a consequence the graphene conductivity $\sigma=1/\rho$, increases linearly with the applied gate voltage on both sides of the resistivity peak implying the ambipolar field effect in which both holes and electrons contribute to the graphene conductivity. The contribution portion of each carrier type is determined by the position of the Fermi level, which changes due to the surface charge density- $n=\varepsilon_o\varepsilon V_g/te$, where n is the surface charge density, ε_o and ε are the permittivities of free space and dielectric film respectively, t is the thickness of the dielectric film and e is the electron charge - that is induced by the gate voltage (electric field doping) [44].

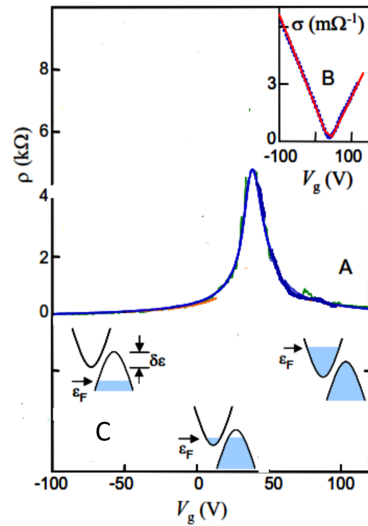

Fig.26: *Field-effect in graphene. (A) Typical dependence of graphene's resistivity ρ on gate voltage. (B) Example of change in channel's conductivity σ=1/ρ. (C) Example of Fermi level, ε_F, shift. The image is adapted from* [44].

4.3 Current- Voltage characteristics of GFETs

The first thing that we have to do in order to electrically characterize the operation of graphene field-effect transistors, is to extract the current- voltage characteristics, namely the drain-to- source current (I_{DS}) as a function of gate voltage (V_G) for a constant drain-to-source voltage (V_{DS}) and the drain-to- source current as a function of drain-source voltage for a range of gate voltages. Hereafter, the first characteristics will be called transfer characteristics while the latter will be called output characteristics, respectively.

Transfer characteristics

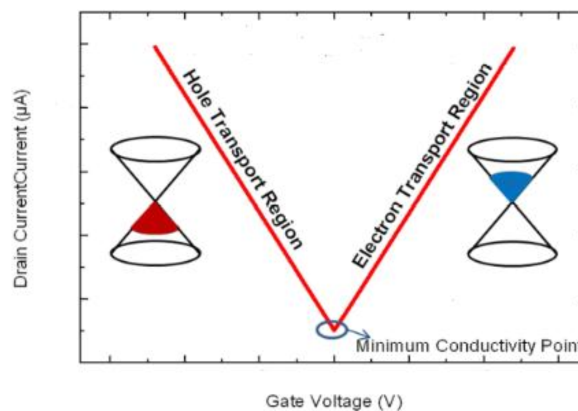

Fig.27: *Schematic of typical transfer characteristics of a graphene-based FET. The image is adapted from* [45].

In the above figure, Fig.27, typical transfer characteristics of a graphene field-effect transistor are illustrated. The ambipolar characteristics due to the absence of band gap in graphene channel are clearly observed. The minimum conductivity point corresponds to the so called Dirac point, in which the conduction based on holes changes to conduction based on electrons. So it is obvious, that for $V_G > V_{Dirac}$ we refer to the electron transport region, the right side of the transfer characteristics where the Fermi level is in the conduction band while for $V_G < V_{Dirac}$ we refer to the hole transport region, the left side of the transfer characteristics where the Fermi level is in the valence band. The Dirac voltage, V_{Dirac}, essentially is in analogy to the flat-band voltage as in the conventional MOSFETs. Away from the Dirac point the drain current is higher because of the availability of carriers, but close to the Dirac point the drain current is very low but non zero. This minimum conductivity is due to a remaining thermal distribution of carriers and spatial fluctuations of energy in the Dirac point. The transfer characteristics depicted in the Fig.3 is a typical or ideal curve of graphene based field-effect transistors. In real cases, an asymmetry is observed between the p-branch and n-branch of the transfer characteristics. This asymmetry is attributed to the formation of p-n junctions between the channel and the source and drain regions depending if the gate voltage is larger or lower than the flat-band voltage ($\equiv V_{Dirac}$) [46].

Output characteristics

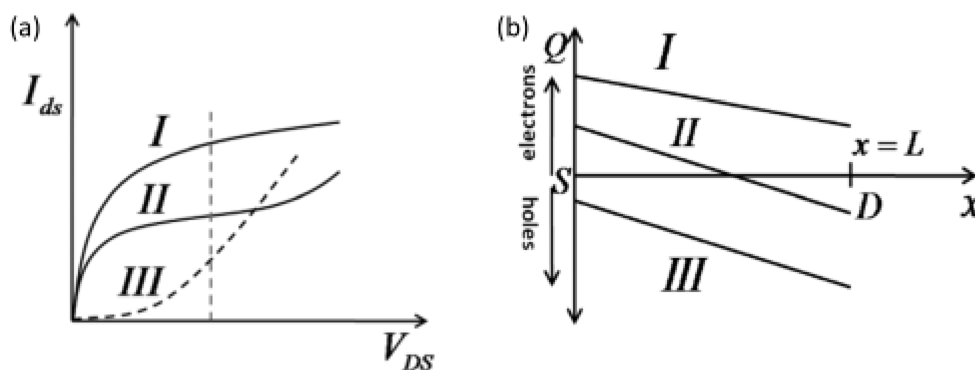

Fig.28: (a) *Schematic of qualitative Output characteristics of a graphene based field-effect transistor.(b) Total charge density as a function of the source-drain distance. The image is adapted from* [46].

In the above figure, Fig.28, qualitative output characteristics of graphene field-effect transistors for different gate voltages and positive drain-source voltages are illustrated. Moving from curve I to curve III the gate voltage decreases. The first thing that we can observe in the output characteristics, Fig.28a, is that the drain-source current (I_{DS}) increases with increasing gate voltage (V_G). Curve I corresponds to a n-type graphene channel where the drain-source current (I_{DS}) sub-linearly increases as the drain-source voltage (V_{DS}) increases, while the total charge density decreases as we move within the graphene channel. Curve III corresponds to a p-type graphene channel where the drain-to-source current (I_{DS}) super-linearly increases as the drain-to-source voltage (V_{DS}) increases, and as it depicted in Fig.28b the charge concentration so as the conductivity also increases with the increasing distance between source and drain. On the other hand, Curve II represents a combination of the two aforementioned cases, meaning that the channel conductivity changes with respect to the drain-source voltage (V_{DS}) from n-type to p-type. This change occurs at the point where Curve II intersects Curve III. The conductivity is large on either side of the intersection point but the drain-source current is reduced due to the reduced conductivity close to the meeting point, but it increases again with increasing drain-to-source voltage [46].

At this point, it is worth to talk about the saturation regime, where the current saturates. Although the diffusive regime dominates in transport, unlike with the MOSFETs where the pinch-off and velocity saturation lead to the saturation regime, in graphene based field-effect transistors due to the absence of the pinch-off in bulk graphene the drain-to-source electric field must be large enough to cause velocity saturation. A possible obstacle to such devices operating in saturation regime, even though high mobilities have been reported, is the poor contact quality on graphene. Thus, higher quality metal contacts on graphene are crucial in order to achieve velocity saturation [46].

4.4 Important parameters of GFETs

4.4.1 Transconductance

Transconductance, denoted as g_m, is an important parameter in GFET characterization, due to the fact that it gives a measure of the gate sensitivity. Moreover, it describes the change of drain-to-source current, I_{DS}, with respect to a change in gate-to-source voltage, V_{GS}. Mathematically, transconductance is given by the following formula

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} |V_{DS} = constant. \quad (4.1)$$

As we can observe from the above equation, Eq.4.1, the higher the transconductance is the higher the gate sensitivity that is implied.

4.4.2 Quantum Capacitance

In graphene based field-effect transistors, since there is no depletion layer as in conventional MOSFETs, the only capacitance components are geometrical capacitance C_G, capacitance that is related to the interface trap charge density C_{it} and the quantum capacitance C_q [64]. The quantum capacitance is defined as

$$C_q = \frac{dQ}{qdE_F} \quad (4.2)$$

and represents the extra voltage required to modulate the charge density for a fixed electrostatic potential [46].

4.4.3 Mobility in Graphene

As we have referred in Chapter 1, one of the unique properties that makes graphene a perfect candidate material for a post-silicon epoch, is the extremely high values of carrier mobility. Moreover, in the absence of charged impurities and ripples, mobilities of 200,000 $cm^2\ V^{-1}\ s^{-1}$ have been predicted [47]. Nevertheless when graphene is utilized in transistors the mobility of charge carriers degrades significantly due to extrinsic scattering mechanisms such as charged impurities on top of graphene, or at graphene/substrate interface, or at graphene/dielectric interface, and interfacial and substrate phonons. Under the Boltzmann transport formalism, the

linear dependence of conductivity on the carrier density at high carrier densities implies the domination of the charged impurities scattering mechanism. Therefore, taking into account that the mobility and conductivity are related to each other with the relation $\mu=\sigma(n)/n$ and the fact that the conductivity is related to the carrier density n and charge impurity density near the graphene/substrate interface n_i with the relation $\sigma \propto n/n_i$, the mobility can be increased either by removing the substrate and hence minimizing charged impurities near the graphene surface, or, for a fixed impurity density, using high-k dielectric films [46]. In the case of Coulomb scattering, on the other side, the mobility does not depend on the carrier concentration, n, but on the strength of the Coulomb scattering potential. Therefore, by increasing the dielectric constant of the surrounding environment the Coulomb scattering potential decreasing leading to higher carrier mobilities. Both mobilities depend on charged impurities and Coulomb scattering are independent on the temperature for low energies [46].

On the other hand mobility affected by acoustic phonon scattering depends both on carrier concentration and temperature, $\mu_{Ph} \propto 1/nT$. Fortunately at low energies both acoustic and optical phonon scattering is weak in graphene allowing for high carrier mobility comparatively with conventional semiconductors [46], [18]. Other scattering centers that affect the carrier mobility originate from the supporting substrate below the graphene channel and the gate dielectric above it. The supporting substrate could degrade carrier mobility via induction of charge impurities (Coulomb scattering centers), remote phonon scattering centers, and through its morphology since any local discontinuity of the substrate may introduce higher resistances. Except for the substrate material the other material that comes in contact with graphene channel is the top gate dielectric layer. In order to achieve such a contact in most cases has deleterious effects on carrier mobility due to the doping that is induced during the growth of the dielectric film and the process steps. Therefore, a suitable growth mechanism and the right choice of the most suitable dielectric material are required to benefit from the exceptional properties of graphene [18].

4.4.3.1 Extraction of mobility in the GFETs

In this section, we are going to briefly discuss how we can extract mobility using field-effect measurements in GFETs. Three different extraction methods will be discussed and compared, based on their accuracy and applicability.

Transfer length method (TLM). Although it is used to measure the contact resistance of graphene/metal junctions, under appropriate expansion it can be used to extract the carrier mobility, since in this method the sheet resistance (conductivity) is taken into account as well. Based on field-effect measurements, contact resistance can be extracted using I_{DS}-V_G characteristics, while carrier mobility can be extracted using the gate voltage dependence sheet (graphene channel) resistance. By linear fitting R_{total} of GFETs with different channel lengths under the same net voltage (V_G-V_{Dirac}), we can obtain R_{sheet} and R_c from the slope and intercept respectively. The carrier mobility μ_{TLM} can be extracted from the R_{sheet} –(V_G-V_{Dirac}) relation

$$\mu_{TLM}(V_G - V_{Dirac}) = 1/qn\,(V_G - V_{Dirac})R_{sheet}(V_G - V_{Dirac}) \quad (4.3)$$

in which $n(V_G - V_{Dirac})$ is the gate voltage dependent carrier density in graphene, an is equal to

$$n(V_G - V_{Dirac}) = \sqrt{n_0^2 + (C_G|V_G - V_{Dirac}|^2)} \quad (4.4),$$

where n_0 is residual carrier density induced by charge impurities and C_G is the gate capacitance of GFETs. The gate capacitance if the quantum capacitance of graphene is larger than the capacitance of the gate insulator is given by the following expression

$$C_G = \frac{\varepsilon\varepsilon_0}{t_{ox}} \quad (4.5),$$

where ε, ε_0 are relative and absolute dielectric constant and t_{ox} the dielectric thickness. The mobility here is calculated if the n_0 is known [48].

Direct transconductance method (DTM). In this method the mobility is extracted from the gate voltage dependent transconductance through the expression

$$\mu_{DTM} = g_m \frac{L}{WC_G V_{DS}} \quad (4.6),$$

where $g_m = \frac{dI_{DS}}{dV_G}$ is the transconductance and μ_{DTM} is the field-effect mobility. With this extraction method the mobility value is always lower than of that the one that is extracted by the TLM method, due to non taking the contact resistance into account [48].

Fitting method (FTM). It is about another popular method in which the mobility is extracted from the transfer characteristics of a GFET. For the fitting of transfer curves the following expression is used

$$R_{Total} = R_c + \frac{L}{W}\frac{1}{\mu_{FTM} n(V_G - V_{Dirac})} \quad (4.7),$$

where n is the gate dependent carrier density given by equation (4.4). In this method both the carrier mobility μ_{FTM} and contact resistance R_c are assumed to be constant. Using the above fitting equation for the transfer characteristics the carrier mobility, contact resistance and residual carrier density for both two branches can be obtained. The mobility that is extracted for this method is higher than DTM mobility, and in many cases it could match the mobility at the Dirac point [48].

In the following table, Table 2, the three aforementioned mobility extracting methods are summarized and compared. As we can see, the TLM is the most accurate method providing carrier density dependent mobility and contact resistance as Hall measurements, but the complexity of sample fabrication is high because devices with various channel lengths are required. DTM is the easiest method, providing underestimated carrier density dependent mobility and cannot calculate the contact resistance at the same time. On the other hand, FTM can provide overestimated carrier mobility and contact resistance, assuming that both of them are constant and independent on carrier density [48].

Table 2: *Comparison of three mobility extracting methods based on the field-effect measurements for graphene. The table is adapted from* [48].

Method		TLM	DTM	TFM
Complexity of sample fabrication		High	Low	Low
Mobility	**Accuracy**	High	Underestimating	Overestimating
	Carrier density dependency	Yes	Yes	Constant
Contact resistance	**Accuracy**	High	Unable	Overestimating
	Carrier density dependency	Yes	Unable	Constant

5. Micro fabrication

Modern solid state electronics owe their great success to device fabrication techniques which can produce extremely complicated devices with high yield [49]. In this chapter, even though processing is out of the scope of this thesis, we briefly present the main steps of the microelectronics processing.

5.1 Lithography

Lithography is a photographic process that involves light exposure through a photolithography mask to project the image of a design onto a substrate, much like a negative image in standard photography. This process requires the existence of light-sensitive chemical substances called photo-resists, which coat the wafer to be patterned.

5.2 Photo-resist coating

In order to make the wafer to be patterned sensitive to optical beams, a photo-resist is spread on it by a process called spin coating. Spin coating has emerged as the most reliable technique for photo-resist application. A small puddle of the resist is applied to the center of a wafer which is held on a spindle. As the spindle spins most of the resist is thrown off and drained away. The remaining resist forms a thin layer whose thickness depends on the spin speed (thickness $\sim 1/\sqrt{\omega}$, where ω is the spin frequency [49]. At this point, it must be mentioned that the adhesion between the resist and the wafer plays a crucial role. To achieve this, a pre-bake and a post-bake treatment are required. The pre-bake treatment takes place before the resist deposition to remove any hydroxyl groups that an untreated wafer may have, while the post-bake treatment follows the resist deposition to remove the solvent and enhance the adhesion between the resist and the substrate surface [49].

Once the resist is ready, it is exposed to an optical image through mask for a certain exposure time. The resist is then developed by washing it in a solvent which dissolves away the regions of higher solubility. A resist which becomes more soluble when exposed to illumination is called positive and its image is identical to the

opaque image on the mask plate. A resist that reduces its solubility when illuminated is called negative [49].

5.3 Mask generation and image transfer

As we discussed above, when the resist is in place, one needs to expose it with an optical image, containing the pattern to be transferred to the wafer. This requires the fabrication and use of a mask. Like the negative in the photography, the mask allows one to transfer the complicated pattern onto the sensitive resist deposited on the wafer. Nowadays, for the generation of a design, computer aided design programs are used and then this design is written on to a mask by optical or electron beam writing. The mask plate must be transparent at proper positions for the radiation used to travel to the substrate surface and should also have good mechanical and thermal properties [49].

The equipment for image transfer depends on the feature size. For feature size greater than 0,25μm, one can use optical equipment. This limit is governed by the wavelength of the light available. For smaller feature size one can use x-ray lithography with an appropriate wavelength of 40-80Å or more commonly electron beam lithography [49].

5.4 Etching

Etching is the process whereby one can remove material in a selective manner, once the resist has been patterned. An ideal etching process must be able to remove a layer of semiconductor from the region where there is no resist. Thus, the etchants should not attack the resist, nor should it penetrate under the resist causing undercuts. It should attack only one layer and should be self limiting. Once etching is finished, one must remove resist material by either other etchants or by solvents. Because of its importance in microelectronics processing a number of techniques are developed to carry out etching [49].

5.4.1 Wet chemical etching

In this technique which is the simplest and the used to be the most commonly used, the wafer is soaked in a liquid chemical which dissolves away the

semiconductor. This removal is achieved by a chemical reaction between the elements of the films to be etched and the etching solution. The reactions products can have to be dissolved by the solution to be carried away for the etching to continue. The rate of the etching is proportional to the etch time, it depends upon the concentration of the chemicals used in the etchant and the temperature of the solution, and is usually isotropic. Due to the very sharp sidewalls to be produced, the isotropic nature of this technique is not always suitable for devices and it is not compatible with submicron technology which demands deep anisotropic etching. The most usual etchants are HF, HNO_3, $H_4C_2O_2$, H_2SO_4, H_3PO_4, NH_4OH, and are usually diluted in water [49].

5.4.2 Dry etching

Dry etching is divided into three types: chemical dry etching, physical dry etching (sputtering, ion beam milling) and the third type which is a combination of physical and chemical dry etching (RIE). The main idea of all types of dry etching is the utilization of plasma. Plasma as it is known is the one of the four fundamental states of matter. The matter in plasma contains ions, free radicals and by-products [49].

The plasma is produced by passing an RF electrical discharge through a gas in a chamber where the pressure is low. The RF discharge creates ions and electrons. The ions which are charged particles can be accelerated in the electric field and be made to bombard the substrate with controlled energy, causing etching. The type of etching manner, selective or not, depends on the ions species and their energy. If the energy is large we have less selective manner in atoms removal otherwise at low energies the removal of atoms is primarily defined by chemistry. The electrons that are created by the alternating field oscillate. The motion of the electrons results in a number of processes such as excitation, dissociation and ionization. The electrons can excite one or more bound electrons from the atom or molecule into a higher state. As the excited atom returns to the ground state it emits a photon, this is why a glow appears. The dissociation occurs when the energy of an atom is high enough to break a bond in a molecule providing a free atom which reacts chemically with the surface of the sample. The neutral atoms created by this process are called radicals and they are also chemically active. Finally, in the case of ionization the positively charged

atoms or molecules are accelerated by the electric field giving a rise to the physical etching [49].

A question that should be arisen is what is the behavior of electrons and ions near the electrode where the sample is placed? The walls, of the chamber where all the above processes take place, are grounded so any important attraction or repulsion of charged particles, occurs near the electrode where the sample is located. Electrons close to the electrode hit the surface of the sample and are trapped, charging this region negatively. As the voltage of the electrode builds up, the electrons being negatively charged are repelled while the positively charged ions are attracted. A steady state is achieved when the rate of the hitting electrons becomes equal to the rate of ions [49].

5.4.2.1 Chemical dry etching

This technique based on chemical reaction that radicals and ions cause when they come in contact with the surface of a semiconductor forming volatile products. This process depends on the chemical structure of the material that is to be etched and the reactant species that are created in the plasma. Being a chemical technique it is independent from the kinetic energy of the reactants this is why it could take place at low DC bias. DC bias is the potential difference on the electrode where the sample is positioned. The free radicals and by-products decrease the activation energy in a chemical reaction, resulting in material removal [49], [50].

5.4.2.2 Physical dry etching

In this technique we use noble gas ions such as Argon to bombard the wafer surface. Etching occurs by physically knocking atoms out the surface. Ions are accelerated by the potential difference between the area above the electrode where there are not electrons (sheath region) and the electrode. This potential difference accelerates ions towards the electrode, giving to ions kinetic energy high enough to remove atoms from the surface of the sample. In contrast to the chemical dry etching, physical etching occurs in high DC bias because a high kinetic energy is required. This process is known as sputtering [50].

5.4.2.3 Reactive Ion etching

From the point of view of micro-fabrication, the most useful dry etching technique is the Reactive Ions Etching (RIE). This technique combines the physical and chemical dry etching technique which means that etching occurs through chemical reaction and physical momentum transfer from the etching species to the sample. Initially the substrate that is to be etched is placed in reactive plasma which contains the etchant gases. The function of the plasma is to generate reactive species (radicals and ions) which can assist the removal of material, as it is described above [51].

5.4.2.4 Ion Beam Milling

The ion beam milling is another application of the ions in removing material from a substrate. This technique requires a focused beam of ions of energy high enough that ions can physically knock out atoms from the target, rather than through chemical reaction. Ion milling is particularly advantageous if the etching involves small patterns due to its high directionality [49].

5.5 Dry etching parameters

The dry etching process can be controlled via several parameters such as chamber pressure, gas flow, gas type, dc bias and RF power. The chamber pressure has to do with the pressure that prevails inside the chamber. Low pressures result in higher kinetic energy and higher probability that an ion reaches the surface. On the other hand, high pressures result in less kinetic energy, and higher density of atoms. In the case of low pressures physical etching dominates while at high pressures the chemical etching does. The gas flow is referred to the necessity of replenishing the gas with fresh one. Keep in mind that the gaseous components that react with the sample to be etched increasingly diminish. The rate of replenishment is controlled by the flow measured in standard cubic centimeters per minute. Finally, the RF power is controlled by changing the amplitude of the electric field. The frequency of the generator is not tunable and is usually fixed at 1.356 MHz or 13.56MHz (frequencies

designated for plasma power sources. Any increase of the electric field results in higher kinetic energy of particles. In this case, at high RF power, the velocity of which ions hit the target is higher and the mechanical etching is enhanced. This enhancement of mechanical etching may cause damages on the sample [49], [50], [51].

5.6 Thin film deposition

Thin film deposition processes deposit thin, uniform coatings of various materials onto wafers. There are several methods of thin film deposition such as thermal and e-gun evaporation, sputtering, chemical vapor deposition, and electrochemical deposition. Each of these methods has its advantages and disadvantages, and is capable of depositing a variety of metals, dielectrics or other materials [52].

5.6.1 Thermal evaporation

Evaporation is a physical vapor deposition process in which the wafer is placed in a chamber and subjected to very low pressure. A vacuum pump is used to remove gases from the chamber. Once chamber is free of residual gases the material to be deposited is subjected to a temperature sufficient to cause it to evaporate. The evaporated molecules are dispersed throughout the chamber landing on the wafer coating it uniformly [52].

5.6.2 Sputtering as a physical deposition technique

Sputtering is another physical vapor deposition technique which takes place in a vacuum chamber. The material to be deposited is bombarded with high energy ions from a glow discharge. As ions hit the target they eject its atoms and molecules. These atoms and molecules coat the wafer, condense and form a thin film. Sputtering except for metals deposition, it is also used for insulating films deposition [52].

5.6.3 Chemical vapor deposition

Chemical vapor deposition (CVD) takes place in a vacuum or at atmospheric pressure. This technique is typically used to deposit insulating and semiconducting films. Reactant gases are placed in a vacuum chamber with the wafer, and an energy source is used to activate a chemical reaction causing the reactant gas molecules to break up, adsorb on the wafer and form a high quality thin film [52].

5.6.4 Plasma enhanced chemical vapor deposition

Plasma enhanced chemical vapor deposition (PECVD) is a process by which thin films of various materials can be deposited on substrates at lower temperature (typically 250~350 ^{o}C) than that of chemical vapor deposition (typically 600~800 ^{o}C) (CVD). [43]. In this method, deposition is achieved by introducing reactant gases between a grounded electrode and a RF- energized electrode. In this area a glow discharge (plasma) is generated and energy is transferred into a gas mixture. The product comes from chemical reaction between plasma and gas mixture is deposited on the substrate which is placed on the grounded electrode. [53],[54]. PECVD technique, is used in semiconductor manufacturing to deposit thin films such as silicon nitride, silicon dioxide, silicon-oxy-nitride and amorphous silicon. This deposition method also offers fast deposition rates and high quality thin films at lower deposition temperature as compared with other deposition techniques [53],[55].

5.6.5 Electrochemical deposition

This technique is typically used to deposit a thin conducting copper or gold layer which will be patterned to form interconnects connecting the various devices on an integrated circuit. The wafer is submerged upside down in a conducting copper sulfate solution. In the solution a copper electrode is connected to the positive side of the supply power (anode) while the wafer is connected to the negative side of the power supply (cathode). As current flows through the solution, copper ions near the cathode recombine with electrons from the current flow to form solid copper on the wafer [52].

5.6.6 Electron beam evaporation

Electron beam evaporation (e-beam evaporation) is a process similar to thermal evaporation i.e. a source material is heated above its sublimation temperature and evaporated to form a film on the surfaces. E-beam evaporation is more advantageous than thermal evaporation as a larger amount of energy is added into the source material resulting in a higher temperature in the evaporating target. This allows for materials with very high melting temperature to be evaporated such as W, Mo, Ta and other materials. The material to be evaporated is placed in a crucible or pocket. A filament below the crucible is heated. By applying a large voltage, electrons are drawn from the filament and focused as a beam on the source material. The beam is swept across the surface of the source material causing heating. Nowadays, a multiple crucible electron-beam gun is utilized for the deposition of several different materials in the same chamber [56].

5.6.7 Atomic layer deposition

Atomic layer deposition (ALD) is a technique capable of depositing thin film materials from the vapor phase at moderate temperatures ($<500\ ^{o}C$) [57]. A film is grown on a substrate by exposing its surface to alternate gaseous species, which are called precursors. It is similar with chemical vapor deposition (CVD) technique, but in contrast to CVD method, the precursors are never present at the same time in the reactor, but they are inserted separately [58]. Each precursor is pulsed into a chamber under vacuum (<1 Torr) for a specific time that is needed for a reaction between the precursor and the substrate surface through a self limiting process that leaves no more than one monolayer at the surface. Any un-reacted precursor or reaction by-products are pumped out of chamber via purging with the utilization of inert gases such as N_2 or Ar. This process is then repeated (cycled) in order to achieve the desirable film thickness. Despite the slow deposition rates of thin films (100-300 nm/h) and the carefully choice of the appropriate precursors (must be volatile enough but not subject to thermal decomposition), ALD method offers many advantages such as thin (typically less than one Angstrom/cycle), dense and smooth films with an excellent adhesion with the substrate. Finally, ALD technique is widely used in microelectronics for high-k gate oxides, high-k memory capacitors dielectrics, and

deposition for metal and nitrides for electrodes and interconnects deposition [57], [58], [59].

5.7 Rapid Thermal Annealing

Rapid Thermal Annealing (or RTA) is a process used in semiconductor fabrication. Unique heat treatments are designed for different effects. Wafers can be heated in order to activate dopants, change film-to-film or film-to-substrate interfaces, densify deposited films, change state of grown films, repair damage from ion implantation and move or drive dopants from one film into another or from a film into the wafer substrate. At this point, it must be noted that in this thesis RTA is used to create ohmic contacts through a controlled diffusion of a metal on the surface of the semiconductor. This process takes place in a chamber where the temperature and the speed of the annealing are controlled with accuracy. This accuracy and its short duration allow the diffusion of the metal with little or no defects in the substrate [60], [61].

6. Experimental

6.1 Metal-graphene contacts (Part I)

In this part we study the effect of O_2 plasma treatment prior to metal deposition and the effect of thermal annealing in ambient atmosphere, in vacuum and in forming gas atmosphere (H_2/N_2), on contact resistance and sheet resistance. In order to evaluate the contact and sheet resistance, we measured 5 TLM test samples. In the following section we give a description about their fabrication and information about their treatments.

6.1.1 Sample preparation

Graphene layers were grown on copper foils using chemical vapor deposition (CVD). After the growth, a monolayer of graphene was transferred onto a 285-nm-thick SiO_2 coated Si wafers. At this point, we have to say that the Si/SiO_2/monolayer graphene- substrates were acquired from the Graphene Supermarket. The TLM test structures were fabricated via photolithography, metal deposition and lift-off processes in our laboratory, MRG-FORTH.

More specifically, at first a thin layer of positive photoresist (1.25μm thick, AZ5214) was spin coated onto the graphene and the contacts were defined via photolithography. Following the photolithography process and prior to metal deposition oxygen plasma treatment was performed using 15 Watt power, with a 10ccm (cubic centimeter per minute) O_2 at 100 mTorr pressure and -64 Volts DC bias. Our samples were exposed to plasma for durations of 5, 10, 15 and 20 seconds to reduce the photoresist residues. After plasma treatment, Pd(50nm)/Au(100nm) was deposited through evaporation. The undesirable layers of photoresist and metals were removed via lift-off, by dipping the samples into a bath of acetone. Another thin layer of photoresist was spin coated onto our samples to define the graphene channel. The device structure was patterned with a graphene channel width of 250μm, while the graphene that was out of the TLM structure was etched via RIE (Reactive Ion Etching). The resist removal process concluded the sample fabrication, and the final TLM structure devices with an array of Pd/Au pads (250μm x 250μm) with 5, 10, 20, 30, 40, 50, 100 and 200μm separation distances between the contact pads were

obtained. All the previous steps are summarized in the following figure (Fig.29).

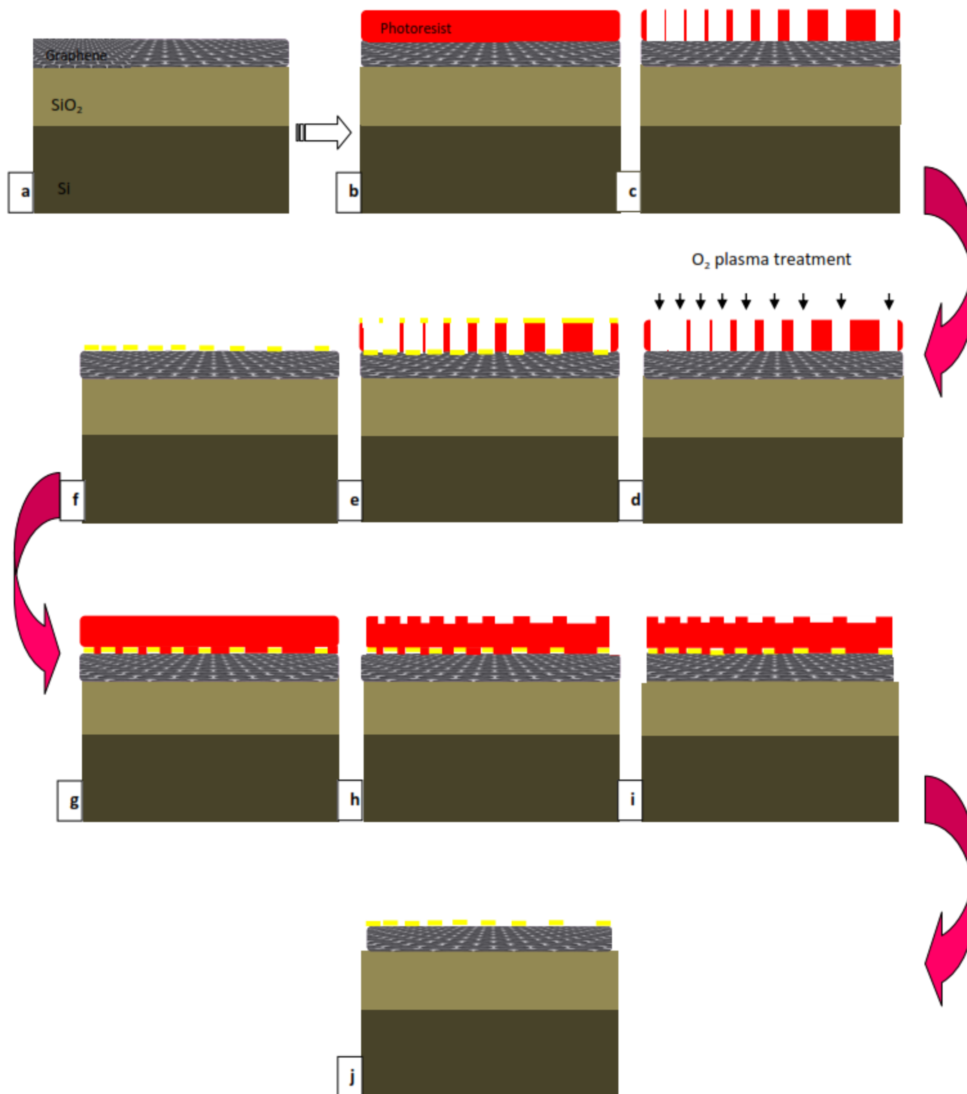

Fig.29: *Schematic illustration of the TLM test devices. a) Si/SiO$_2$/monolayer graphene, b) spin coating of photoresist, c) lithography for contacts, d) O_2 plasma treatment, e) Pd/Au deposition, f) lift-off, g) spin coating of photoresist, h) lithography for graphene channel definition, i) RIE etching, j) lift-off and final TLM structure.*

While the interface between the metal and graphene contact was cleaned by O_2 plasma, thermal annealing has been shown to be helpful for cleaning the graphene channel region. Thus, after the samples fabrication three different types of thermal annealing were applied on them: annealing in air at 300°C for 10 minutes, annealing in vacuum at 300°C for 10 minutes and annealing in forming gas (H_2/N_2) atmosphere

at 200, 300, and 400°C for 10 minutes respectively. All the samples with the corresponding treatments are depicted in the following table, Table 1.

Table 3: *In the following table the samples with their corresponding treatments are presented.*

Sample	O_2 plasma treatment time (sec)	No annealing	Vacuum annealing (300^OC for 10min)	Air annealing (300^OC for 10min)	Forming gas (H_2/N_2) annealing (200^OC,300^OC,400^OC for 10min)
Sample1	*0,5,10*	√		√	
Sample2	*0,15*	√	√	√	
Sample3	*0,20*	√		√	
Sample4	*0,5,10,20*	√	√		
Sample5	*0,10,15*	√			√

6.1.2 Data analysis

The contact resistances and sheet resistances were extracted through the transmission line method (TLM). Each of our samples was located on a probe station, as is shown in the following figure, Fig. 30. Our data were collected by using a semiconductor analyzer (370 Programmable Curve Tracer; Sony Tektronix), in ambient conditions.

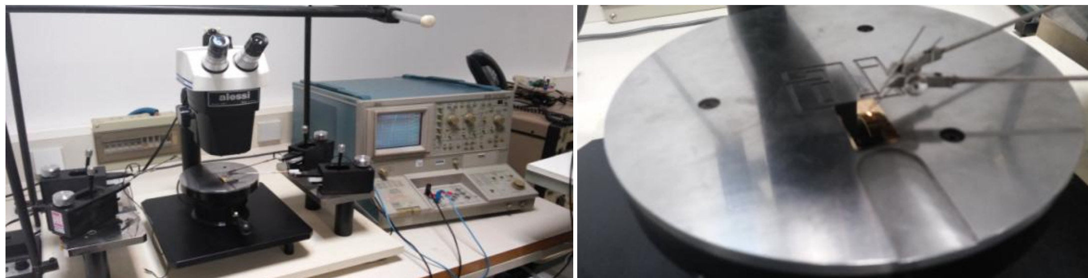

Fig.30: *Probe station and semiconductor parameter analyzer (Curve Tracer) which are used for the measurements conduct.*

For each pair of contact pads we applied voltage and we measured the current. We repeated this process for all the array of the contact pads. Then, for each pair of contact pads we calculated the total resistance R (Ohm) using the Ohm's law (R=V/I). The final step was plotting of the total resistance R versus the separation distance between the contact pads, d (μm). We extracted contact resistance R_c directly from the y-intercept of the R versus d curve, and the sheet resistance R_{sheet} from the curve's slope, as the theory of transmission line method (TLM) requires. Following, we introduce an example of the analysis method for better understanding.

In the following table, Table 2, we introduce the I-V measurements of the sample; Sample4; post-vacuum annealing. The first column contains the voltage and the second one the current measurements.

Let us examine the first row. To complete the third column with the values of the corresponding resistances, we use the Ohm's law. The fourth column results from the third column minus the parasitic resistance $R_{parasitic}$[1], which was equal to 1.98 Ω

Table 4: *I-V measurements. The data belong to sample Sample4 post-vacuum annealing, Period: 5EBTM.*

R_1=V/I=5.05e-1/1.25e-3
=4.06e+2 Ω

$R_{corrected}$= R_1- $R_{parasitic}$
= 4.06e+2-1.98
= 4.04e+2 Ω

V(V)	I(A)	R(Ohm)	Rcorrected(Ohm)	d(μm)
5,05E-01	1,25E-03	4,06E+02	4,04E+02	200
4,80E-01	2,09E-03	2,30E+02	2,28E+02	100
4,10E-01	3,83E-03	1,07E+02	1,05E+02	50
3,70E-01	4,44E-03	8,33E+01	8,14E+01	40
4,85E-01	7,44E-03	6,52E+01	6,32E+01	30
4,25E-01	8,86E-03	4,80E+01	4,60E+01	20
2,40E-01	9,32E-03	2,58E+01	2,38E+01	10
1,95E-01	1,26E-02	1,55E+01	1,36E+01	5

With the table completed, we can plot the total resistance versus separation distance d. So we select the fourth column and the last one, and we make the corresponding plot, as is shown in figure 31, Fig.31. To extract the contact resistance and the sheet resistance a linear fitting is required. After that, we can calculate the above quantities and the their derivatives, using the following formulas

Contact resistance R_c= (y-intercept)/2 ; R_c=(2.44±2.31) Ω

Sheet resistance R_{sheet}= (slope) × (W) ; R_{sheet}=(508.4±12.5) Ω/□

Transfer length L_T= (x-intercept)/2 ; L_T= 1.20 μm

Normalized contact resistance R_{CW}= R_c × W=(610±578) Ω μm, where W is the contact pad width; W=250 μm, equal to the channel width.[2]

Specific contact resistivity ρ_c= $(R_{CW})^2/R_{sheet}$=(7.34±6.02)e-6 Ωcm^2

[1] $R_{parasitic}$ is the resistance that is obtained when the two probes touch in the same contact pad.
[2] Hereafter when we refer to the contact resistance, we actually mean normalized contact resistance and it will be denoted as R_c.

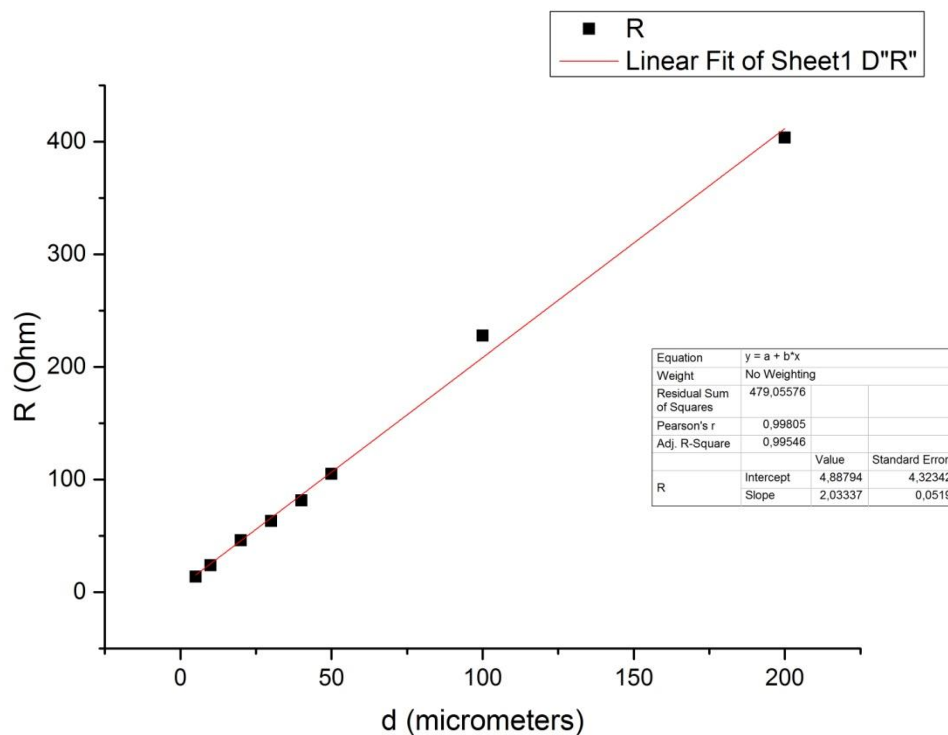

Fig.31: *The total resistance R(Ω) versus channel length d(μm) diagram of the data introduced in Table 2, with the corresponding linear fitting.*

6.1.3 Results and discussion

In this section the results of our measurements are presented and discussed. Our purpose was to find how the contact resistance (R_c) and sheet resistance (R_{sheet}) change with O_2 plasma treatment time and thermal annealing type. The structure of this section will be as follows:

Subsection 1: R_c versus O_2 plasma treatment time without thermal annealing
Subsection 2: R_{sheet} versus O_2 plasma treatment time without thermal annealing
Subsection 3: R_c versus thermal annealing type
Subsection 4: R_{sheet} versus thermal annealing type,

where in two first subsections the optimum O_2 plasma treatment time was determined, while in two last subsections the optimum thermal annealing type was determined, for contact resistance and sheet resistance respectively.

- ***Subsection 1: R_c versus O_2 plasma treatment time without thermal annealing***

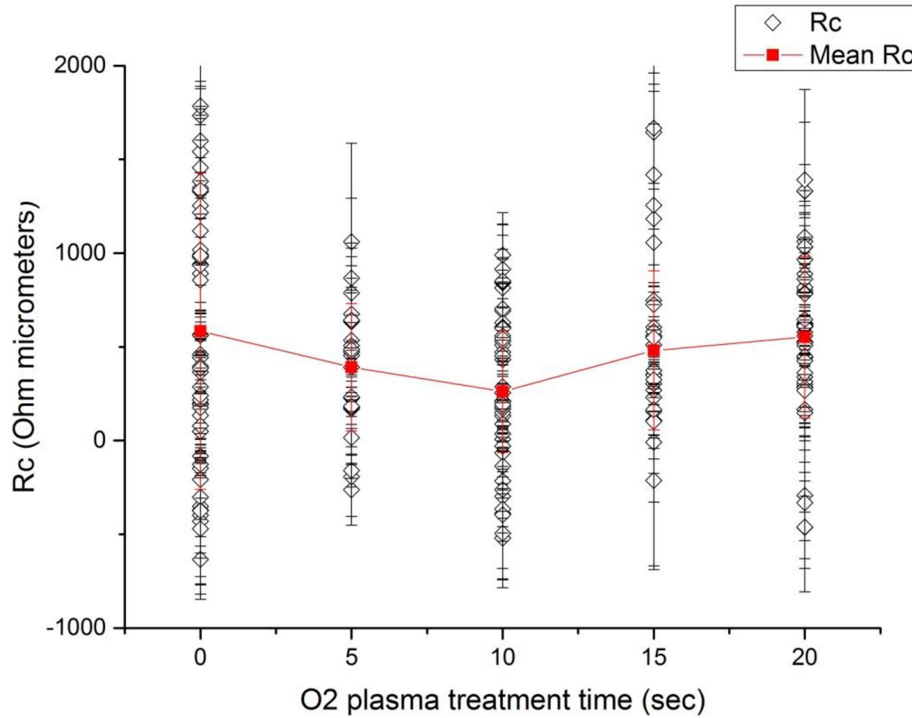

Fig.32: *Contact resistance R_c and mean contact resistance Mean R_c (Ω μm) versus O_2 plasma treatment time (sec) for all TLM test samples (Sample1, Sample2, Sample3, Sample 4, Sample5). 0sec of O_2 plasma treatment time is referred to the section of our samples without O_2 plasma treatment.*

The above figure, Fig.32, shows how the contact resistance R_c of the Pd/Au on graphene changes with the O_2 plasma treatment time. Trying to give a quantitative analysis in our results we will talk about the mean values of our measurements, however, the dispersion of our results is essential. So, as we observe the value of mean contact resistance was (584±845) Ω μm without plasma treatment, while as the surface of graphene prior to the metal deposition was treated this value decreases. Optimal contact resistance value of (284±325) Ω μm was achieved when the graphene surface was treated for 10sec. More specifically we see that the contact resistance with 10sec O_2 plasma treatment is reduced about 2 times with respect to the contact resistance without any treatment. This improvement in the value of contact resistance is due to the reduction of the photoresist residues indicating the plasma treatment is an effective cleaning method in providing good contacts. Returning in Fig.32, we can see that for exposure time of graphene to O_2 plasma, beyond 10sec, the value of the contact resistance increases, probably due to the degradation of graphene. Finally, we

have to mention that the enormous errors of the mean values (standard deviation) are ascribed to the large dispersion of our measurements. This effect is commonly observed among all groups working on graphene.

- ***Subsection 2: R_{sheet} versus O_2 plasma treatment time without thermal annealing***

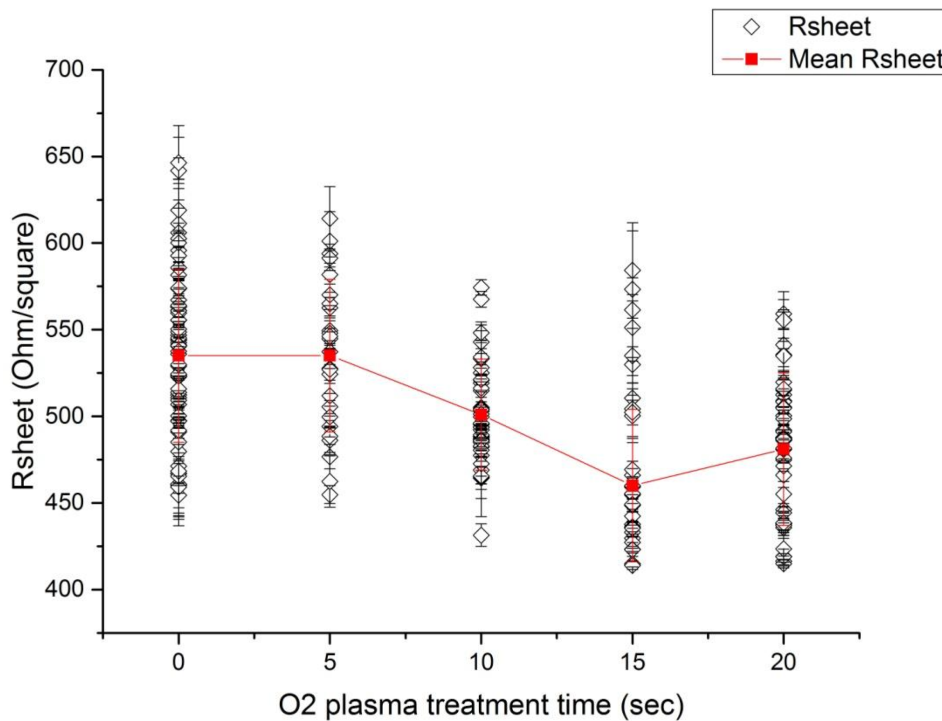

Fig.33: *Sheet resistance R_{sheet} and mean sheet resistance Mean R_{sheet} (Ω/square) versus O_2 plasma treatment time (sec) for all TLM test samples (Sample1, Sample2, Sample3, Sample 4, Sample5). 0sec of O_2 plasma treatment time is referred to the section of our samples without O_2 plasma treatment.*

The above figure, Fig.33, illustrates how the sheet resistance R_{sheet} changes with the O_2 plasma treatment. As we observe, the minimum value of the mean R_{sheet} (460±44) Ω/□ was achieved for 15sec O_2 plasma treatment time, while the maximum value appears in the case of no treatment (535±50) Ω/□. In addition as the theory requires, the sheet resistance of graphene did not change significantly for short times of plasma treatment. Any change probably comes from doping of graphene near the contacts.

- ***Subsection 3: R_c versus thermal annealing type***

In Subsection 1, we found that the optimum O_2 plasma treatment time for contact resistance was 10sec without any thermal annealing treatment. In this subsection our purpose was to investigate the effect of different thermal annealing types to contact resistance.

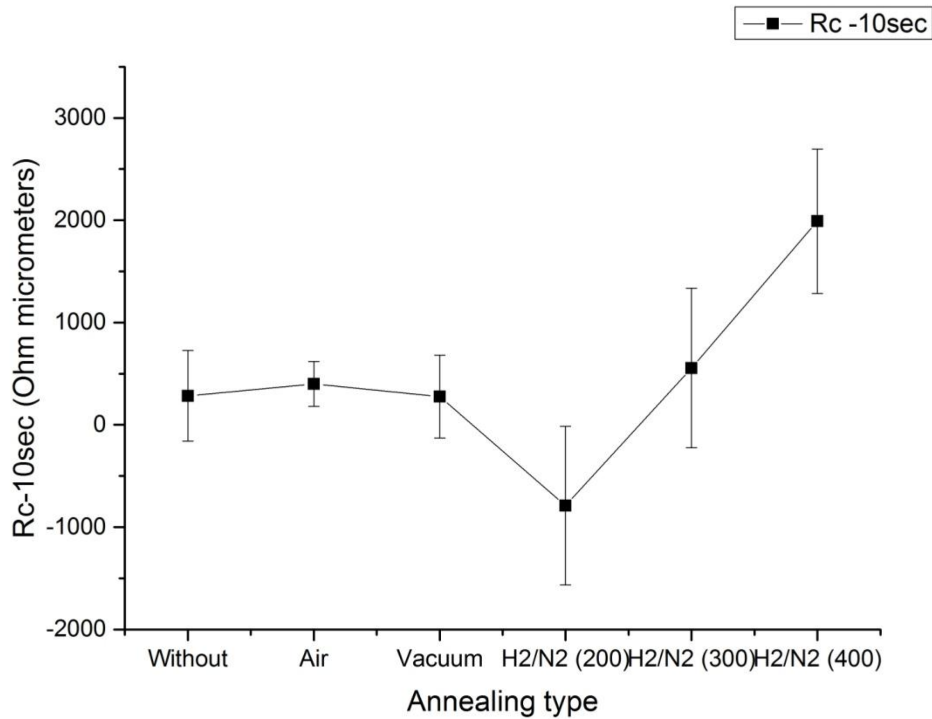

Fig.34: *Mean R_c for 10sec O_2 plasma treatment time versus all thermal annealing types (in air, in vacuum, in H_2/N_2 at 200^oC, 300^oC and 400^oC) respectively.*

In the above figure, Fig.34, we see how the contact resistance for samples exposed to 10sec O_2 plasma treatment time changes with the thermal annealing type. We chose to plot the values of mean contact resistance that were achieved for 10sec O_2 plasma treatment time because at this particular O_2 plasma treatment time we had the lowest contact resistance. Indicatively we quote the results of our measurements for each thermal annealing type at the end of this subsection in Fig.35 in order to justify this choice. So, as we observe in Fig.34 without any thermal annealing the value of the contact resistance was (584±845) Ω μm while this value decreased to (400±220) Ω μm after thermal annealing in air at 300 ^oC for 10minutes. After thermal annealing in vacuum at 300 ^oC for 10minutes the contact resistance appeared to

decrease to a value of (276±405). In the case of thermal annealing in a forming gas (H_2/N_2) atmosphere the trend of the contact resistance values was different and an increase was observed as the temperature of the annealing increased from 200 ^oC to 300 ^oC and from 300 ^oC to 400 ^oC respectively. For forming gas annealing at 200 ^oC the mean value of the contact resistance appears to be negative, this effect is known and probably indicates a doping effect from the contatcs [62].

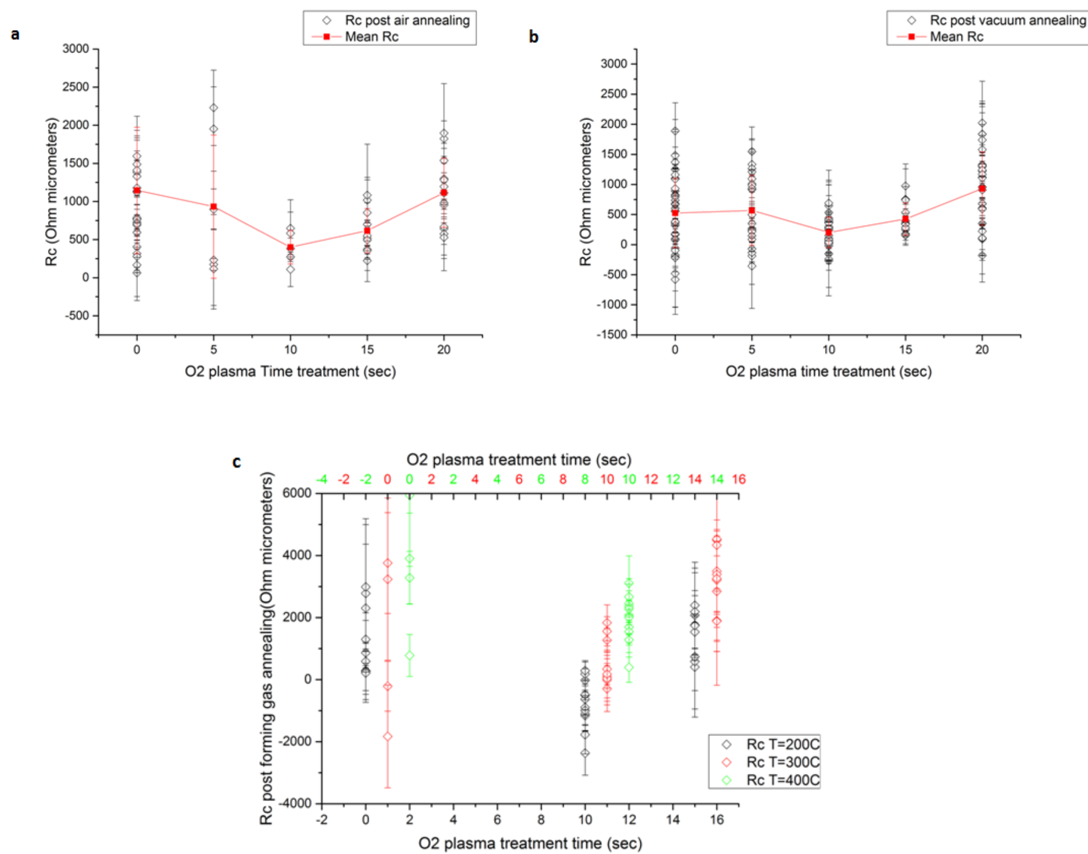

Fig.35: *35a: Contact resistance Rc for post-air annealing versus* O_2 *plasma treatment time, 35b: Contact resistance for post-vacuum annealing versus* O_2 *plasma treatment time, 35c: Contact resistance for post-forming gas annealing at 200* ^oC*, 300* ^oC *and 400* ^oC *versus* O_2 *plasma treatment time.*

In Fig.35, we see that our choice about the optimum O_2 plasma treatment time is justified, since in all cases the lowest value of contact resistance was achieved for 10sec plasma treatment.

- ***Subsection 4: R_{sheet} versus thermal annealing type***

In Subsection 2, we found that the optimum O_2 plasma treatment time for the contact resistance was 10sec with no thermal annealing treatment and in Subsection 3 we found that its lowest value obtained for 10sec O_2 plasma treatment and after forming gas annealing at T=200^oC. In this subsection our purpose was to investigate the effect of different thermal annealing types to the values of sheet resistance for samples exposed to 10sec O_2 plasma treatment.

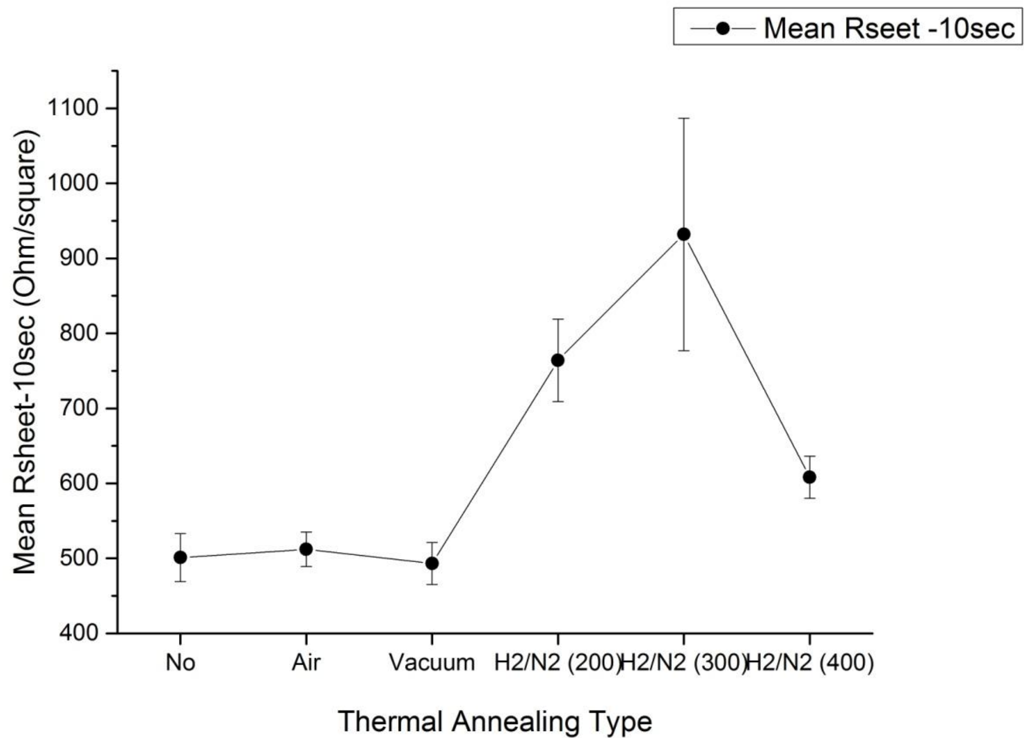

Fig.36: *Mean R_{sheet} for 10sec O_2 plasma treatment time versus all thermal annealing types (in air, in vacuum, in H_2/N_2 at 200^oC, 300^oC and 400^oC) respectively.*

In the above figure, Fig.36, we see how the sheet resistance for samples exposed to 10sec O_2 plasma treatment time changes with the thermal annealing type. We chose to plot the values of mean sheet resistance that were achieved for 10sec O_2 plasma treatment time because at this particular O_2 plasma treatment time we had the lowest contact resistance. Indicatively we quote the results of our measurements for each thermal annealing type at the end of this subsection in Fig.37. So, as we observe in Fig.36 with no thermal annealing the value of the sheet resistance was (501±32) Ω/□ while this value increased to (512±23) Ω/□ after thermal annealing in air at 300

^oC for 10minutes. After thermal annealing in vacuum at 300 ^oC for 10minutes the sheet resistance appears to decrease to (493±28) Ω/□. In the case of thermal annealing in a forming gas (H_2/N_2) atmosphere the sheet resistance values increased as the temperature of the annealing increased from 200 ^oC to 400 ^oC. Its highest value, (932±155) Ω/□, obtained for samples exposed to forming gas annealing at 300°C for 10 min.

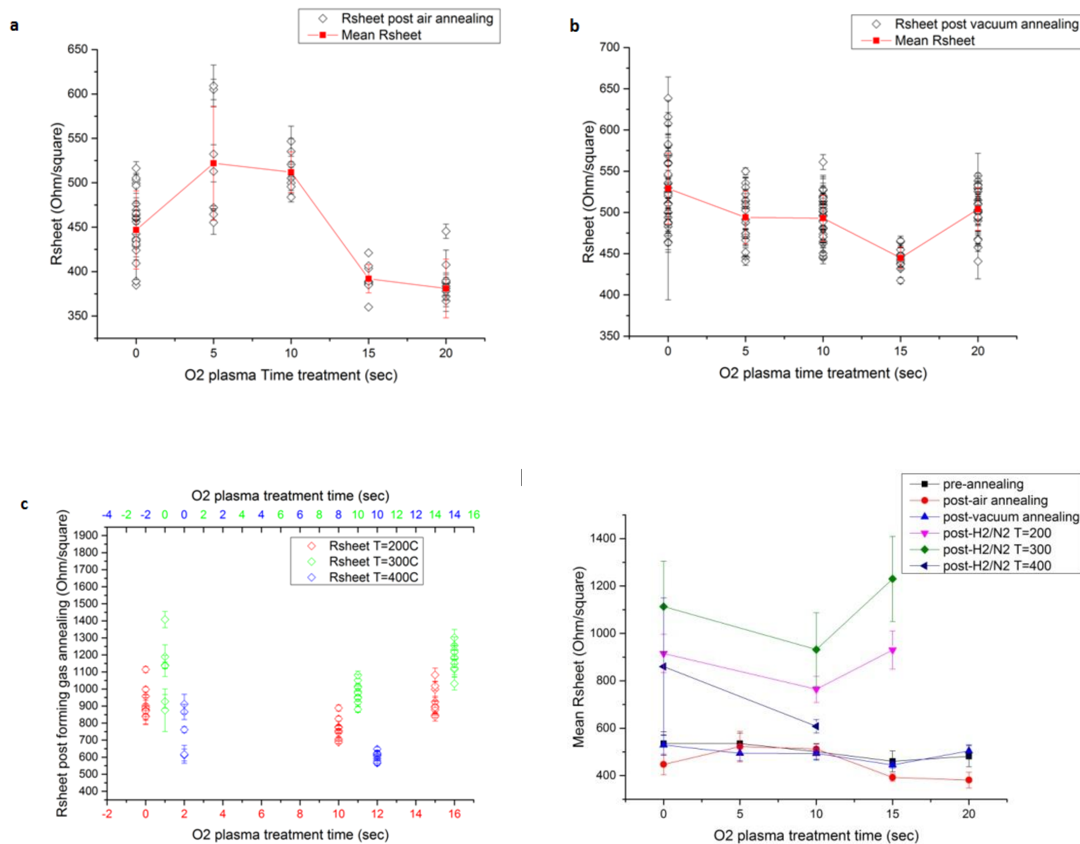

Fig.37: *37a: Sheet resistance Rsheet for post-air annealing versus O_2 plasma treatment time, 37b: Sheet resistance for post-vacuum annealing versus O_2 plasma treatment time, 37c: Sheet resistance for post-forming gas annealing at 200 ^oC, 300 ^oC and 400 ^oC versus O_2 plasma treatment time., 37d:Mean Rsheet for all the thermal annealing types versus O_2 plasma treatment time.*

6.1.4 Conclusions

As we mentioned at the beginning of this part, our purpose was to study the effect of O_2 plasma treatment mainly on contact resistance and additionally on sheet resistance. We say 'additionally' because we ideally expected that significant changes occurred in contact resistance since the treatment was performed prior to metal deposition in the contact area while the rest of the channel region remained protected under the resist during the plasma treatment. In chapter 2.10.2.2 we discussed in detail the principles of plasma treatment as a cleaning method for removing organic contaminations. O_2 plasma treatment prepares surfaces for intimate contact between metal and graphene. Residue contaminants on the sample surface will be removed in two ways. First, the high energy ions mechanically break up molecular bonds of the surface molecules and effectively blast the molecular particles off the sample surface. Second, oxygen in the plasma readily reacts with the surface contaminants, breaking them up into smaller and more volatile pieces which easily evaporate off the surface [27].

In our results the effectiveness of O_2 plasma treatment was imprinted by the trend of contact resistance values versus treatment time. As we observe in Fig.32, the contact resistance, R_c, changed versus the O_2 plasma treatment time and more specifically as the treatment time increased the value of contact resistance decreased. For 10 seconds O_2 plasma treatment time the value of the contact resistance achieved the minimum value of (284±444) Ωμm indicating the reduction of the photoresist residues. Beyond that time the value of the contact resistance increased and the degradation of the graphene may explain that finding. Except for the changes of the contact resistance with respect to the O_2 plasma treatment time, the contact resistance changes according to the thermal annealing type. The contact resistance after thermal annealing in air atmosphere is higher than that after thermal annealing in vacuum atmosphere. This trend is probably ascribed to the oxidation that takes places during the thermal annealing in air atmosphere leading in higher contact resistance. A clear increasing trend of contact resistance is observed as the temperature of the forming gas annealing is increased. In the case of the 200 ^oC the contact resistance becomes negative. This apparent negative contact resistance is probably due to the doping effect which may be more substantial than the actual contact resistance [62].

In the case of sheet resistance, our results show that the minimum value was achieved for 15 seconds plasma treatment. Although, the sheet resistance didn't change significantly for 0 and 5 seconds plasma treatment an important decrease was observed for 10 and 15 seconds while beyond 15 seconds the sheet resistance increased. At this point, we have to notice that since the treatment was performed at the region where the metal was to be deposited any change in the sheet resistance was mainly attributed to the region of graphene below the contacts. Concerning the thermal annealing type small deviations of the sheet resistance are observed between no thermal annealing and thermal annealing in air and vacuum atmospheres while for the case of forming gas annealing the sheet resistance starts to increase exhibiting its maximum value at $300^{o}C$ of forming gas annealing. Finally, we must be careful with the sheet resistance interpretation. A low sheet resistance does not mean necessary that is the desired one. If we assume that the mobility of carriers remains constant after the O_2 plasma treatment and any of the thermal annealing types, we could say that higher values of sheet resistance probably imply more effective cleaning process.

6.2 Dielectrics (Part II)

In this part we investigate the electrical properties of HfO_2 dielectric films deposited through e-gun evaporation and atomic layer deposition method. In order to evaluate the breakdown voltage (V_{br}) and the leakage current (I_{leak}) we measured 7 different metal insulator metal (MIM) test devices, 4 and 3 for the above deposition techniques respectively. In the following section we give a description about the sample features.

6.2.1 Sample preparation

The MIM capacitors with HfO_2 dielectric films were fabricated on Si substrates. A 10-Å-thick Cr layer was deposited via thermal evaporation in order to achieve better adhesion between the bottom electrode of the MIM structure and the silicon substrate. After the deposition of the thin film of Cr, a 50-nm-thick Pt bottom electrode layer was deposited via e-gun evaporation. The next step was the deposition of the dielectric film. So, four samples were fabricated with e-gun evaporated HfO_2 with thicknesses of 10nm, 20nm, 80nm and 200nm respectively and three samples with atomic layer deposited HfO_2 with thicknesses[1] of 5nm, 10nm and 15nm respectively. Following the dielectric deposition, the same thickness Pt (50nm) was deposited as a top electrode. Finally, Pt electrodes were patterned using optical lithography lift-off technique and a number of MIM capacitors in different sizes were formed. The typical structure of a MIM capacitor and the top electrode diameters of the final form of the test devices are summarized in the following figure, Fig.1, while the samples with the corresponding deposition method and dielectric thicknesses are introduced in the table, Table.1.

Fig.38: *Schematic illustration of the MIM test devices. a) the typical structure of a MIM capacitor, b)the final form of the test device, with different size MIM capacitors .One period of each sample consists of four different in size capacitors. The top electrode of each different capacitor has a diameter of 226μm, 176μm, 126μm and 46μm respectively.*

Table 5: *In the following table the samples with their characteristics are presented.*

Sample	HfO_2 thickness (nm)	Deposition technique
Sample 1	*10*	*e-gun evaporation*
Sample 2	*20*	*e-gun evaporation*
Sample 3	*80*	*e-gun evaporation*
Sample 4	*200*	*e-gun evaporation*
Sample 5	*7*	*e-gun evaporation +ALD*
Sample 6	*12*	*e-gun evaporation +ALD*
Sample 7	*17*	*e-gun evaporation +ALD*

[1]The total thickness of the Sample 5, Sample 6, and Sample 7 comes from:
Sample 5: 2nm e-gun evaporated HfO_2 + 5nm atomic layer deposited HfO_2.
Sample 6: 2nm e-gun evaporated HfO_2 + 10nm atomic layer deposited HfO_2.
Sample 7: 2nm e-gun evaporated HfO_2 +15nm atomic layer deposited HfO_2.

The samples with e-gun evaporated HfO_2 were fabricated in our laboratory, while the atomic layer deposited HfO_2 were fabricated in Cambridge.

6.2.2 Data analysis

The breakdown voltage and leakage current were extracted through I-V measurements. Each of our samples was located on a probe station, as is shown in the following figure, Fig. 2. Our data were collected by using a semiconductor parameter analyzer (Keithley 2612), in ambient conditions.

Fig.39: *Probe station and semiconductor parameter analyzer (Keithley 2612) which are used for the measurements conduct.*

For all the I-V measurements, the bottom electrode remained grounded while the bias was applied to the top metal electrode. Thus, for each capacitor we applied voltage and we measured the corresponding current. In the following figure, Fig.40, we introduce the J-V characteristic of the sample, Sample 5; Period:1AL126up, as an example for better understanding of our analysis.

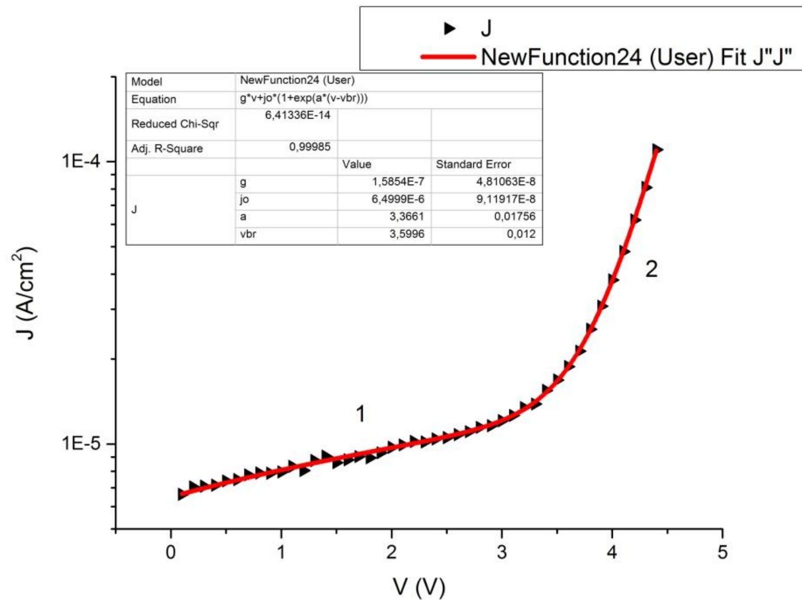

Fig.40: *J-V characteristic. Current density (J) against the applied voltage (V). The data belong to sample, Sample5, Period:1AL126up.*

In the above figure, Fig.40, two distinct regions can be seen. In the first region which is denoted with the number 1 a linear relation between the current density and the applied voltage is observed while beyond a specific value of voltage the relation becomes exponential, region 2. The region 1 corresponds to the regular operation of the capacitor and the specific value of the voltage where the exponential behavior is observed indicates the onset of the breakdown event. The slope in the linear part of the J-V curve indicates the leakage current of the capacitor and any possible deviation of the linearity implies that more than one conduction mechanisms contribute to the leakage current. To extract the breakdown voltage (V_{br}) and the leakage current density or the leakage current (J or I_{leak}) a suitable fitting is required. The equation that we used to fit our measurements is a combination of a linear and an exponential part. The linear part corresponds to the region 1 and the exponential part to the region 2, respectively.

Fitting equation:

$$J(V) = g * V + J_o[1 + \exp\big(a(V - V_{br})\big)$$

where J is the current density (current per unit capacitor area), g is the slope of the linear part and represents the conductivity, the voltage independent term, J_o, is the intercept of the linear part, a is a parameter with units of 1/V and represents how fast the phenomenon of breakdown propagates and finally V_{br} is the breakdown voltage.

At this point we have to mention how we determine the value of the leakage current. First, it is obvious that the leakage current appears in the region 1, the region of the regular operation of the capacitor. Thus the leakage current comes from the linear part of the fitting equation. Even though, in the literature, the leakage current is defined at a specific value of applied voltage, in our analysis since the scope of this part is not the study of a MIM device itself but the investigation of how the breakdown voltage and the leakage current change with the deposition technique and the dielectric thickness, the leakage current is determined by the intercept of the linear part of the fitting equation J_o. This choice is based on the fact that for biases smaller than the breakdown voltage where we refer in the region of the regular operation of the capacitor the intercept J_o dominates over the other terms such as the slope of linear part and the exponential part. Therefore, taking into account all the aforementioned the breakdown voltage for the J-V characteristic of the Fig.40, is V_{br}=(3.60±0.01)V and the leakage current density is J_{leak}=(6.50e-6±9.12e-8)Acm^{-2} or the leakage current is I_{leak}=(8.10e-10±1.14e-11)A.

6.2.3 Results and discussion

In this section the results of our measurements are presented and discussed. The structure of this section will be as follows:

Subsection 1: Breakdown voltage and leakage current for e-gun evaporated HfO_2
Subsection 2: Breakdown voltage and leakage current for atomic layer deposited HfO_2
Subsection 3: Comparison between the e-gun evaporated and atomic layer deposited HfO_2
Subsection 4: Further investigation of the more reliable samples,

where in the two first subsections the breakdown voltage and the leakage current for e-gun evaporated and atomic layer deposited HfO_2 respectively are presented, in the third subsection a comparison between these two deposition methods takes place, and in the last subsection since the more advantageous deposition method which provides better dielectric film quality has been defined a further investigation in the electrical properties of these samples with the highest dielectric quality is conducted.

- ***Subsection 1: Breakdown voltage and leakage current for e-gun evaporated HfO_2.***

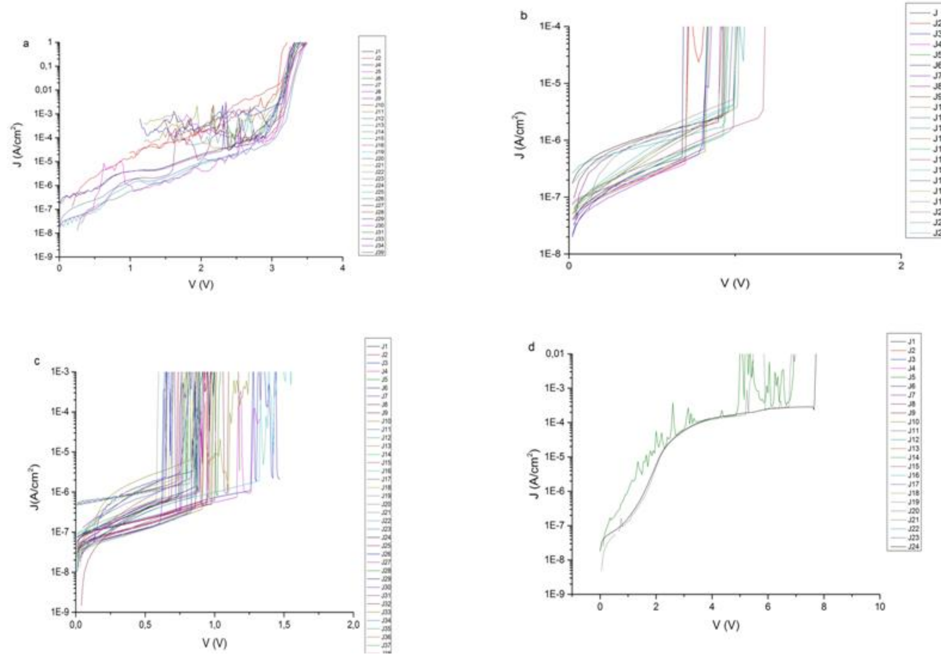

Fig.41: *J-V characteristics of samples with e-gun evaporated HfO_2. a) Sample 1 with 10nm HfO_2, b) Sample 2 with 20nm HfO_2, c) Sample 3 with 80nm HfO_2 , and d) Sample 4 with 200nm HfO2.*

In the above figure, Fig.41, the J-V characteristics of the samples with e-gun evaporated HfO_2 are illustrated. As we observe the breakdown voltage and the leakage current density for the sample with 10-nm thick HfO_2 were (2.90±0.60)V and (1.06e-6±1.02e-6)A/cm^2, respectively. For the samples with 20-nm and 80-nm thick HfO_2 the values of the breakdown voltage were (0.90±0.10)V and (0.83±0.17)V while the corresponding leakage currents were (1.62e-7±1.02e-7)A/cm^2 and (1.32e-7±1.04e-7)A/cm^2. Finally, the breakdown voltage and the leakage current density for the sample with 200-nm thick HfO_2 were (6.30±1.32)V and (1.12e-7±8.40e-8)A/cm^2, respectively. The results of our measurements are summarized in the following table, Table 6.

Table 6: *In the above table the results of the samples with e-gun evaporated HfO_2 are summarized.*

HfO_2 thickness (nm)	V_{br}(V)	J_{leak}(A/cm^2)
10	(2.90±0.60)	(1.06e-6±1.02e-6)
20	(0.90±0.10)	(1.62e-7±1.02e-7)
80	(0.83±0.17)	(1.32e-7±1.04e-7)
200	(6.30±1.32)	(1.12e-7±8.40e-8)

- ***Subsection 2: Breakdown voltage and leakage current for atomic layer deposited HfO_2.***

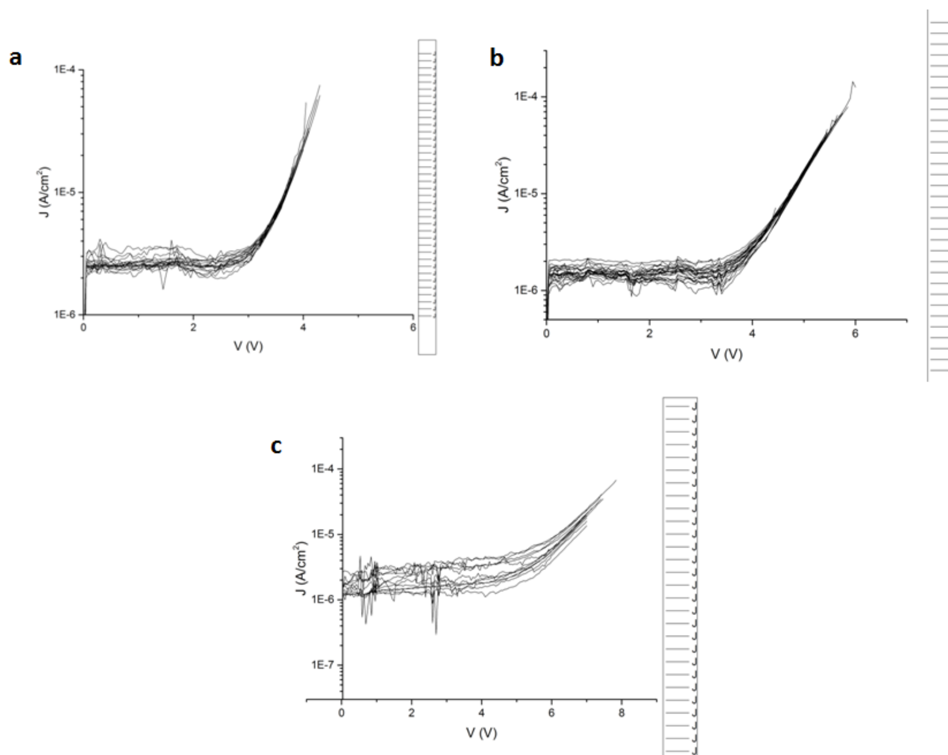

Fig.42: *J-V characteristics of samples with mainly atomic layer deposited HfO_2. a) Sample 5 with 7nm HfO_2, b) Sample 6 with 12nm HfO_2, and c) Sample 7 with 17nm HfO_2.*

In the above figure, Fig.42, the J-V characteristics of the samples with mainly atomic layer deposited HfO_2 are illustrated. As we observe the breakdown voltage and the leakage current density for the sample with 7-nm thick HfO_2 were (3.20±0.40)V

and (4.15e-6±8.80e-7)A/cm^2, respectively. For the samples with 12-nm and 17-nm thick HfO_2 the values of the breakdown voltage were (4.50±0.50)V and (5.70±0.40)V while the corresponding leakage currents were (1.80e-6±5.80e-7)A/cm^2 and (1.40e-6±8.70e-8)A/cm^2. The results of our measurements are summarized in the following table, Table 7.

Table 7: *In the following table the results of the samples with mainly atomic layer deposited HfO_2 are summarized.*

HfO_2 thickness (nm)	V_{br}(V)	J_{leak}(A/cm^2)
7	(3.20±0.40)	(4.15e-6±8.80e-7)
12	(4.50±0.50)	(1.80e-6±5.80e-7)
17	(5.70±0.40)	(1.40e-7±8.70e-8)

- ***Subsection 3: Comparison between the e-gun evaporated and atomic layer deposited HfO_2.***

In this subsection, Subsection 3, a comparison between the e-gun evaporated and atomic layer deposited HfO_2 films takes place. This comparison is based on the results of the I-V measurements, as those were presented in the previous subsections, Subsection 1 and Subsection 2, respectively. In this thesis, we mainly studied two of the intrinsic electrical properties, i.e. breakdown voltage and leakage current, of HfO_2 as a function of the deposition method and its thickness in order to use it as a gate dielectric in graphene field effect transistors. Therefore, taking into account the main purpose of this study and the results of our measurements more reliable samples seem to be those with atomic layer deposited HfO_2. More specifically, the values of the breakdown voltage for the HfO_2 films that were deposited through atomic layer deposition technique, even though they were thinner than e-gun evaporated HfO_2 films, are larger, indicating that atomic layer deposition provides higher quality dielectric films which sustain stronger electric fields without losing their insulating properties. At this point we have to mention that for the samples with e-gun evaporated HfO_2 the behavior of the breakdown voltages against the dielectric thickness was not the expected one, i.e. as the dielectric thickness increases the breakdown voltage also increases. This expected trend appears for the samples with

atomic layer deposited HfO_2. Moving in the evaluation of the leakage current densities, comparing for the same thickness, the values for the ALD films were much smaller than the values of e-gun evaporated films, which is expected since the ALD layers are of better quality. Moreover in the case of the atomic layer deposited HfO_2, it is clear that the leakage current density decreases significantly as the dielectric thickness increases. The same trend is observed in the case of e-gun evaporated HfO_2 as well, but the changes in the magnitude of the leakage current densities are not so obvious. In any case both the values of the breakdown voltages and their dependency on the dielectric thickness advocate to conclude that the atomic layer deposited films are more reliable for gate applications. All the above are illustrated in the following figure, Fig.43.

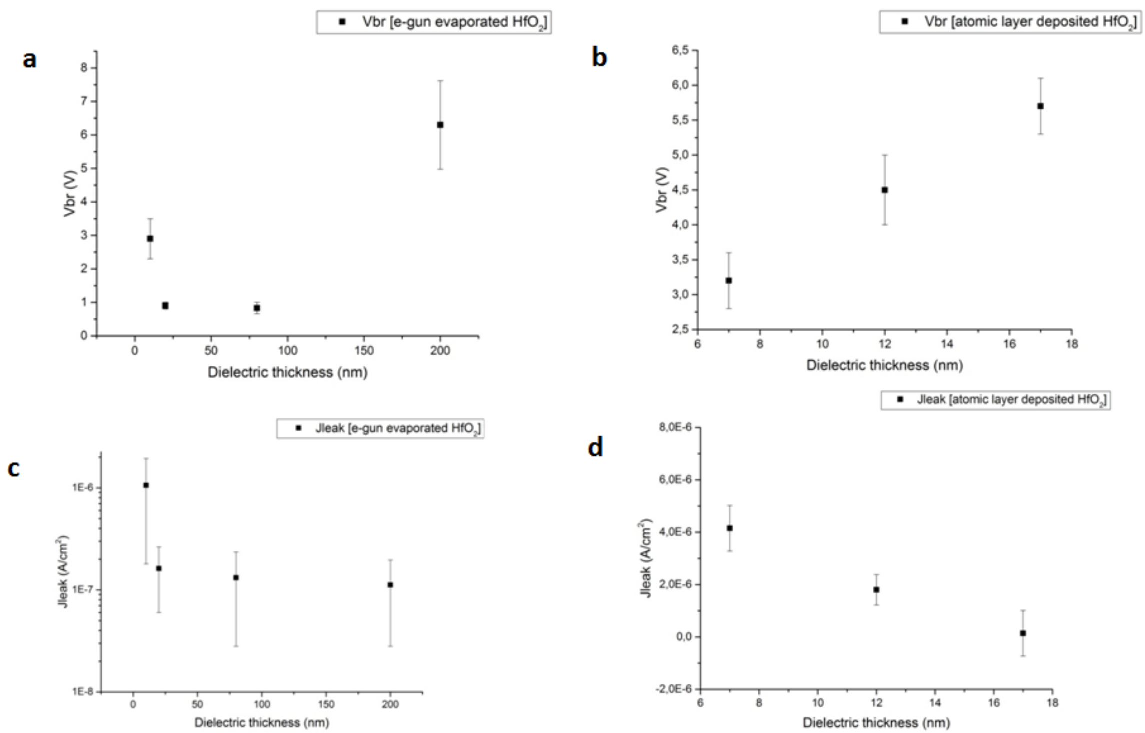

Fig.43: *Breakdown voltage and leakage current density against dielectric thickness. a) V_{br} vs dielectric thickness for e-gun evaporated HfO_2, b) V_{br} against dielectric thickness for atomic layer deposited HfO_2, c) J_{leak} against dielectric thickness for e-gun evaporated HfO_2 , and d) J_{leak} against dielectric thickness for atomic layer deposited HfO_2.*

- ***Subsection 4: Further investigation of the more reliable samples.***

Since in the previous subsections, the results of our I-V measurements were presented and a comparison between the e-gun evaporated and atomic layer deposited HfO_2 took place, in this subsection, Subsection 4, we move to a further investigation of the more reliable samples as these were identified from Subsection 3, since the samples with atomic layer deposited HfO_2 are considered as the most suitable candidates for gate dielectrics in graphene field effect transistors. This is why, at this point, we chose to further study only these samples and not also the samples with e-gun evaporated HfO_2. Do not forget, that the main goal of this part was to conclude to the more reliable dielectric films through a first order analysis, by studying their two intrinsic electrical properties such as breakdown voltage and leakage current.

The first thing that we observed during our study on these samples was the dependency of the breakdown voltage and leakage current on dielectric thickness. As the dielectric thickness increases the breakdown voltage increases as well, but the leakage current decreases. This dependency is shown in the figures, Fig.43b and Fig.43d respectively. Except for this dependency, an additional dependency was observed between the breakdown voltage and the leakage current on the capacitor size. This dependency for all the samples with atomic layer deposited HfO_2, is illustrated in the following figure, Fig.44.

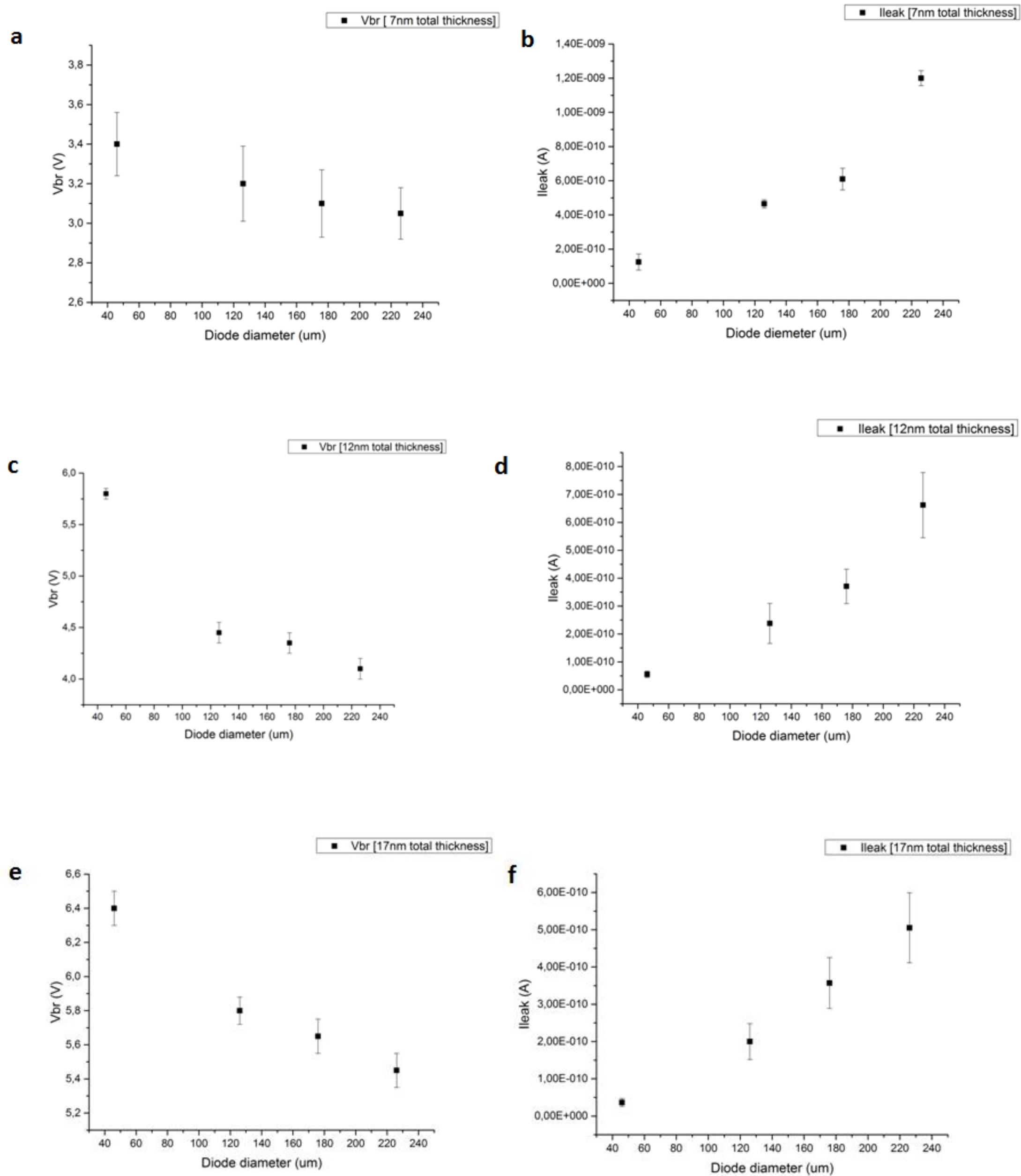

Fig.44: *Breakdown voltage and leakage current against diode diameter. a)* V_{br} *vs diode diameter for 7nm thick* HfO_2*, b)* I_{leak} *against diode diameter for 7nm thick* HfO_2*, c)* V_{br} *vs diode diameter for 12nm thick* HfO_2*, d)* I_{leak} *against diode diameter for 12nm thick* HfO_2*, e)* V_{br} *vs diode diameter for 17nm thick* HfO_2*, and f))* I_{leak} *against diode diameter for 17nm thick* HfO_2*.*

In the above figure, Fig.44, the dependency of the breakdown voltage and leakage current on the capacitor size is shown. Since, at this point, we are more interested in the qualitative meaning of the above dependency and less in the quantitative one, we just quoted the numerical results at the end of this subsection and we will attempt to explain where this dependency was attributed. Therefore,

remaining in the above figure, Fig.44, we observe that for all the samples with different dielectric thickness the dependency of the breakdown voltage and leakage current on the diode diameter which corresponds to the capacitor size is largely the same. As the capacitor size increases the breakdown voltage is reduced, while the leakage current increases. In other words, capacitors with larger top plate diameter, the breakdown effect comes earlier, while the larger in size capacitors conduct higher currents. This dependency of the breakdown voltage on the capacitor size is probably attributed to the fact that devices with larger area have higher probability of containing a breakdown site (defect). Regarding the dependency of leakage current on the capacitor size we can say that it is an expected behavior, but the noticeable point is the way that the leakage current increases against the capacitor size. It is clearly shown in the corresponding figures, Fig.44b, 44c, and 44d respectively, that there is a quadratic behavior and not a linear one, indicating that the leakage current comes from the bulk of the capacitor and not from the electrodes-plates.

Table 8: *In the following table the results of the breakdown voltage and leakage current with respect to the capacitor size are summarized.*

7nm HfO_2		
Top plate diameter	**V_{br} (V)**	**I_{leak}(A)**
46μm	(3.40±0.16)	(1.25E-10±4.70E-11)
126μm	(3.20±0.18)	(4.65E-10±2.40E-11)
176μm	(3.10±0.16)	(6.10E-10±6.38E-11)
226μm	(3.05±0.15)	(1.20E-9±4.38E-10)
12nm HfO_2		
46μm	(5.80±0.05)	(5.60E-11±1.15E-11)
126μm	(4.45±0.10)	(2.40E-11±7.20E-12)
176μm	(4.35±0.10)	(3.70E-10±6.20E-11)
226μm	(4.10±0.10)	(6.62E-10±1.20E-10)
17nm HfO_2		
46μm	(6.40±0.10)	(3.65E-11±1.10E-11)
126μm	(5.80±0.08)	(2.00E-10±4.80E-11)

176μm	(5.65±0.20)	(3.57E-10±6.83E-11)
226μm	(5.45±0.20)	(5.05E-10±9.40E-11)

6.2.4 Conclusions

In this part, Part 2, we studied the breakdown voltage and the leakage current of e-gun evaporated and atomic layer deposited HfO_2 and how these two quantities change against the dielectric thickness and the deposition method. Through our analysis we concluded that more reliable samples for gate dielectrics are considered the atomic layer deposited HfO_2, mainly due to their higher breakdown voltages indicating that sustain stronger electric fields without losing their insulating properties. Additionally, the leakage current magnitudes are acceptable for gate dielectric applications, since the upper limit of the leakage current density for gate applications is very low. The smallest value of the leakage current density was (1.40E-7±8.70e-8)A/cm^2 and this value belongs to the thickest sample among the ones deposited with atomic layer HfO_2. Concerning the behavior of the breakdown voltage and leakage current with respect to the dielectric thickness we found that as the dielectric thickness increases the breakdown voltage increases as well. Conversely as the dielectric thickness increases the leakage current decreases since any tunneling effect is inhibited with the increased dielectric thickness. The aforementioned changes of the values as a function of the dielectric thickness were clear for the samples with atomic layer deposited HfO_2. In the sequel, the qualitative results which were arisen from the more detailed investigation of the samples with atomic layer deposited HfO_2 showed a dependency between the breakdown voltage and leakage current on the capacitor size. More specifically, as the capacitor size increases the breakdown voltage is reduced, while the leakage current exhibits a quadratic increase. The fact that for larger in size capacitors the breakdown effect comes earlier is attributed to the higher probability of the devices with larger area to contain a breakdown defect while the quadratic increase of the leakage current against the capacitor size indicate that any conduction mechanism comes mainly from the bulk of the capacitor.

6.3 Graphene Field-Effect Transistors (PART III)

The final part, Part 3, of the thesis focuses on the electrical characterization of graphene field-effect transistors (GFETs) as complete devices. Therefore, we performed dc current-voltage measurements in order to obtain the output and transfer characteristics of the devices and additionally based on the above two diagrams we extracted the transconductance and the source-drain resistance which are important parameters for the electrical characterization of GFETs performance.

6.3.1 Sample preparation

In our FET devices graphene was used as the channel material. Monolayer graphene was grown on SiC in Linkoping University, while the rest of the fabrication process of the final devices was completed in our laboratory (FORTH). The first step of the sample fabrication was the definition of the source –drain pads using optical lithography technique. 50 nm Pd/ 20 nm Ni/ 50 nm Au source and drain contacts were deposited via thermal evaporation. At this point we have to mention that prior to source-drain metal deposition the graphene areas where the source-drain contacts were defined, they were treated with O_2 plasma for 10 seconds. Following this step and after the gate definition 2 nm of HfO_2 was deposited on graphene via e-gun evaporation in order to functionalize the graphene surface and then 7 nm of HfO_2 was deposited through atomic layer deposition. Finally, 30 nm Pt/ 100 nm Au top gate electrode was deposited via thermal evaporation. In the following figure, Fig.45, one period of the studied sample and devices with different number of fingers and gate width are illustrated.

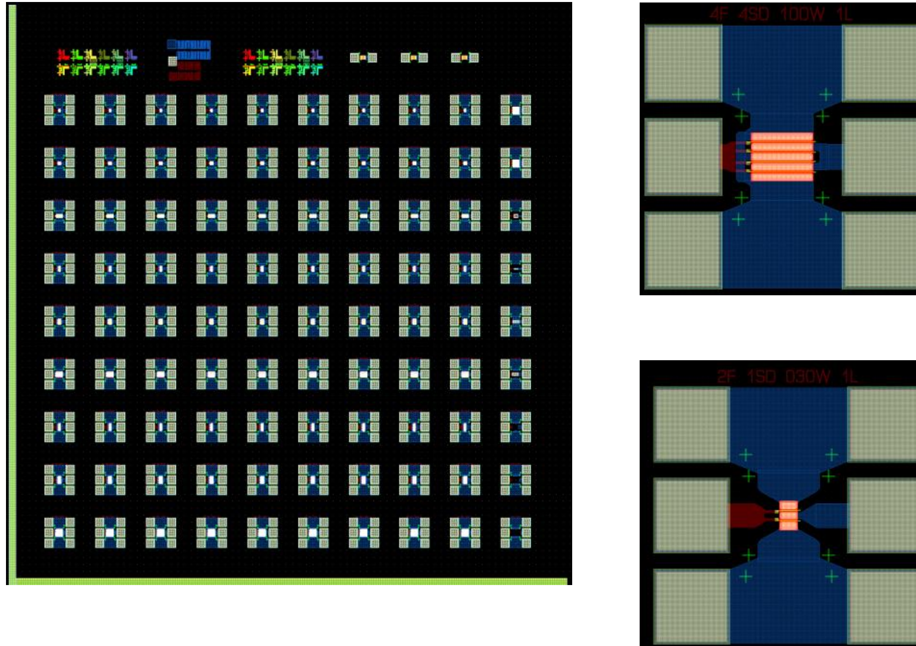

Fig.45: *Left: Image of a period of the studied sample. Right up: A GFET device with 4 fingers and 100μm gate width. Right down: A GFET device with 2 fingers and 30μm gate width.*

This period consists of 81 total GFET devices with no identical characteristics to each other, meaning that these devices are classified according to their gate width, source-drain distance, gate length, and the number of the fingers. Therefore we have devices with 30, 50, 100μm gate width, with 1, 1.5, 2.0μm source-drain distance, with 200, 400, 800nm gate length, and with 2, 4, 6 number of fingers. The above description regards the first 8 columns (from the left to right), where the GFET test devices are located. The last two columns contain open and short test devices to measure gate dielectric capacitance and metal resistivity. The sample illustrated in the Fig.45, except for the dc electrical characterization was destined for RF characterization as well.

Table 9: *Mapping of the 81 GFET test devices of the studied sample*

2F2SD30a	*2F2SD30b*	*2F2SD30b*	*2F1.5SD30a*	*2F1.5SD30b*	*2F1.5SD30c*	*2F1SD30b*	*2F1SD30c*	*2F1SD30c*
2F2SD50a	*2F2SD50b*	*2F2SD50b*	*2F1.5SD50a*	*2F1.5SD50b*	*2F1.5SD50c*	*2F1SD50b*	*2F1SD50c*	*2F1SD50c*
2F2SD100a	*2F2SD100b*	*2F2SD100b*	*2F1.5SD100a*	*2F1.5SD100b*	*2F1.5SD100c*	*2F1SD100b*	*2F1SD100c*	*2F1SD100c*
4F2SD30a	*4F2SD30b*	*4F2SD30b*	*4F1.5SD30a*	*4F1.5SD30b*	*4F1.5SD30c*	*4F1SD30b*	*4F1SD30c*	*4F1SD30c*
4F2SD50a	*4F2SD50b*	*4F2SD50b*	*4F1.5SD50a*	*4F1.5SD50b*	*4F1.5SD50c*	*4F1SD50b*	*4F1SD50c*	*4F1SD50c*
4F2SD100a	*4F2SD100b*	*4F2SD100b*	*4F1.5SD100a*	*4F1.5SD100b*	*4F1.5SD100c*	*4F1SD100b*	*4F1SD100c*	*4F1SD100c*
6F2SD30a	*6F2SD30b*	*6F2SD30b*	*6F1.5SD30a*	*6F1.5SD30bb*	*6F1.5SD30c*	*6F1SD30b*	*6F1SD30c*	*6F1SD30c*
6F2SD50a	*6F2SD50b*	*6F2SD50b*	*6F1.5SD50a*	*6F1.5SD50b*	*6F1.5SD50c*	*6F1SD50b*	*6F1SD50c*	*6F1SD50c*
6F2SD100a	*6F2SD100b*	*6F2SD100b*	*6F1.5SD100a*	*6F1.5SD100b*	*6F1.5SD100c*	*6F1SD100b*	*6F1SD100c*	*6F1SD100c*

In the above table, Table 9, the mapping of the studied sample is introduced. Each device has a characteristic name which indicates its dimensions. The nomaclature is as follows: **iFjSDka,or b,or c**, where the symbol i indicates the number of the fingers (number of gates), the symbol j indicates the source-drain distance, the symbol k indicates the gate width, and the indicators a,b and c correspond to the gate lengths of 800nm, 400nm and 200nm respectively. Thus, the name 2F2SD30a corresponds to a GFET device with 2 fingers, 2μm source-drain distance, 30μm gate width and 800nm gate length.

6.3.2 Data analysis

The output and transfer characteristics were extracted through dc I-V measurements. Our sample was located on a probe station, as it shown in the following figure, Fig. 46. Our data were collected by using a semiconductor parameter analyzer (Keithley 4200), in ambient conditions.

Fig.46: *Probe station and semiconductor parameter analyzer (Keithley 4200) which are used for the measurements conduct.*

Transfer characteristics

In order to obtain the transfer characteristics meaning the source-drain current I_{DS} as a function of the gate voltage V_G, for a constant source-drain voltage V_{DS}, we posed to the parameter semiconductor analyzer, Keithley 4200, the following parameters: the gate voltage, V_G, was taking values from -2.0V to 2.0V (voltage sweep) with step of 0.5V while the source-drain voltage, V_{DS}, remained constant (voltage biased) at 0.2V (see Fig.48a). For all the current-voltage measurements the source electrode remained grounded.

Output characteristics

In order to obtain the output characteristics meaning the source-drain current I_{DS} as a function of the source-drain voltage V_{DS}, for different gate voltages V_G, we worked based on the following parameters: the drain-source voltage, V_{DS}, changed from 0V to 3.0V (voltage sweep) with step of 0.05V while the gate voltage, V_G, was taking values from -2.0V to 2.0V (voltage step) with step of 0.5V (see Fig.48b). For all the current-voltage measurements the source electrode remained grounded.

Source-Drain Resistance

One important parameter that inform us about the carrier transport in GFETs is the source-drain resistance R_{DS} which is given by the following formula

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = R_C + R_A + R_G + R_A + R_C = 2R_C + 2R_A + R_G \quad (1) ,$$

where R_C is the contact resistance, R_A is the access resistance which corresponds to uncovered area of graphene, and R_G is the resistant that corresponds to the graphene area under the gate electrode. The above quantities are shown in the following figure, Fig.47.

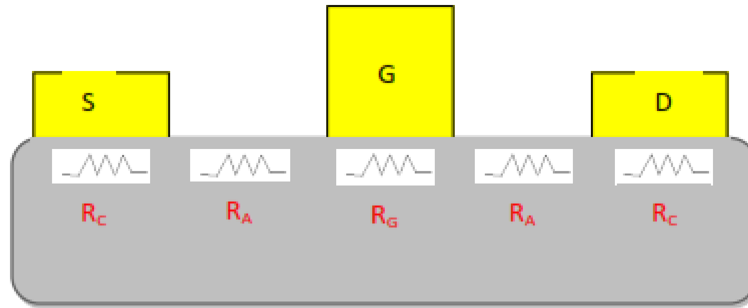

Fig.47: *Typical illustration of source-drain resistance. R_C is the contact resistance, R_A is the access resistance and R_G is the graphene resistance under the gate electrode.*

In our analysis the source-drain resistance is extracted by the output characteristics. More specifically, from the curve that corresponds to V_G=2.0V where we have the maximum source-drain current and for source-drain voltages ≤ 1.5V where the relationship between the source-drain current and source-drain voltage is linear. For each V_{DS} we measured the corresponding I_{DS}, therefore by applying the Ohm's law we calculate the source-drain resistance, $R_{SD}=V_{DS}/I_{DS}$.

Transconductance Extraction

Based on the above characteristics we are capable of extracting the transconductance. More specifically, the first derivative of the transfer characteristics gives the transconductance in the low-field regime (see Fig.48c). For the high-field transconductance our purpose was to study how it changes both with the source-drain voltage, V_{DS}, and the gate voltage, V_G (see Fig.48d). Thus for each V_{DS} we calculated

the transconductance for each pair of I-V curves which make up the graph of the output characteristics. Following we quote an example of our calculations for better understanding.

Example of high-field transconductance calculation

Table 10: *Data for transconductance calculation. The following data belong to the 2F1.5SD50 device. For the scope of this example we quote data for V_{DS}=[0,0.15]V but in our analysis we took into account data obtained for V_{DS}=[0,3]V.*

V_{DS}	$I_{DS}[V_G1]$	$I_{DS}[V_G2]$	$I_{DS}[V_G3]$	$I_{DS}[V_G4]$	$I_{DS}[V_G5]$	$I_{DS}[V_G6]$	$I_{DS}[V_G7]$	$I_{DS}[V_G8]$	$I_{DS}[V_G9]$
0	7,17E-10	1,83E-10	2,72E-10	3,85E-10	2,34E-10	3,27E-10	-4,88E-10	-6,21E-10	-2,34E-10
0,05	6,34E-04	6,12E-04	6,86E-04	7,70E-04	8,84E-04	6,10E-04	6,37E-04	8,11E-04	9,58E-04
0,1	1,27E-03	1,22E-03	1,37E-03	1,53E-03	1,77E-03	1,21E-03	1,29E-03	1,63E-03	1,93E-03
0,15	1,90E-03	1,83E-03	2,04E-03	2,29E-03	2,65E-03	1,82E-03	1,93E-03	2,45E-03	0,00289

As we can see in the above table, Table 10, in the first column we have the source-drain voltage V_{DS}(V) while in the rest columns we have the source-drain currents I_{DS}(A) which correspond to a different gate voltage V_{Gi}, where i=-2,…,2 with step=0.5. In order to calculate the transconductance, g_m, we use the following formula

$$g_m = \frac{\partial I_{DS}}{\partial V_G} | V_{DS=const.} \quad (2)$$

Therefore, for V_{DS}=0V we obtain $g_{m1} = \frac{I_{DS2} - I_{DS1}}{V_{G2} - V_{G1}} = \frac{1.83E-10 - 7.17E-10}{-1.50-(-2)} = -1.07\, S.$ Based on the last formula we calculated all the transconductance values, g(i) in S units, that are introduced in the following table, Table 11.

Table 11: *Transconductance calculated from data introduced in Table10. The following data belong to the 2F1.5SD50 device. For the scope of this example we quote data for V_{DS}=[0,0.15]V but in our analysis we took into account data obtained for V_{DS}=[0,3]V.*

V_{DS}	**g(1)**	**g(2)**	**g(3)**	**g(4)**	**g(5)**	**g(6)**	**g(7)**	**g(8)**
0	-1.07E-9	1,78E-10	2,26E-10	-3,02E-10	1,85E-10	-1,63E-9	-2,65E-10	7,74E-10
0,05	-4,46E-5	1,47E-4	1,70E-4	0,0002	-5,47E-4	5,31E-5	3,49E-4	2,93E-4
0,1	-0,0001	3,00E-4	3,20E-4	0,00048	-1,12E-3	1,60E-4	6,80E-4	6,00E-4
0,15	-0,00014	4,20E-4	5,00E-4	0,00072	-1,66E-3	2,20E-4	1,04E-3	8,80E-4

In our analysis the transconductance g_{mi} will be denoted as g(i) and its units will be mS/mm, meaning that the transconductance will be normalized on the gate width and the number of fingers. Each g(i), i=1,..,8 with step=1, corresponds to a specific pair of gate voltages. Particularly,

g(1): for 0V≤Vds≤3V and ΔV_G= -1.5-(-2)=0.5V

g(2): for 0V≤Vds≤3V and ΔV_G = -1.0-(-1.5)=0.5V

g(3): for 0V≤Vds≤3V and ΔV_G = -0.5-(-1)=0.5V

g(4): for 0V≤Vds≤3V and ΔV_G = -0.0-(-0.5)=0.5V

g(5): for 0V≤Vds≤3V and ΔV_G = 0.5-(0)=0.5V

g(6): for 0V≤Vds≤3V and ΔV_G = 1.0-(0.5)=0.5V

g(7): for 0V≤Vds≤3V and ΔV_G = 1.5-1.0=0.5V

g(8): for 0V≤Vds≤3V and ΔV_G = 2.0-1.5=0.5V.

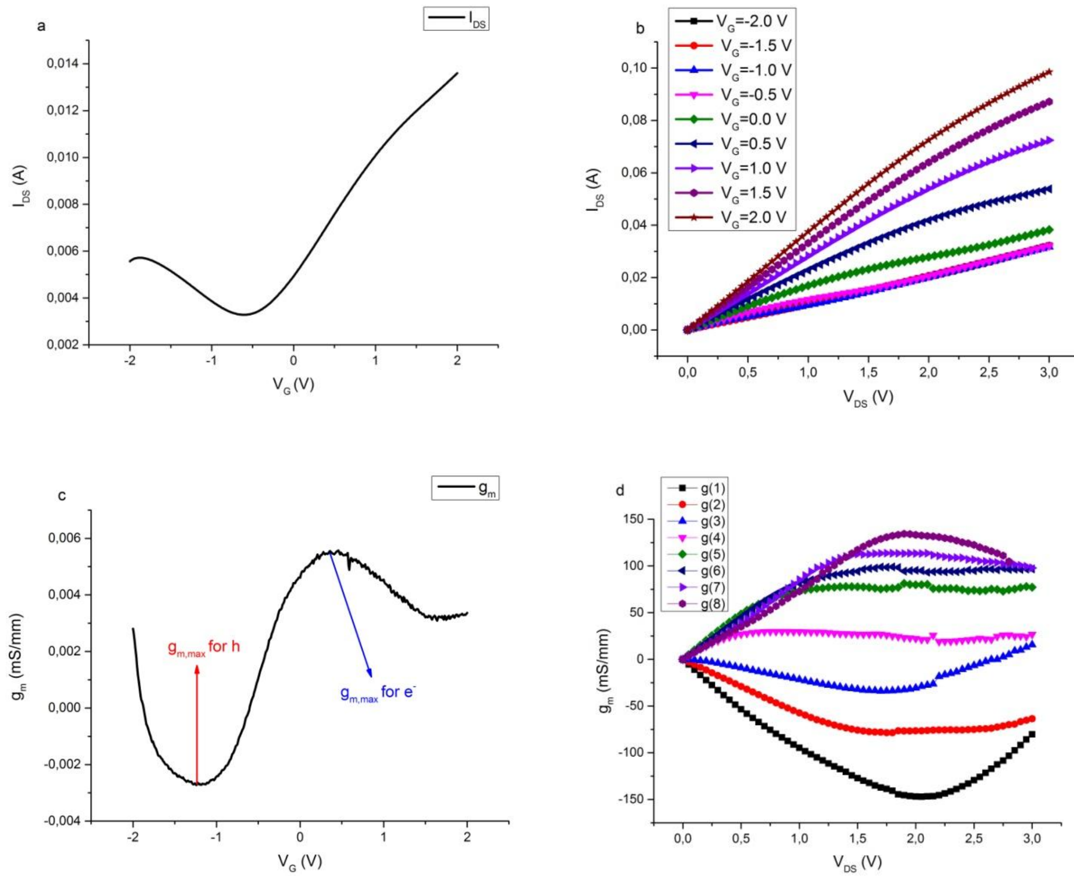

Fig.48: *a) Transfer characteristics, b) Output characteristics, c)Low-field transconductance* g_m *, and d) High-field tranconductance* g_m*. The above data belong to 6F2SD30 device.*

In the above figure, Fig.48, representative transfer characteristics, output characteristics, low-field transconductance and high-field transconductance are illustrated. In the figure, Fig.48a, we have the transfer characteristics while in the figure, Fig.48b, we have the transfer characteristics where each of the current-voltage curves corresponds to a different gate voltage. Then in the figure, Fig.48c, we have the low-field transconductance which results from the first derivative of the transfer characteristics Fig.48b, and finally in the figure, Fig.48d, the high-field transconductance is shown which is calculated in the way that is described above (example of high-field transconductance calculation).

6.3.3 Results and discussion

In this section the results of our measurements are presented and discussed. The structure of this section will be as follows:

Subsection 1: Transfer characteristics
Subsection 2: Output characteristics
Subsection 3: Source-Drain Resistance
Subsection 4: Transconductance,

where in the two first subsections the transfer and output characteristics respectively are presented, in the third subsection both the source-drain resistance and contact resistance are shown, and in the last subsection we present the results of the measured transconductance and how this parameter changes as a function of the device dimensions and the transport regime (low-field transport regime and high-field transport regime respectively).

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- ***Subsection 1: Transfer characteristics***

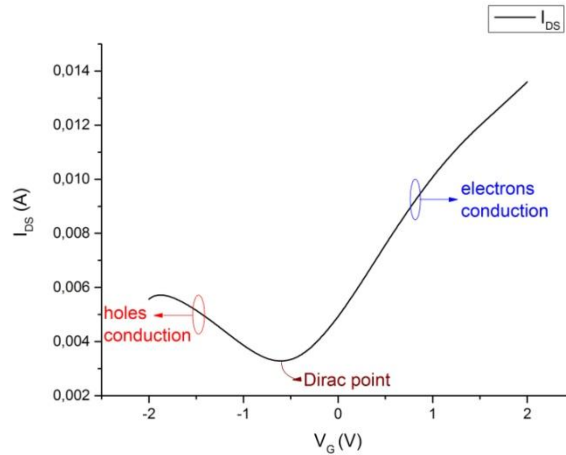

Fig.49: *Transfer characteristics of device 4F1SD100. Holes and electrons conduction branches are shown and Dirac point as well. The above figure belongs to 4F1SD100 device.*

In the above figure, Fig.49, the transfer characteristics of the 4F1SD100 device is illustrated. At this point we have to mention that we chose to quote this I_{DS}-V_G characteristic of this particular device because the gate voltage where the Dirac point is located, V_{Dirac}=-0.70V is very close to the mean value of the V_{Dirac}=(-0.72±0.02)V of all the measured devices (75 measured devices) and the shape of the I_{DS}-V_G curve is very similar to each other. So, this is a typical device of our sample and thus referring to it, it will be as we refer to the total sample. Returning to the position of the Dirac point, we observe that it is not located at V_G=0V as the theory requires but it is shifted leftward. This shift reflects the influence (doping) of the top gate, the gate dielectric, the impurities that are present in the graphene channel and defects such as electron-hole puddles that come from the substrate. Except for the shift of the Dirac point the shape of the I_{DS}-V_G although it represents the ambipolar behavior of such devices is not the theoretically expected one, but a clear asymmetry between the hole and electron conduction branches is observed. More specifically, the holes contribution to conduction is much smaller than that of electrons contribution. Far from the Dirac point the maximum current value at V_G=-2V (maximum current is ascribed to holes conduction, I_{DSh}=~0.006A) is less than the maximum current value at V_G=+2V (maximum current is ascribed to electrons conductions, I_{DSe}=~0.014A). This inconsistency or asymmetry is possible due to the differently doped graphene

areas across the source-drain length of graphene field-effect transistor. Particularly, both source and drain contacts are made of Pd which slightly p-dopes the graphene under the source and drain pads. But, prior to Pd deposition we have performed O_2 plasma treatment in order to remove any contaminations come from the nanofabrication process, so eventually the graphene under the source and drain pads is n-type doped. Thus, by applying a $V_G<V_{Dirac}$ the rest area of graphene within the source-drain distance is p-doped and as a consequence we have the formation of a "n-p-n" junction. This junction formation gives rise to resistance and results in the reduction of source-drain current which is attributed to the holes transport. On the other hand, by applying a $V_G>V_{Dirac}$ we have a uniform doping of graphene areas within the source-drain length, i.e. graphene areas under the source-drain pads are n-type doped similar to the rest graphene areas of the source-drain length. So as a consequence, non additional restrictions present in electrons transport leading to higher source-drain current values. Finally, far from the Dirac point, for example at $V_G>1V$ a deviation of perfect linearity between I_{DS} and V_G is observed, implying that due to ultra high carrier densities the interaction between the carriers is essential and affects the performance of the device, since this interaction between the carriers reduces the mobility of carriers and as a result the conductance is reduced as well.

- ***Subsection 2: Output characteristics***

In this subsection, Subsection 2, we are going to present some of the output characteristics of the measured devices, and a discussion of these results and how they change as a function of the gate width, source-drain distance, and the number of fingers will take place. Before quoting our results we have to say that in all cases we observed that the source-drain current (I_{DS}) was increasing as the source-drain voltage (V_{DS}) increased. Except for the dependency on the source-drain voltage the source-drain current also depended on the gate voltage (V_G). Particularly, for $V_G>0$ it was clear that higher gate biases were resulting in higher source-drain currents. In the case of negative gate biases $V_G<0$ this effect and the influence of the gate on the modulation of the channel conductivity were not so obvious.

I_{DS}-V_{DS} characteristics as a function of the gate width

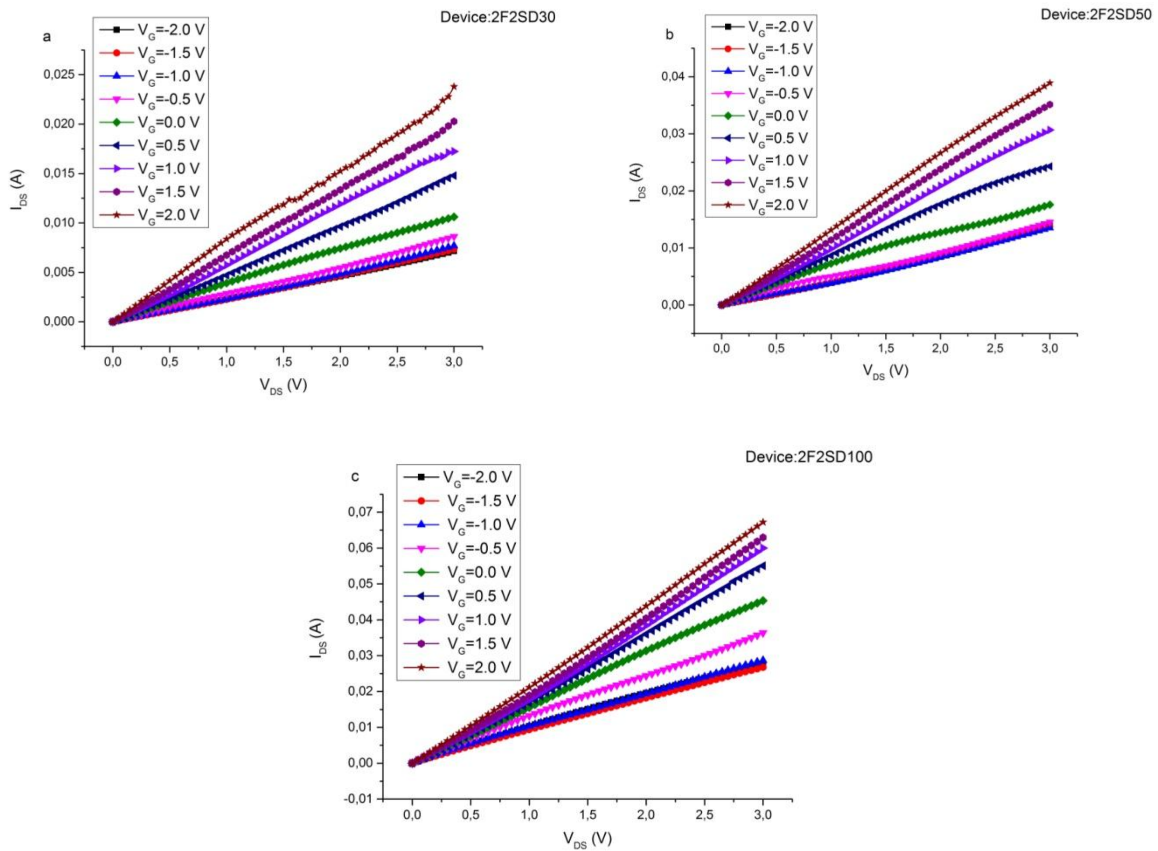

Fig.50: *Output characteristics of a) 2F2SD30, b) 2F2SD50, and c) 2F2SD100 devices. All the above devices have the same number of fingers and source-drain distance, but different gate width 30, 50, and 100μm respectively.*

In the above figure, Fig.50, the output characteristics of the devices with the same number of fingers 2, same source-drain distance of 2μm, but with different gate widths of 30, 50, and 100μm respectively are illustrated. As we can observe larger devices conduct higher currents. More specifically, the source-drain current for gate width of 30μm was about 0.025A (Fig.50a), for width of 50μm was about 0.04A (Fig.50b) and for width of 100μm the source-drain current reached the value of about 0.07A (Fig.50c). This is what we expected from theory.

I_{DS}-V_{DS} characteristics as a function of the source-drain distance

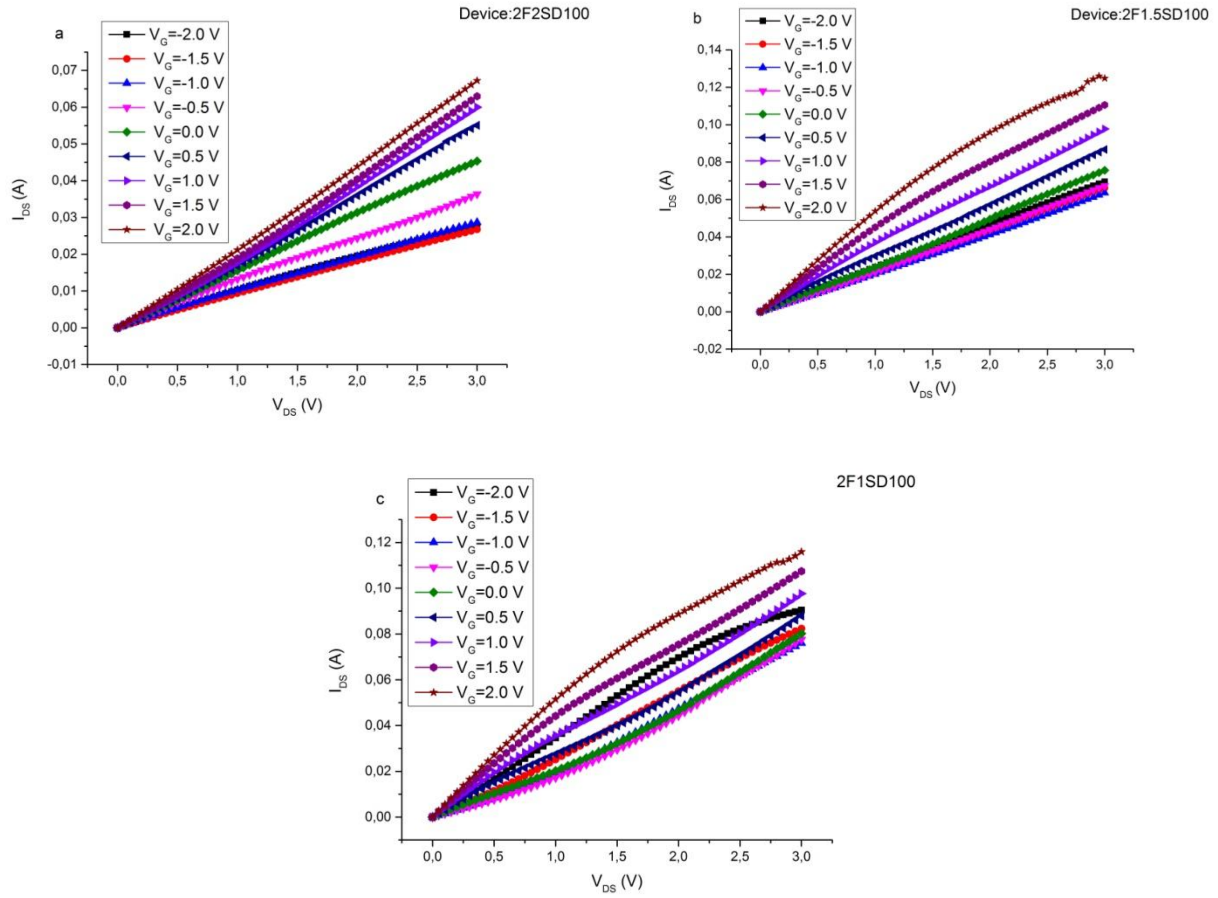

Fig.51: *Output characteristics of a) 2F2SD100, b) 2F1.5SD100, and c) 2F1SD100 devices. All the above devices have the same number of fingers and gate width, but different source-drain distances of 2, 1.5, and 1μm respectively.*

In the above figure, Fig.51, the output characteristics of the devices with the same number of fingers 2, same gate width of 100μm, but with different source-drain distances of 2, 1.5, and 1μm respectively are illustrated. The first point that we have to mention is that contrary to what we expected, the source-drain current did not increase as the source-drain distance decreases, given that for longer source-drain distances the resistance is expected to be higher. More specifically, the source-drain current for source-drain distance of 2μm was about 0.07A (Fig.51a), then when the source-drain distance became 1.5μm the source-drain current was about 0.14A (Fig.51b), and for the smallest source-drain distance, 1μm, the source-drain current

decreased to 0.12A (Fig.51c). This can be explained taking into account that for low source-drain distance the resistance is dominated by the contact resistance and not the channel resistance. Except for the source-drain current scaling with the source-drain distance, another issue that appeared in the above characteristics was that for shorter source-drain distances (1.5μm and 1μm) a pseudo-saturation region was formed possibly indicating that different transport regime or in other words different scattering phenomena take place in shorter devices.

I_{DS}-V_{DS} characteristics as a function of the fingers number

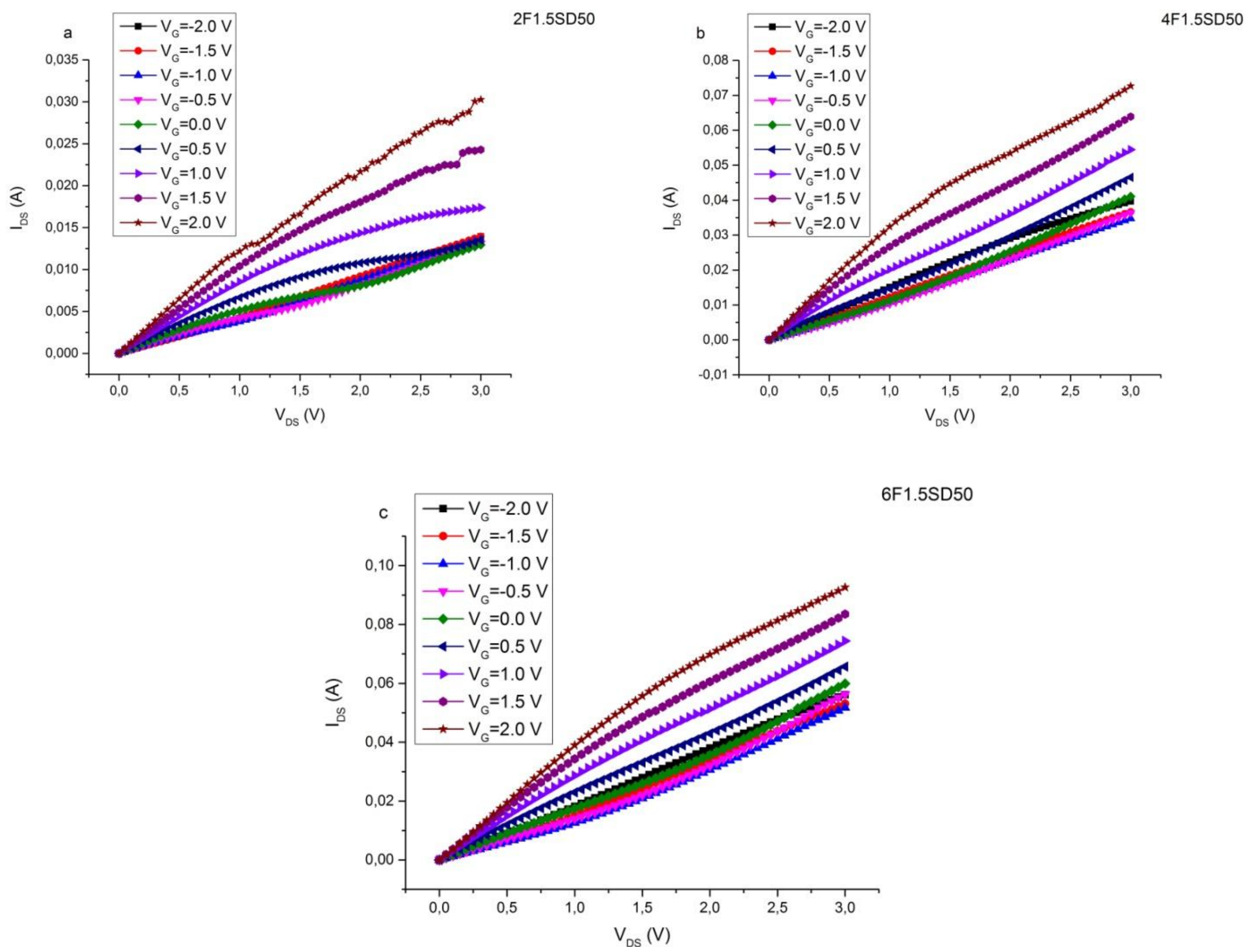

Fig.52: *Output characteristics of a) 2F1.5SD50, b) 4F1.5SD50, and c) 6F1SD50 devices. All the above devices have the same gate width and source-drain distance, but different number of fingers 2, 4, and 6 respectively.*

In the above figure, Fig.52, the output characteristics of the devices with the same gate width of 50μm, same source-distance of 1.5μm, but with different number of fingers 2, 4, and 6 respectively are illustrated. It is obvious that as the number of

finger increases the maximum value of source-drain current also increases. More specifically, in the case of 2 fingers the maximum source-drain current was about 0.035A (Fig.52a), following in the case of 4 fingers the source-drain current reached the value of about 0.08A (Fig.52b) and finally for 6 fingers the maximum source-drain current was about 0.10A (Fig.52c). This enhanced response of the devices (from the source-drain current point of view) with the larger number of fingers has similar explanation with the devices with larger width that conduct larger currents. In general, for higher source-drain currents we prefer devices (GFETs) with large gate width but with shorter gate length. Shorter gate lengths ensure the minimization of the gate resistance of the gate electrode. Thus, keeping the same gate width with increasing the number of gates in the same device geometry we can achieve higher source-drain currents.

- ***Subsection 3: Source-Drain Resistance***

In this subsection, Subsection 3, we introduce the source-drain resistance and how it changes as a function of the source-drain distance.

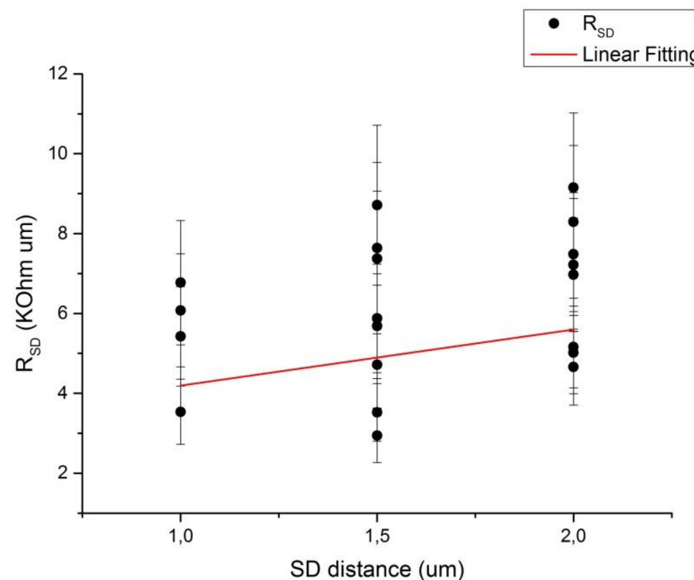

Fig.53: *Source-drain resistance, R_{SD}, versus the source-drain distance, with linear fitting in order to check the trend of the measurements.*

In the above figure, Fig.53, the source-drain resistance, R_{SD}, as a function of the source-drain distance is illustrated. The values of the source-drain resistance were multiplied by the width of the devices for normalization. As it is observed, the source-drain resistance increases with the increasing of the source-drain distance, as we expected since resistance is proportional to source-drain distance. Although, the dispersion of our measurements was pronounced mainly due to the two-dimensional nature of graphene, we calculated the mean values of the source-drain resistances for each source-drain distance, in order to give a quantitative estimation of our measurements. So, the mean value of source-drain resistance for source-drain distance of 1μm was (5.45±1.40)KΩ·μm, in the case of 1.5μm source-drain distance the mean value of source-drain resistance increased to (5.80±2.00)KΩ·μm, and finally for the longer devices with 2μm source-drain distance the mean value of source-drain resistance reached the maximum value of (6.74±1.64)KΩ·μm. Performing a linear fitting we can extract the contact resistance from the intercept of the fitting equation divided by 2 and the sheet resistance of the graphene from the slope of the fitting equation. Therefore, the contact resistance, R_c, is equal to (1.66±0.82)KΩ·μm and the sheet resistance, R_{sheet}, is equal to (1.40±1.03)KΩ/□. The contact resistance is larger than the resistance of graphene itself (sheet resistance) indicating that the source and drain contacts or in other words the quality of these contacts play an essential role to the performance of our devices especially in shorter channel devices in which the contact resistance dominates over the sheet resistance. This fact it will be taken into account in the later presentation and discussion of our results.

- ***Subsection 4: Transconductance***

In this subsection, Subsection 4, we introduce the results of maximum transcoductance and how this important parameter of GFET devices changes as a function of their geometrical characteristics (gate width, number of fingers, source-drain distance, gate length).

Maximum transconductance, g_m, as a function of gate width and number of fingers

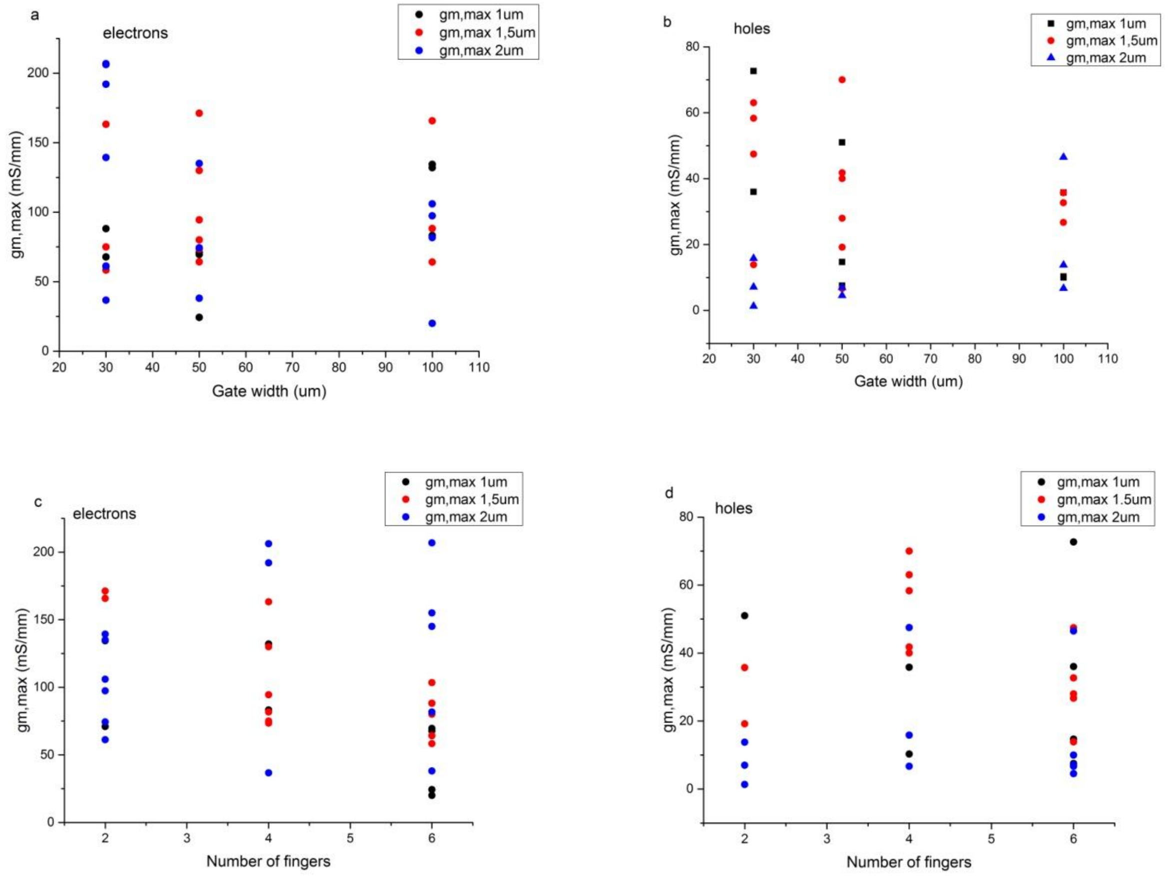

Fig.54: *a)* ***maximum transconductance*** *for* ***electrons*** *as a function of gate width, for different source-drain distances 1um, 1.5um, and 2um respectively. b)* ***maximum transconductance*** *for* ***holes*** *as a function of gate width, for different source-drain distances 1um, 1.5um, and 2um respectively. c)* ***maximum transconductance*** *for* ***electrons*** *as a function of the number of fingers, for different source-drain distances 1um, 1.5um, and 2um respectively. d)* ***maximum transconductance*** *for* ***holes*** *as a function of the number of fingers, for different source-drain distances 1um, 1.5um, and 2um respectively. The maximum values of transconductance were obtained at high drain-source voltage.*

In the above figure, Fig.54, the maximum transconductance both for electrons and holes as a function of the gate width (Fig.54a, Fig.54b) and as a function of the number of fingers (Fig.54c, Fig.54d) is illustrated. The values of the maximum transconductance were obtained for high source-drain voltages, meaning that each of them correspond to a gate voltage in which our devices had the highest performance (usually +2V for electrons and -2V for holes) and to a source-drain voltage that the transconductance reached its maximum value. The maximum transconductance for electrons exhibited the value of

215mS/mm while for the holes the maximum transconductance exhibited the value of 75mS/mm. Since the studied values of maximum transconductance are normalized over the gate width and the number of fingers in the above figure, Fig.54, we cannot observe any pronounced trend between the maximum transconductance neither the gate width nor the number of fingers. Nevertheless, based on our analysis in the previous subsections, we could say that devices with smaller gate width and with larger number of fingers, give higher values of maximum transconductance.

Maximum transconductance, g_m, as a function of source-drain (SD) distance

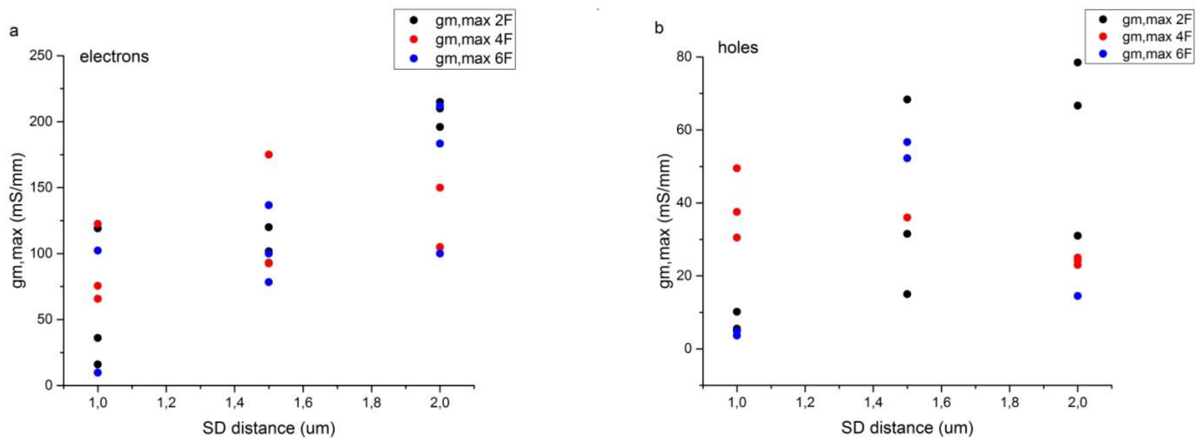

Fig.55: *a)* ***maximum transconductance*** *for* ***electrons*** *as a function of source-drain distancce, for different number of fingers 2, 4, and 6 respectively. b)* ***maximum transconductance*** *for* ***holes*** *as a function of source-drain distance, for different number of fingers 2, 4, and 6 respectively. The maximum values of transconductance were obtained at high drain-source voltage.*

After the study of how the maximum transconductance varies with the gate width and the number of fingers, another important parameter that must be taken into account is the relation between the transconductance and the source-drain distance. In the above figure, Fig.55, this relation is illustrated, both for electrons (Fig.55a) and holes (Fig.55b). As we can see, in both cases, the maximum transconductance increases with the increase of the source-drain distance.

Because the contribution in the conduction of our sample, as resulted from the transfer characteristics, is attributed mainly to electrons transport we will focus our analysis on electrons. So, although the dispersion of the values of the maximum transconductance is large in Fig.55a, we will give a qualitative analysis of our results,

giving the mean values of the maximum transconductance for each source-drain distance. Thus, for 1um source-drain distance the mean value of the maximum transconductance was (68±45)mS/mm, for the case of 1.5um source-drain distance the mean value of the maximum transconductance increased to (110±30)mS/mm and finally for 2um source-drain distance the mean value of the transconductance reached its maximum value of (170±45)mS/mm.

Maximum transconductance, g_m, as a function of gate length

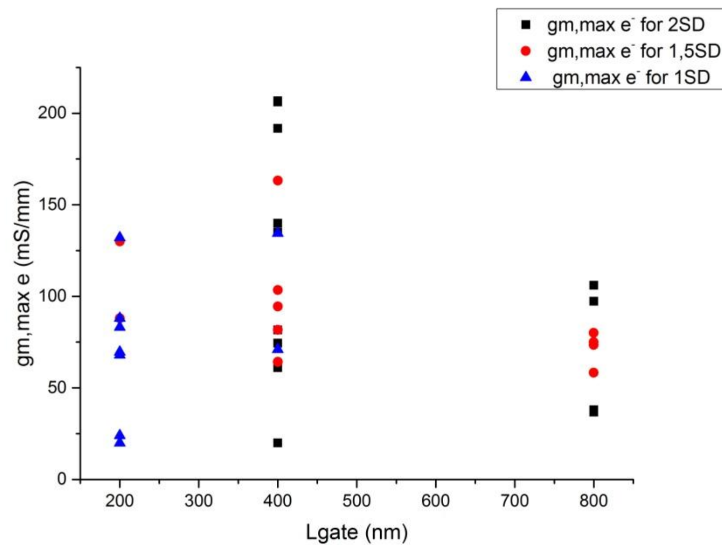

Fig.56: ***maximum transconductance*** *for* ***electrons*** *as a function of gate length, for different source-drain distances 2μm, 1.5μm, and 1μm respectively.*

In the above figure, Fig.56, the maximum transconductance of electrons obtained at high source-drain bias as a function of the gate lengths is illustrated. As we observe, in the case of the 800nm gate length the values of the maximum transconductance are lower than the values achieved for shorter gate lengths. An obvious increase appears in the case of the 400nm gate length but the values reduce for the case of the 200nm gate length. This trend probably is attributed to the enhanced Klein tunneling which is stronger for devices with shorter channels.

In semiconductor MOSFETs, we expect an opposite dependence of the transconductance as a function of the source-drain distance and gate length, meaning that the maximum transconductance should decrease with the increase of the source-drain distance and gate length respectively. In other words, we would expect that shorter GFET devices would exhibit higher performance. But in our case the aforementioned argument was not valid. Possible reasons that could explain the abnormal dependence of the transconductance on the source-drain distance, should be the high contact resistance which was higher than the sheet resistance of graphene (see Subsection 3). In shorter channel devices, the contact resistance dominates over the other components of the total resistance and as a consequence the quality of the metal contacts on graphene strongly affects the performance of such devices. Another possible reason could be the well known issue that since graphene has zero effective mass carriers, short gates exhibit pronounced Klein tunneling effect and thus loose their ability to control the flow of carriers. It is also important to note that the values of the maximum transconductance that are illustrated in the figures, Fig.54, Fig.55, were obtained by applying high source-drain voltages. Therefore, under high drain-to-source biasing the charge trapping is made worse which strongly affects transistor characteristics and especially those of shorter channel because of hot carrier injection [63], [64].

Concerning the latter possible reason, we introduce the maximum transconductance obtained at low source-drain bias (V_{DS}= 0.2V). As we can observe in the following figure, Fig. 57, the maximum transconductance increases with the decrease of the source-drain distance and gate length.

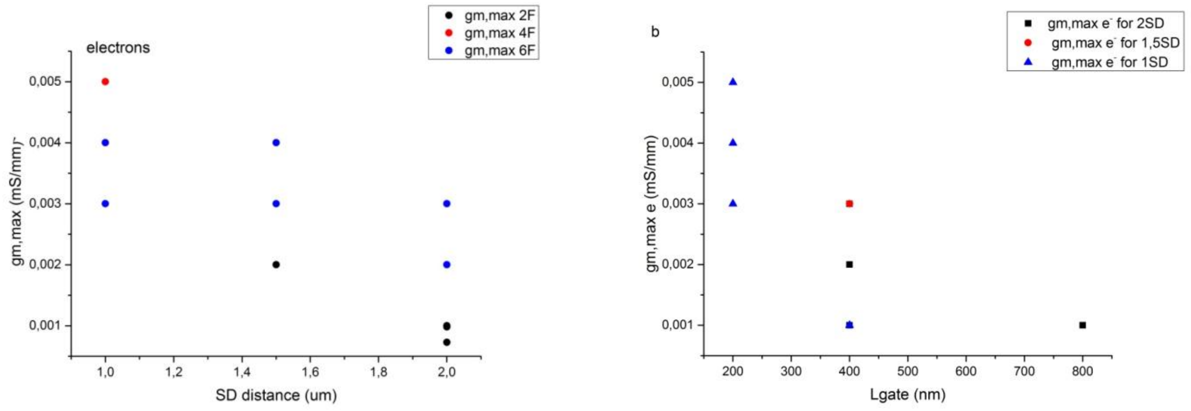

Fig.57: *a) **maximum transconductance** for **electrons** as a function of source-drain distance, for different number of fingers 2, 4, and 6 respectively. b) **maximum transconductance** for **electrons** as a function of gate length, for different source-drain distances 2μm, 1.5μm and 1μm respectively. The maximum values of transconductance were obtained at low drain-source voltage,* $V_{DS}=0.2V$.

6.3.4 Conclusions

In this part, Part 3, we studied the transfer characteristics, the output characteristics, the source-drain resistance and the maximum transconductance of the graphene field effect transistors.

Concerning the transfer characteristics we found that the Dirac point, it is not located at V_G=0V but it is shifted leftward at V_G=-0.70V. This shift reflects the influence (doping) of the top gate, the gate dielectric, the impurities that are present in the graphene channel and defects such as electron-hole puddles that come from the substrate. A clear asymmetry between the hole and electron conduction branches is observed and more specifically the holes contributions to conduction is much smaller than that or electrons contribution. This asymmetry is possible due to the differently doped graphene areas across the source-drain length of graphene field-effect transistor. Finally, far from the Dirac point, a deviation of perfect linearity between I_{DS} and V_G is observed, implying that due to ultra high carrier densities the interaction between the carriers is essential and affects the performance of the device.

The output characteristics showed that the source-drain current (I_{DS}) was increasing as the source-drain voltage (V_{DS}) increased, and higher positive gate biases were resulting in higher source-drain currents. In addition, larger devices conduct higher currents as the theory requires, but the behavior between the source-drain current and source-drain distance was not the expected one. More specifically, the source-drain current did not increase as the source-drain distance decreased. Also a pseudo-saturation region was formed for shorter source-drain distances possible due to the fact that different scattering phenomena take place in shorter devices. Finally, regard to the number of fingers we found that as the number of fingers increases the maximum value of source-drain current also increases. This enhanced response of the devices (from the source-drain current point of view) with the larger number of fingers has similar explanation with the devices with larger width that conduct larger currents.

The electrical resistance across the source-drain distance increased with the increasing of the source-drain distance as we expected, since resistance is proportional to source-drain distance.

Finally, since the studied values of maximum transconductance are normalized over the gate width and the number of fingers, we did not observe any pronounced trend between the maximum transconductance neither the gate width nor the number of fingers. Nevertheless, we could say that devices with smaller gate width and with larger number of fingers, give higher values of maximum transconductance. Contrariwise, a significant trend is observed between the maximum transconductance obtained for high source-drain biases and the source-drain distance. As the source-drain distance and gate length decreased the maximum transconductance also decreased, but this trend was not consistent to what we expected according to the conventional semiconductor MOSFET theory. Possible reasons that could explain the abnormal dependence of the transconductance on the source-drain distance and gate length should be the high contact resistance, the pronounced Klein tunneling effect and thus the loosing of the carriers flow control, and the charge trapping that is made worse and especially in shorter channel because of hot carrier injection [63], [64].

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