UNIVERSITY of CRETE

Physics Department

Fabrication and analysis of heterostructure field effect transistors based on AlN and InN

A dissertation submitted in fulfillment of the requirements for the degree of

Doctor of Philosophy

by

Christos Zervos

Heraklion, Crete, March 2018

Ph. D Dissertation

Fabrication and analysis of heterostructure field effect transistors based on AlN and InN

by

Christos Zervos

Advisory Committee:

Alexandros Georgakilas (Advisor)
Professor, Physics Department, University of Crete

Eleftherios Iliopoulos
Associate Professor, Physics Department, University of Crete

Zekentes Konstantinos
Researcher, Institute of Electronic Structure and Laser, FORTH

Examination Committee:

Alexandros Georgakilas (Advisor)
Professor, Physics Department, University of Crete

Eleftherios Iliopoulos
Associate Professor, Physics Department, University of Crete

Konstantinos Zekentes
Researcher, Institute of Electronic Structure and Laser, FORTH

Nikos Pelekanos
Professor, Department of Materials Science and Technology, University of Crete

Zaharias Hatzopoulos
Associate Professor, Physics Department, University of Crete

George Konstantinidis
Principal Researcher, Institute of Electronic Structure and Laser, FORTH

George Deligeorgis
Researcher, Institute of Electronic Structure and Laser, FORTH

Abstract

The aim of this thesis was to create new knowledge for material and device processing effects on the performance of novel III-Nitride Heterostructure Field Effect (HFET) transistors using either an AlN barrier or InN channel layers. The AlN/GaN heterojunction offers the highest polarization discontinuity for GaN two-dimensional electron gas (2DEG) channel transistors, and high electron mobility transistor (HEMT) devices can be realized with ultra-shallow channels and very high current density.

In this work, an extensive study of unpassivated HEMTs (with L_g~1 μm) based on thin double AlN/GaN/AlN heterostructures with 1 nm GaN cap, directly grown on sapphire subtrates by plasma-assisted molecular beam epitaxy (PAMBE) is reported. The analysis is based on dc, pulsed and breakdown measurements, which were carried out on the devices for an AlN top barrier thickness in the range of 2.2-4.5 nm. The 2DEG density (N_s) varied from 6.8 x 10^{12} to 2.1 x 10^{13} cm^{-2} as the AlN barrier thickness increased from 2.2 to 4.5 nm and the maximum dc drain-source current (I_{ds}) was 1.1 A/mm for AlN barrier thickness of 3.0 and 3.7 nm. The 3.0 nm AlN barrier HEMT exhibited the best operation in terms of standard performance metrics such as transconductance and off-state breakdown voltage (V_{br}). Moreover, the V_{br} of the 3.0 nm AlN barrier HEMT was more than double (70 V) the value measured for a single AlN/GaN HEMT grown on a thick GaN buffer layer, due to improved electron confinement in the 2DEG channel. Pulsed measurements were performed with a 500 ns pulse-width and exhibited a current collapse varied between 6%–12% and 10%–15% under gate and drain lag conditions, respectively. Small positive shifts of threshold voltage (0.2-0.4 V) with negligible reduction of transconductance interpreted to suggest small electron trapping predominantly in the layers and interfaces underneath the Schottky gate contact. These results suggest that the double heterostructures may offer intrinsic advantages for the breakdown and current stability characteristics of high current HEMTs.

AlN/GaN/AlN double heterostructures using a 5-nm-thick GaN quantum well were also tested for transistor normally-off operation. The fabricated devices exhibited very low maximum I_{ds} currents, ranging between 0.16-0.60 mA/mm, due to very high on-resistances resulting from the

absence of 2DEG across the entire source-drain region. These structures may offer promise well beyond the established power-related applications and could be useful for digital applications.

The potential of using in situ SiN_x deposition by PAMBE on an AlN/GaN/AlN HEMT structure (with 1 nm GaN cap and 3.5 nm AlN top barrier thickness) as a passivation layer and gate dielectric, was also investigated. The 5 nm in situ SiN_x dielectric resulted in a large increase in N_s, exhibiting a value of 3.8 x 10^{13} cm^{-2}, when compared to a similar structure without SiN_x cap, in which N_s was 1.9 x 10^{13} cm^{-2}, suggesting the presence of an additional positive charge at the SiN_x/GaN cap interface. HEMT devices with ~1 µm gate length exhibited drain-source currents directly comparable to the N_s values, being 1.15 and 0.43 A/mm at V_{gs} = 0 V for SiN_x and Schottky-gate AlN/GaN/AlN HEMTs, respectively. However, the SiN_x/AlN/GaN/AlN HEMTs exhibited increased gate leakage currents and severe current collapse due to the presence of high interface trap state densities.

To boost performance over GaN-based devices and pave the way for terahertz frequency electronics, InN as channel material represents the best candidate due to its unique transport properties. SiN_x deposited in situ in the PAMBE system could effectively modulate the electron concentration and work as a gate dielectric for 2 nm ultrathin InN channel field effect transistors. Operation of InN-on-GaN field effect transistors was demonstrated for the first time exhibiting a maximum I_{ds} of about 60 mA/mm and a pinch-off voltage of -9.5 V and -15 V for 5 and 10 nm thick SiN_x, respectively.

An increase of InN layer thickness, in the 4-10 nm thickness range, could increase significantly I_{ds} up to 1.2 A/mm, however, the channel could not fully pinch-off. This was attributed to the increased conductivity of the InN layers, caused by the high density of dislocations formed due to the large lattice mismatch between InN and GaN. The charge conduction mechanisms of Ni/SiN_x/InN metal-insulator-semiconductor capacitors were investigated and I-V analysis suggested ohmic conduction by hopping at low electric fields, while field emission of electrons from trap centers in SiN_x located 1.1-1.3 eV below the conduction band was prevailed at high electric fields. These results emphasize the use of ultrathin InN layers and the growth optimization of SiN_x dielectric and SiN_x/InN interface formation as a prerequisite for the development of InN channel transistors for ultra-high frequency applications.

ACKNOWLEDGEMENTS

I would especially like to thank my advisor, Prof. Alexandros Georgakilas, for giving me the opportunity to realize this work in the microelectronics research group of University of Crete and FORTH, as well as for his significant guidance and support during my PhD study.

I am very grateful to all the people in the microelectronics research group for their valuable contribution and assistance during this research project. Adam Adikimenakis for the growth of MBE samples and Thanasis Kostopoulos for his constant support in the clean room activities. Petros Beleniotis, who worked very closely with me during his master's thesis project, was extremely valuable during my research work. He performed a part of theoretical calculations and helped me a lot in the electrical characterization and analysis of a countless number of devices.

I also want to express my gratitude to Antonis Bairamis who carried out band diagram simulations in the first part of this study. Many thanks to Maria Kayambaki for her assistance and technical support in the electrical characterization lab, Katerina Tsagaraki who characterized my samples by SEM and AFM and Maria Androulidaki for FTIR and Raman measurements. I would also like to acknowledge George Stavrinidis for training in the processing lab and George Deligeorgis regarding the rf characterization of devices. I am greatful to friends and colleagues I had the privilege of working with including George Doundoulakis, Stelios Kazazis and Foteini Miziou. I am thankful for their help and support.

Finally, I would like to especially thank Dr. Jan Kuzmik and Milan Tapajna from Slovak Academy of Sciences for all the interesting discussions.

This work was supported partially by the ESPA ARISTEIA program, Project No. 1935: "NITROHEMT" and was co-funded by the European Social Fund (ESF) and National Resources. I am also grateful for the financial support provided by IESL-FORTH until the completion of this research project.

Journal publications

1. **Ch. Zervos**, A. Adikimenakis, P. Beleniotis, A. Kostopoulos, M. Androulidaki, K. Tsagaraki, M. Kayambaki, G. Konstantinidis, and A. Georgakilas, "Investigation of of thin InN/GaN heterostructures with *in situ* SiN_x dielectric grown by plasma-assisted molecular beam epitaxy", J. Vac. Sci. Technol. B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena 35, 021210, 2017.
2. **Ch. Zervos**, A. Adikimenakis, P. Beleniotis, A. Kostopoulos, K. Tsagaraki, M. Kayambaki, G. Konstantinidis, and A. Georgakilas, "In-situ SiN_x/InN structures for InN channel transistors", Appl. Phys. Lett. 108, 142102, 2016.
3. **Ch. Zervos**, A. Adikimenakis, A. Bairamis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas, "Analysis of current instabilities of thin AlN/GaN/AlN double heterostructure high electron mobility transistors", Semicond. Sci. Technol. 31, 065002, 2016.
4. A. Bairamis, **Ch. Zervos**, A. Adikimenakis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis & A. Georgakilas, "Electron density and currents of AlN/GaN high electron mobility transistors with thin GaN/AlN buffer layer", Appl. Phys. Lett. 105, 113508, 2014.

Publications in conference preceedings

1. A. Adikimenakis, **Ch. Zervos**, P. Beleniotis, A. Kostopoulos, K. Tsagaraki, M. Kayambaki, G. Konstantinidis, and A. Georgakilas, "InN/SiN_x MIS capacitors and MISFETs grown by Plasma-Assisted MBE", 40th Workshop on Compound Semiconductors Devices and Integrated Circuits (WOCSDICE), 6-10 June 2016, Aveiro, Portugal, pp. 45-46.
2. **Ch. Zervos**, A. Bairamis, A. Adikimenakis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis & A. Georgakilas, "AlN/GaN/AlN double heterostructures with thin AlN top barriers", 10th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM), 20-22 October 2014, Smolenice, Slovakia, pp. 113-116 (IEEE, 2014).
3. **Ch. Zervos**, A. Bairamis, A. Adikimenakis, A. Kostopoulos, M. Kayampaki, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas, "AlN/GaN HEMTs with thin GaN/AlN buffer

layers on sapphire (0001) substrates", 38th Workshop on Compound Semiconductors Devices and Integrated Circuits (WOCSDICE), 15-20 June 2014, Delphi, Greece, pp. 55-56.

Conference presentations

1. **<u>Ch. Zervos</u>**, A. Adikimenakis, P. Beleniotis, A. Kostopoulos, M. Kayambaki, M. Androulidaki, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas, "InN field-effect transistors with in-situ SiN_x gate dielectric", European Congress and Exhibition on Advanced Materials and Processes (EUROMAT 2017), 17-22 September 2017, Thessaloniki, Greece.
2. A. Georgakilas, A. Adikimenakis, **<u>Ch. Zervos</u>**, A. Bairamis, K. E. Aretouli, K. Tsagaraki, A. Kostopoulos, A. Stavrinidis, E. Tsikritsaki, E. Iliopoulos, and G. Konstantinidis, "Physics and growth of AlN/GaN HEMT structures on sapphire and diamond substrates", European Materials Research Society (EMRS 2015), 15-18 September 2015, Warsaw, Poland. (**invited paper**).
3. **<u>Ch. Zervos</u>**, A. Adikimenakis, A. Bairamis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas, "Analysis of device characteristics of thin AlN/GaN/AlN HEMTs grown on sapphire substrates", 11th International Conference on Nitride Semiconductors (ICNS-11), 30 August – 4 September 2015, Beijing, China.
4. A. Bairamis, **<u>Ch. Zervos</u>**, A. Adikimenakis, A. Kostopoulos, M. Kayampaki, K. Tsagaraki, G. Konstantidis and A. Georgakilas, "Growth and evaluation of thin AlN/GaN/AlN HEMT structures by molecular beam epitaxy", 11th International Conference on Nitride Semiconductors (ICNS-11), 30 August – 4 September 2015, Beijing, China.
5. A. Adikimenakis, K. Tsagaraki, A. Bairamis, **<u>Ch. Zervos</u>**, and A. Georgakilas, "Growth and properties of AlN on sapphire (0001) substrates", 11th International Conference on Nitride Semiconductors (ICNS-11), 30 August – 4 September 2015, Beijing, China.
6. **<u>Ch. Zervos</u>**, A. Bairamis, A. Adikimenakis, A. Kostopoulos, M. Kayampaki, K. Tsagaraki, G. Konstantinidis and A. Georgakilas, "AlN/GaN/AlN double heterostructures with thin AlN top barriers", 10th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM 2014), Smolenice Castle, Slovakia, 20-22 October, 2014.

7. **Ch. Zervos**, A. Bairamis, A. Adikimenakis A. Kostopoulos, M. Kayampaki, K. Tsagaraki, G. Konstantinidis and A. Georgakilas, "AlN/GaN HEMTs with thin GaN/AlN buffer layers on sapphire (0001) substrates", 38th Workshop on Compound Semiconductor Devices and Integrated Circuits" (WOCSDICE 2014), Delphi, Greece, 15-18 June, 2014.

8. **Ch. Zervos**, A. Adikimenakis, F. Miziou, A. Bairamis, M. Kayambaki, A. Kostopoulos, G. Konstantinidis, and A. Georgakilas, "Effects of Al cap layers and HCl treatment on contacts on AlN/GaN 2DEG heterostructures", International Workshop on Nitride Semiconductors (IWN 2014), Wroclaw, Poland, 24-29 August, 2014.

9. A. Bairamis, **Ch. Zervos**, A. Adikimenakis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis and A. Georgakilas, "Growth and evaluation of thin AlN/GaN/AlN HEMT structures by Molecular Beam Epitaxy", 30th Panhellenic Conference on Solid-State Physics and Materials Science, Heraklion, Crete, Greece, 21-24 September, 2014.

‘On the meridian of time, there is no injustice:

there is only the poetry of motion creating the illusion of truth and drama’

Henry Miller

Contents

CHAPTER 1 .... **1**

Introduction **1**

1.1 III-Nitride semiconductors 1

1.2 Scope of this work 3

1.3 Chapter 1 references 5

CHAPTER 2 .... **8**

Fundamentals of III-Nitrides & Device Characteristics **8**

2.1 Polarization physics and the AlN/GaN heterostructure 8

2.2 AlN/GaN HEMT device characteristics 13

2.2.1 Scattering effects and mobility 13

2.2.2 Current-voltage relationship of HEMT 15

2.2.3 Transconductance and parasitic resistance 18

2.2.4 Breakdown voltage 20

2.2.5 Ohmic and Schottky contacts 21

2.3 Metal-Insulator-Semiconductor Capacitors 25

2.3.1 Ideal MIS Capacitor 25

2.3.2 Interface traps 27

2.3.3 Insulator charges 28

2.3.4 Flat-band voltage 28

2.3.5 Charge conduction mechanisms 30

2.4 Literature summary for III-nitride HEMTs 32

2.4.1 Overview of the AlN/GaN heterostructure system 33

2.4.2 InN-based heterostructures background 33

2.5 Chapter 2 references 35

CHAPTER 3 .... **44**

Device Processing and Characterization **44**

3.1 Device fabrication 44

3.1.1 Surface cleaning 46

3.1.2 Mesa isolation 46

3.1.3 Ohmic metallization 48
3.1.4 Gate metallization 48
3.2 Electrical characterization methods 49
3.2.1 DC characterization 49
3.2.2 Pulsed characterization 49
3.2.3 Capacitance-Voltage characterization 51
3.3 Chapter 3 references 56
CHAPTER 4 58
AlN/GaN/AlN HEMTs 58
4.1 Introduction and motivation of the study 58
4.2 Experimental details 61
4.3 Polarization effects 63
4.4 Electrical properties 65
4.5 C-V characterization of Schottky contacts 67
4.6 DC characterization of AlN/GaN/AlN HEMT transistors 69
4.7 Pulsed characterization of AlN/GaN/AlN HEMTs and of trapping effects 76
4.8 Normally-off approach of AlN/GaN heterostructures 85
4.9 AlN/GaN/AlN HEMTs with in-situ deposited SiN_x 88
4.8 Conclusions 97
4.9 Chapter 4 references 97
CHAPTER 5 107
InN-based devices 107
5.1 Introduction to InN 107
5.2 SiN_x/InN/GaN structures with 2 nm ultrathin InN layer 108
5.3 SiN_x/InN/GaN structures with 4/7/10 nm thin InN layer 116
5.4 Summary 123
5.6 Chapter 5 references 123
CHAPTER 6 128
Conclusions 128
6.1 Summary of the results 128
6.2 Future work 129
6.3 Chapter 6 references 131

CHAPTER 1

Introduction

1.1 III-Nitride semiconductors

Since the emergence of III-Nitride semiconductors (GaN, AlN, InN) and the first reports of GaN-based field effect transistors in the early 1990s [1,2], the III-Nitride system with direct band gap energies from 0.65 to 6.2 eV, which cover the whole visible spectrum (Fig. 1.1), has attracted an enormous attention by various academic institutions and industrial laboratories for both optical and electronic applications. The large bandgap (except for InN) and the corresponding high breakdown electric fields, excellent transport properties and the high thermal stability are the primary advantages of the nitrides over other semiconductors. They also exhibit spontaneous and piezoelectric polarization along the usual growth axis (the [0001], c-axis), which can result to the formation of a two-dimensional electron gas (2DEG) at the heterointerface of two III-Nitride layers. Thus, 2DEG structures suitable for fabrication of high electron mobility transistors (HEMTs) can be realized, without the introduction of dopants.

Typically, a thin $Al_xGa_{1-x}N$ layer epitaxially grown on Ga-face (0001) GaN results to a polarization induced 2DEG at the GaN side of the AlGaN/GaN heterointerface, which is used as the channel of GaN HEMTs. The 2DEG density which can reach values in the 10^{13} cm^{-2} range, well in excess of those observed in other III-V semiconductor systems, can be modified by changing the thickness of the AlGaN barrier as well as the Al content (AlN mole fraction, x). However, to achieve high frequency operation ultra-scaled devices are needed. This implies a decrease of the metallurgical gate length L_g as well as a decrease of the barrier thickness t_b to avoid short channel effects [3-5] restricting the performance of devices. Short channel effects take the form of a degraded drain current modulation by the gate voltage, which causes a negative threshold voltage shift resulting from poor confinement of electrons in the channel [4,5]. Typically, an aspect ratio $L_g/t_b \geq 5$ is required [4]; for example, for $L_g = 20$ nm the barrier thickness should be decreased

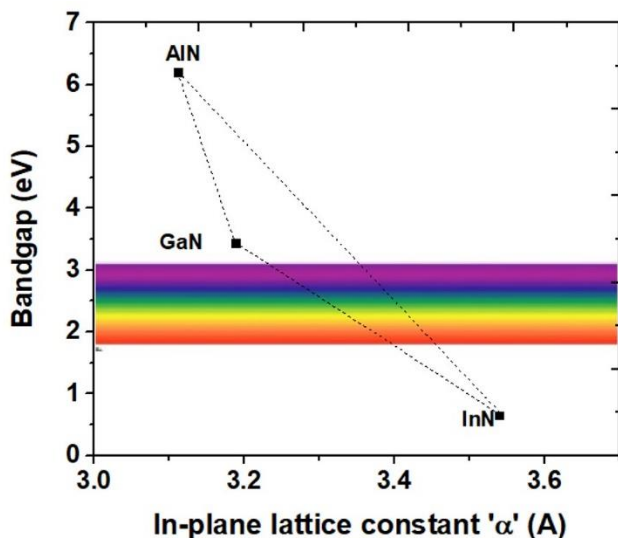


Figure 1.1. The bandgap versus lattice constant 'α' plot. The color scale for the visible spectrum corresponds to the bandgap.

---

to 4 nm to obtain L_g/t_b = 5 and mitigate short channel effects [4]. However, decreasing the AlGaN barrier thickness below 10 nm results in a strong decrease on the 2DEG density [6] causing a poor device performance.

To minimize the $Al_xGa_{1-x}N$ barrier thickness while achieving a high 2DEG density for GaN HEMTs, an ultrathin AlN barrier is an excellent candidate since the net polarization charge at the interface, and therefore the possible 2DEG density (ranging between 2 – 6 x 10^{13} cm^{-2}), is the highest that can be achieved for the $Al_xGa_{1-x}N$/GaN heterojunction [7]. On the other hand, AlN/GaN heterostructures may exhibit epitaxial growth and fabrication issues due to factors like large tensile strain ~2.4% between the AlN and the underlying GaN layer, strain relaxation and surface sensitivity of AlN [7-13].

To boost performance over GaN-based devices and pave the way for terahertz frequency electronics, InN as channel material may represent the best candidate due to its unique properties such as small electron effective mass, very high mobility, and high electron peak velocity (~6 x 10^7 cm/s) [14,15] (Fig.1.2). However, several challenges need to be addressed before any high-speed/frequency InN channel transistors will be developed. Major impediments are related to (a) high bulk electron concentration in 10^{18}–$10^{19}$$cm^{-3}$ range, (b) Fermi level pinning at the InN surface

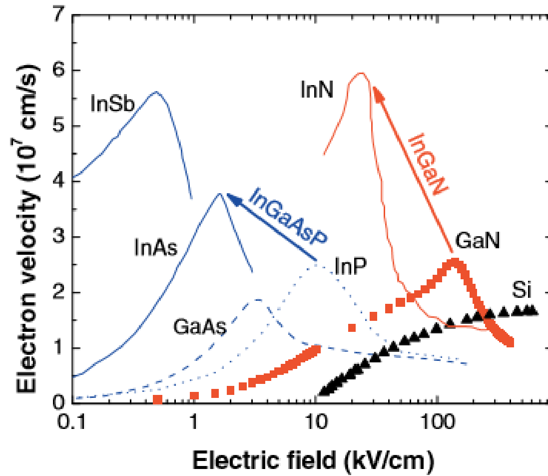


Figure 1.2. Electron velocity dependence on the electric field at room temperature in various semiconductors. Image taken from ref. [15].

---

within the conduction band [16] and formation of a surface electron accumulation layer [16-18], (c) large lattice mismatch (>10%) between InN and either GaN or AlN buffer layers, leading to immediate strain relaxation by introduction of misfit dislocations [19-21], with the accompanying formation of threading dislocations, and (d) electron accumulation at the highly defective epilayer/substrate interfaces [17,18].

1.2 Scope of this work

Polarization plays an important role in the electrical properties of nitride heterostructures and presents many interesting possibilities for the realization of novel device structures. While the targeted goal of GaN-based transistors is in high-frequency/high power applications, the scope of this work was not to set records in maximum operation frequencies or output power densities. Instead, the objective of this research effort was to identify the effects of epitaxial growth, heterostructure design and device fabrication processes on the operation characteristics of novel HEMT devices, with either AlN barrier or InN channel.

Chapter 2 presents the essential background of the III-Nitride semiconductor system. GaN-based HEMT basic operation is enlightened and brief description of the devices characteristics such as transconductance, breakdown and ohmic/Schottky and MIS contacts is provided. Charge

conduction mechanisms are also discussed. The chapter concludes with a literature summary concerning the Al(Ga)N/GaN system and the InN-based heterostructures background.

Chapter 3 presents the basic fabrication tools and details regarding the processing steps followed in this work; UV lithography, plasma etching, ohmic and gate metallization. The basic electrical characterization methods (DC and pulsed I-V, C-V) are also presented.

In Chapter 4, the potential of thin double AlN/GaN/AlN HEMT heterostructures (~0.5 μm total thickness), with 1 nm GaN cap, and different AlN top barrier thicknesses, directly grown on sapphire substrates by plasma-assisted molecular beam epitaxy (PAMBE), is demonstrated. Dc and pulsed I–V, C-V and electric breakdown measurements were performed in the fabricated devices and the electrical characteristics are analyzed and discussed. AlN/GaN/AlN double heterostructures using a 5-nm-thick GaN quantum well were also tested for transistor normally-off operation. The potential of using in situ SiN_x deposition on AlN/GaN/AlN HEMT structures, at the end of their growth in the PAMBE reactor, as a passivation layer and gate dielectric, is also investigated. Finally, the electrical characteristics of Ni/SiN_x/GaN metal-insulator-semiconductor capacitors (MISCAPs) with a SiN_x dielectric deposited at three different temperatures, 250, 500 and 700 ^oC, are evaluated.

Chapter 5 focuses on the formation and properties of Ni/SiN_x/InN MISCAPs and InN MIS-gate field effect transistors (MISFETs). SiN_x dielectric layers were deposited in-situ in the PAMBE system on the surface of thin InN layers, grown on GaN buffer layers. MISCAPs were fabricated and the C-V and I-V measurements are presented. The capability of MISCAPs to control the electron concentration in the InN layer allowed the successful fabrication and operation of MISFET InN transistors in the case of an ultrathin 2 nm InN layer. To further extend this evaluation, the effect of InN channel thickness is examined and the charge conduction mechanisms are analyzed and discussed for a 4-10 nm InN thickness range.

Chapter 6 concludes the results obtained in this work and provides suggestions for future research.

1.3 Chapter 1 references

[1] M. Asif Khan, J. N. Kuznia, A. R. Bhattarai, and D. T. Olson. Metal semiconductor field effect transistor based on single crystal GaN. Appl. Phys. Lett. 62, 1786, 1993.

[2] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson. High electron mobility transistor based on GaN-$Al_xGa_{1-x}N$ heterojunction. Appl. Phys. Lett. 63, 1214, 1993.

[3] G. H. Jessen, R. C. Fitch, J. K. Gillespie, G. Via, A. Crespo, D. Langley, D. J. Denninghoff, M. Trejo, and E. R. Heller. Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices. IEEE Trans. Electron Devices 54, 2589, 2007.

[4] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos, and M. Micovic. Scaling of GaN HEMTs and schottky diodes for submillimeter-wave MMIC applications. IEEE Trans. Electron Devices 60, 2982, 2013.

[5] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert, and J. C. De Jaeger. Punch-through in short-channel AlGaN/GaN HFETs. IEEE Trans. Electron Devices 53, 395, 2006.

[6] F. Medjdoub. Ultrathin GaN-on-Silicon devices for millimeter wave applications. Microelectronics Reliability 54, 1, 2014.

[7] Y. Cao and D. Jena. High-mobility window for two-dimensional electron gases at ultrathin AlN/GaN heterojunctions. Appl. Phys. Lett. 90, 182112, 2007.

[8] K. D. Chabak, D. E. Walker, M. R. Johnson, A. Crespo, A. M. Dabiran, D. J. Smith, A. M. Wowchak, S. K. Tetlak, M. Kossler, J. K. Gillespie, R. C. Fitch, and M. Trejo. High-performance AlN/GaN HEMTs on sapphire substrate with an oxidized gate insulator. IEEE Electron Device Lett. 32, 1677, 2006.

[9] A. Adikimenakis, K. E. Aretouli, E. Iliopoulos, A. Kostopoulos, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas. High electron mobility transistors based on the AlN/GaN heterojunction. Microelectron. Eng. 86, 1071, 2009.

[10] T. Huang, X. Zhu, K. M. Wong, and K. M. Lau. Low-leakage-current AlN/GaN MOSHFETs using Al_2O_3 for increased 2DEG. IEEE Electron Device Lett. 32, 212, 2012.

[11] S. Taking, D. MacFarlane, and E. Wasige. AlN/GaN MOS-HEMTs with thermally grown Al_2O_3 passivation. IEEE Electron Device Lett. 32, 1418, 2011.

[12] A. Bairamis, Ch. Zervos, A. Adikimenakis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis & A. Georgakilas. Electron density and currents of AlN/GaN high electron mobility transistors with thin GaN/AlN buffer layer. Appl. Phys. Lett. 105, 113508, 2014.

[13] Ch. Zervos, A. Adikimenakis, A. Bairamis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas. Analysis of current instabilities of thin AlN/GaN/AlN double heterostructure high electron mobility transistors. Semicond. Sci. Technol. 31, 065002, 2016.

[14] Ch. Zervos, A. Adikimenakis, P. Beleniotis, A. Kostopoulos, K. Tsagaraki, M. Kayambaki, G. Konstantinidis, and A. Georgakilas. In-situ SiN_x/InN structures for InN channel transistors. Appl. Phys. Lett. 108, 142102, 2016.

[15] T. Palacios. Beyond the AlGaN/GaN HEMT: new concepts for high speed transistors. Phys. Status Solidi A 206, 1145, 2009.

[16] I. Mahboob, T. D. Veal, C. F. McConville, H. Lu, and W. J. Schaff. Intrinsic electron accumulation at clean InN surfaces. Phys. Rev. Lett. 92, 036804, 2004.

[17] H. Lu, W. J. Schaff, L. F. Eastman, and C. E. Stutz. Surface charge accumulation of InN films grown by molecular-beam epitaxy. Appl. Phys. Lett. 82, 1736, 2003.

[18] C. C. Katsidis, A. O. Ajagunna, and A. Georgakilas. Optical characterization of free electron concentration in heteroepitaxial InN layers using Fourier transform infrared spectroscopy and a 2 x 2 transfer matrix algebra. J. Appl. Phys. 113, 073502, 2013.

[19] E. Dimakis, E. Illiopoulos, K. Tsagaraki, Th. Kehagias, Ph. Komninou, and A. Georgakilas. Heteroepitaxial growth of In-face InN on GaN (0001) by plasma-assisted molecular-beam epitaxy. J. Appl. Phys. 97, 113520, 2005.

[20] Th. Kehagias, A. Delimitis, Ph. Komninou, E. Iliopoulos, E. Dimakis, A. Georgakilas, and G. Nouet. Misfit accommodation of compact and columnar InN epilayers grown on Ga-face GaN (0001) by molecular-beam epitaxy. Appl. Phys. Lett. 86, 151905, 2005.

[21] Ch. Zervos, A. Adikimenakis, P. Beleniotis, A. Kostopoulos, M. Androulidaki, K. Tsagaraki, M. Kayambaki, G. Konstantinidis, and A. Georgakilas. Investigation of of thin InN/GaN heterostructures with *in situ* SiN_x dielectric grown by plasma-assisted molecular beam epitaxy. J. Vac. Sci. Technol. B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena 35, 021210, 2017.

CHAPTER 2

Fundamentals of III-Nitrides & Device Characteristics

2.1 Polarization physics and the AlN/GaN heterostructure

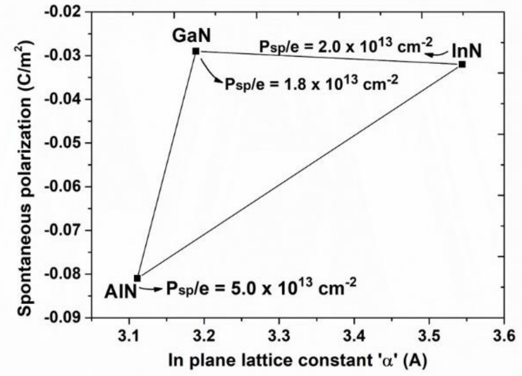
Polarization in the III-Nitride semiconductor system comprises an attractive characteristic for the development of HEMT devices and will be discussed briefly in the following. For an in depth analysis of the polarization physics in III-Nitrides, the reader is cited to the book of C. Wood and D. Jena [1]. Our studies will be confined to metal (Ga, Al or In)-face (0001) structures, meaning that the crystal surface would consist of Ga or Al or In atoms if one cuts the crystal along a plane with vertical bonds. The bonds in all III-V and II-VI semiconductors are polar due to the difference in the ionicity of the constituent atoms. The wurtzite crystal structure characteristic of III-Nitrides results to the existence of a large spontaneous polarization field P_{sp} aligned along the $[000\overline{1}]$ direction. The nonzero P_{sp} exists due to the lower symmetry of the wurtzite crystal structure compared to the cubic zinc-blende structure, for which P_{sp} vanishes [1]. To obtain an estimation of the magnitude of P_{sp}, the (spontaneous) polarization induced surface charge densities of relaxed InN, GaN and AlN crystals, P_{sp}/e ($e = -1.602 \times 10^{-19}$ C), are ~ 1.99×10^{13}, 1.81×10^{13} and 5.05×10^{13} cm^{-2}, respectively (Table 2.1, Fig. 2.1) [2]. These charges are fixed, and are large enough to affect significantly the electrical properties of the material at surfaces and interfaces.

In addition to spontaneous polarization effects, III-Nitrides are also characterized by large piezoelectric coefficients and large values of piezoelectric polarization arise when strain is applied to the crystal. Lateral expansion or contraction of the films' crystal results from the strained epitaxial growth on a substrate with a different lattice constant, and leads to the generation of a piezoelectric polarization field P_{pz} that can be comparable in magnitude to P_{sp} [1]. P_{pz} can be calculated from

$$P_{pz} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad (2.1)$$

where α_0 is the equilibrium in-plane lattice constant, α is the actual lattice constant (strained), e_{31} and e_{33} are the piezoelectric coefficients, and C_{13}, C_{33} are the elastic constants (Table 2.1).

material	Lattice constant α_0 (c_0) A	Direct gap (eV)	P_{sp} (C/m^2)	e_{33} (C/m^2)	e_{31} (C/m^2)	C_{13} (GPa)	C_{33} (GPa)
GaN	3.189 (5.185)	3.4	-0.029	0.73	-0.49	103	405
InN	3.544 (5.718)	0.65	-0.032	0.97	-0.57	92	224
AlN	3.111 (4.978)	6.2	-0.081	1.46	-0.60	108	473



(left) Table 2.1 III-Nitride material properties [1], (right) Fig. 2.1 Predicted spontaneous polarization P_{sp} for GaN, AlN and InN showing the corresponding surface polarization charge densities P_{sp}/e [1,2].

The values of C_{13}, C_{33} and e_{33} are always positive in wurtzite III-Nitrides, while e_{31} is always negative. This means that $(e_{31} - e_{33}C_{13}/C_{33})$ will always be negative. As a result, P_{pz} in these materials is always negative for layers under tensile strain ($\alpha > \alpha_0$) and positive for layers under compressive strain ($\alpha < \alpha_0$). P_{sp} is always negative, which means that the polarization vector points towards the $[000\overline{1}]$ direction (the substrate), P_{sp} and P_{pz} are parallel to each other for tensile strain, and in the case of compressive strain the two polarizations are antiparallel [1].

Since most of the material presented in this work will deal with growth on GaN (0001) buffer layers, strain will be referenced to the relaxed lattice of GaN. In the following, the AlN/GaN heterojunction will be discussed for the case of a strained AlN layer grown on top of a strain-relaxed GaN layer, which comprise a significant part of this thesis. In that case, P_{sp} in GaN points in the direction shown in Fig. 2.2 towards the substrate and there is an absence of piezoelectric polarization. The AlN is grown pseudomorphically on GaN and will have an in-plain tensile strain $\varepsilon_1 = (\alpha_{GaN} - \alpha_{AlN}) / \alpha_{AlN} > 0$ due to its smaller lattice constant α compared to GaN. This results to a piezoelectric polarization in the AlN layer in addition to the spontaneous polarization. Utilizing the piezoelectric and spontaneous polarization coefficients from ref. [3], for fully strained AlN, the polarization sheet charge at the AlN/GaN interface will be:

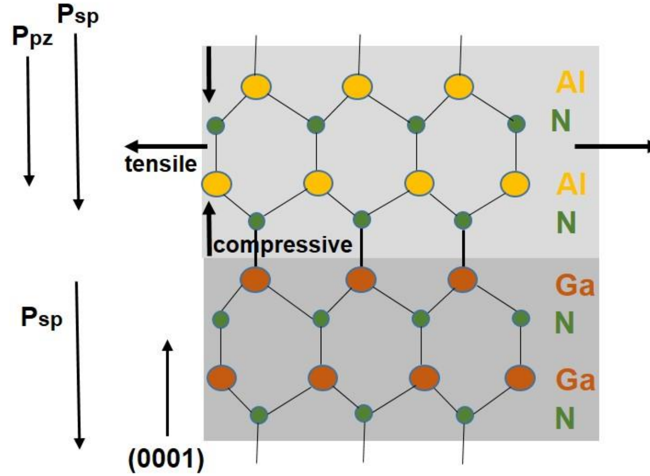


Fig. 2.2 Schematic drawing showing polarization fields in Ga-face strained AlN/GaN heterostructures (adapted from *Polarization effects in semiconductors- C. Wood and D. Jena.,* ref. [1]). The lattice mismatch causes a biaxial tensile strain, and the thermal mismatch (caused by the thermal expansion coefficient difference between the substrate and the epitaxial layer) may result a biaxial compressive strain in the growth plane [1].

$$\sigma/e = \Delta P/e = 1/e[(P_{(AlN)} - P_{(GaN)}] = 1/e\{P_{sp(AlN)} + P_{pz(AlN)}\} - (1/e)P_{sp(GaN)} = +6.4 \times 10^{13}\ /cm^2$$

As a consequence, free electrons will be attracted by the positive bound sheet charge at the AlN/GaN interface, and a 2DEG with a sheet carrier density (N_s) close to the density of the bound sheet charge can be formed. In real applications, the surface band bending prevents approaching sheet carrier densities as high as 6.4×10^{13} cm^{-2} for AlN barrier thicknesses up to ~5 nm, which is the maximum possible thickness without strain relaxation (formation of microcracks) [4].

Nowadays it is generally accepted that donor-like surface states play an important role in the formation of the 2DEG. The group of U. K. Mishra in 2000 was the first group to point this out based on a simple electrostatic analysis in an AlGaN/GaN structure [5]. The sum of the various space charges should be zero since the structure as a whole must be charge neutral in the absence of an externally applied field. Following Fig. 2.3, the charge components contained in the structure are (a) the 2DEG electrons with a charge $\sigma_n = eN_s$, (b) polarization-induced charges; σ_{p1} is the total (spontaneous plus piezoelectric) polarization charge at the AlGaN edges and σ_{p2} is the polarization

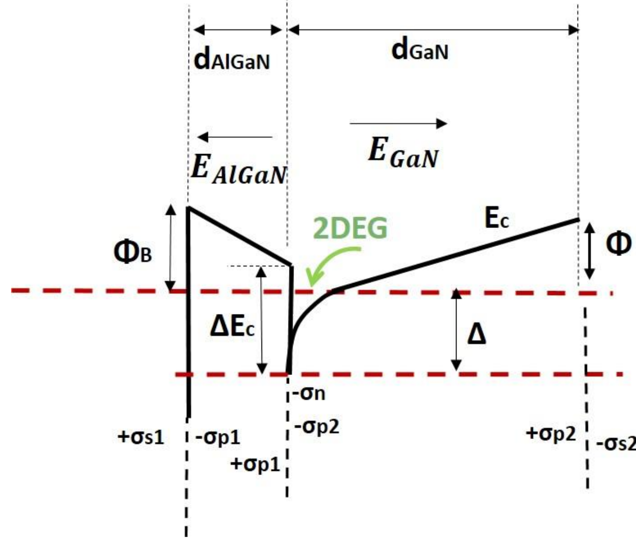


Fig. 2.3 Schematic energy band diagram, shown relative to the Fermi level for the AlGaN/GaN heterostructure where the 2DEG channel of the HEMT can be approximately characterized by a triangular potential well. Charges associated with each interface are also indicated.

---

charge at the GaN buffer edges, (c) charge σ_{s1} due to ionized surface states, and (d) σ_{s2} is the magnitude of the negative charge at the bottom buffer interface. The polarization-induced charges, by their nature, form a dipole whose net contribution to the total space charge is zero.

If the bottom buffer interface is neglected, since in well-designed field effect transistors the buffer (bulk) charge should be as small as possible, the following charge neutrality equation can be obtained

$$\boldsymbol{\sigma_{s1} - eN_s = 0} \tag{2.2}$$

The above equation implies that a positive surface charge must exist due to electron transfer from donor-like surface states into empty states in the GaN that are lower in energy [5]. Now considering the conduction band profile (Fig. 2.3), by applying Gauss' law at the heterointerface a relationship between the fields in each layer to the interface charges is given by [6,7]

$$\varepsilon_{GaN} E_{GaN} + \varepsilon_{AlGaN} E_{AlGaN} = \sigma_{p1} - \sigma_{p2} - \sigma_n \tag{2.3}$$

where ε_{GaN} and ε_{AlGaN} are the permittivity of the buffer and barrier respectively, and E_{GaN}, E_{AlGaN} are the electric fields. Similarly, by assuming zero field outside the structure, the positive surface charge σ_{s1} is related to the field in the barrier by [6,7]:

$$-\varepsilon_{AlGaN} E_{AlGaN} = \sigma_{S1} - \sigma_{p1} \quad (2.4)$$

Also, from the equilibrium band diagram of the structure another equation for E_{AlGaN} can obtained: [1,7]

$$\Phi_B - eE_{AlGaN} d_{AlGaN} - \Delta E_c + \Delta = 0 \quad (2.5)$$

Δ is the magnitude of the depth of the quantum well in the conduction band below the Fermi level, which is determined by the electron density in the well [6,7], Φ_B is the metal/AlGaN Schottky barrier height (or the surface potential), ΔE_c is the AlGaN/GaN conduction band offset and d_{AlGaN} is the thickness of the AlGaN layer.

From Eq. (2.5), the electric field in the barrier is

$$E_{AlGaN} = \frac{\Phi_B - \Delta E_c + \Delta}{ed} \quad (2.6)$$

The field in the buffer can be approximated by

$$E_{GaN} d_{GaN} = \Phi \quad (2.7)$$

where Φ is the potential difference along the buffer layer.

By substituting Eq. (2.6, 2.7) in Eq. (2.3) it is derived that

$$\sigma_n = \sigma_{p1} - \sigma_{p2} - \varepsilon_{AlGaN} \left(\frac{\Phi_B - \Delta E_c + \Delta}{ed_{AlGaN}} \right) - \varepsilon_{GaN} \frac{\Phi}{d_{GaN}} \quad (2.8)$$

In Eq. (2.8), the last term that corresponds to the depletion term from the buffer can be neglected, since the buffer layer is typically much thicker than the barrier ($d_{GaN} >> d_{AlGaN}$). Taking into account that $\sigma_n = eN_s$, Eq. (2.8) results in the widely cited equation reported by Ambacher et al [3]

$$\boldsymbol{N_s = \frac{\sigma_{p1} - \sigma_{p2}}{e} - \frac{\varepsilon_{AlGaN}}{de^2} (\Phi_B - \Delta E_c + \Delta)} \quad \mathbf{(2.9)}$$

Thus, from the above discussion it is concluded that N_s increases with thickness of the AlGaN barrier according to the interplay between Fermi level, occupied surface states, and the AlGaN/GaN conduction band discontinuity.

2.2 AlN/GaN HEMT device characteristics

AlN/GaN HEMTs are excellent candidates for high frequency and high-power switching applications due to the extremely shallow channel with very high electron density and gate capacitance, enabling very high drive current ($J=eN_s v_e$) and transconductance ($g_m \sim v_{sat} C_{gs}$) [8]. The high electron mobility and 2DEG density in these structures yield a high $N_s\mu$ product which contributes to a low on-state resistance R_{on} [1]. At the same time, the wide band gap of GaN makes the breakdown voltage of III-nitride based devices generally higher than analogous devices of the same size fabricated with Si or classical III-V semiconductors.

2.2.1 Scattering effects and mobility

In any semiconductors, electrons are accelerated by an electric field and achieve an average velocity determined by the carrier scattering effects [1]. Mobility is a key parameter in the operation of electronic devices used to characterize the microscopic quality of the semiconductor layers. The low field mobility (μ) is defined as the proportionality constant in the average carrier velocity (v_d) versus electric field (E) relationship:

$$v_d = \mu E \tag{2.10}$$

In high electric fields, Eq. 2.10 is invalid since the velocity at a specific lateral electric field within the HEMT channel approaches a constant value known as the saturated drift velocity (Fig. 2.4) [1]. This property arises from various scattering effects within the crystal. When the electric field achieves such a level that scattering prohibits further increase in velocity at higher fields, velocity saturation occurs [1].

Figure 2.4 shows the structure of the AlN/GaN HEMT and the electric field directed along the channel E(x) during typical device operation [1]. The integrated area under the electric field plot equals to the drain-source (symbols: d, s, respectively) applied voltage, $-\int_s^d E(x)dx = V_{ds}$ [1]. Since usually the drain contact is biased while the source is grounded, the electric field is non-

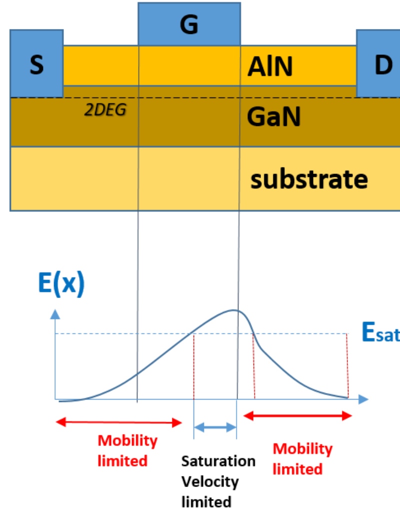


Fig. 2.4 AlN/GaN HEMT structure and the electric field along the channel under typical HEMT operation. The integrated area under the electric field plot equals to the drain-source applied voltage, $-\int_s^d E(x)dx = V_{ds}$ (adapted from *Polarization effects in semiconductors - C. Wood and D. Jena.*, ref. [1]).

---

uniform and it peaks at the gate side towards the drain [1]. Under typical device operation, the field in this regime exceeds the field beyond which the electron velocity saturates, E_{sat} (Fig. 2.4) [1]. Even in this situation, which occurs at high bias conditions, a major fraction of the channel has an electric field lower than the saturationfield, where the electron velocity $v(x)$ is linearly related to the field through the relationship $v(x) = \mu E(x)$. The source-access region (the region between source and gate) is an unwanted series resistance which slows the HEMT operation and the resistivity of this region is limited by the $N_s\mu$ product [1]. Therefore, the electrons transport through a part of the channel is always mobility limited, as shown in Fig. 2.4.

A high electron mobility is of great importance for obtaining high speed devices. The AlN/GaN heterostructure, as a binary junction, eliminates disordered alloy scattering [1] which is present in the case of an $Al_xGa_{1-x}N$ barrier, and therefore greatly benefits the 2DEG low-field mobility [9]. However, a number of scattering mechanisms exists for AlN/GaN HEMTs limiting the conductivity. Coulombic scattering can occur due to charged dislocations and remote (surface) charged states ($N_{surf} \sim N_s$ by charge neutrality) [9]. At room temperature, scattering from polar

optical phonons dominates over all other scattering processes and interface roughness scattering has been found to be dominant at low temperatures [9].

2.2.2 Current-voltage relationship of HEMT

In an AlN/GaN HEMT the electrons flowing between the source and drain ohmic contacts, through the highly conductive 2DEG channel, are controlled by the Schottky gate contact. A schematic drawing of the AlN/GaN HEMT is shown in Fig 2.4. When a voltage V_{ds} is applied to the drain electrode with the source electrode grounded, a current I_{ds}, whose magnitude depends on the total resistivity of the 2DEG channel, flows between the two electrodes. The gate electrode, by acting on the 2DEG density below it with the application of voltage V_{gs}, modulates the channel resistivity and thus I_{ds}. Typically, the gate is placed asymmetrically and shifted away from the drain side to obtain low source resistance, R_s, and reduce the peak of the electric field which occurs at the gate end towards the drain at high V_{ds} values [1], and can have detrimental effects on the devices breakdown characteristics.

Keeping in mind that the drain current I_{ds} must be constant throughout the channel and if we do not consider any field dependence of μ, to simplify analysis for a basic understanding of the current-voltage characteristics, I_{ds} may expressed by [1]

$$I_{ds} = \sigma_n(x)Wv(x) = \sigma_n(x)WE(x)\mu \tag{2.11}$$

where x is the direction along the channel, $\sigma_n(x)=eN_s(x)$ is the 2DEG charge per unit area, v is the velocity, W is the gate width. For long channel transistors (long gate length) and/or for very small V_{ds} we can assume that the channel voltage V(x) varies along the channel, from 0 to V_{ds}. N_s is a function of the distance x, along the channel, and thus [1]:

$$\sigma_n(x) = eN_s(x) = \frac{\varepsilon}{d + \Delta d}\{(V_{gs} - V_{th} - V(x)\} \tag{2.12}$$

where d is the barrier thickness and Δd is the effective distance of the 2DEG from the heterointerface. With the contribution of Eq. 2.12, Eq. 2.11 becomes

$$I_{ds} = \frac{W\varepsilon E(x)\mu}{d + \Delta d}\{(V_{gs} - V_{th} - V(x)\} \tag{2.13}$$

Considering that $E(x) = dV(x)/dx$ Eq. 2.13 is given by [1]

$$I_{ds} = \frac{W\varepsilon\mu}{d + \Delta d}\{(V_{gs} - V_{th} - V(x)\}dV(x)/dx \tag{2.14}$$

By integrating this equation over the gate length L_g, from the source to the drain, and keeping in mind that $V(x=0)=0; V(x=L_g)=V_{ds}$ we obtain a relation between I_{ds} and V_{ds} :

$$I_{ds} = \frac{W\varepsilon\mu}{L_g(d + \Delta d)}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] = \beta_d\left[V_{geff}V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{2.15}$$

where $V_{geff} = V_{gs} - V_{th}$ and $\beta_d = \frac{\mu W\varepsilon}{L_g d}$

In a field effect transistor, V_{ds} produces a lateral field. The current saturates when V_{ds} is increased to the point where the field in the channel exceeds its critical value thereby causing the velocity to saturate [1]. In the saturation region the drain current is given by:

$$I_{dss} = eWv_{sat}N_s = \frac{\varepsilon W v_{sat}}{d + \Delta d}\left(V_{gs} - V_{th} - V_{dss}\right) = \beta_d V_0\left(V_{geff} - V_{dss}\right) \tag{2.16}$$

where V_{dss} is the saturation drain voltage, I_{dss} is the saturation current, $V_0 = v_{sat}L_g/\mu$, and v_{sat} the saturation velocity. For AlGa/GaN devices Δd can be neglected because the maximum of the 2DEG is typically 2-4 nm from the interface, which is smaller than the thickness of the barrier layer, typically greater than 20 nm [1]. However, this is not valid in the case of AlN/GaN HEMTs. The above analysis is known as the two-piece model, implying that an abrupt transition occurs from the constant mobility region to the constant velocity region [1], where μ assumed to be constant and independent of the electric field E. At high electric fields, carriers fail to follow this model due to the velocity saturation effect [1]. A more precise analysis of the HEMT operation can be obtained if a smoother transition is assumed allowing the use of a phenomenological velocity-field relationship. In this approach, the peak in the velocity-field plot is neglected and Si-like velocity-field characteristics are assumed [1]. In that case:

$$v = \frac{\mu E(x)}{1 + \mu E(x)/v_{sat}} = \frac{\mu E(x)}{1 + E(x)/E_c} \tag{2.17}$$

where μ the low field mobility and $E_c = v_{sat}/\mu$ is the electric field in the saturation point.

By using:

$$I_{ds} = \frac{W\varepsilon v(x)}{d}\left(V_g - V_{th} - V(x)\right) \tag{2.18}$$

and by substituting Eq. 2.17 in Eq. 2.18:

$$I_{ds} = \frac{W\varepsilon\mu v_{sat}}{d}\left[\frac{\frac{dV(x)}{dx}}{v_{sat} + \frac{\mu dV(x)}{dx}}\{V_g - V_{th} - V(x)\}\right] \tag{2.19}$$

By integrating Eq. 2.19 from the source end (x=0) of the channel to the drain end (x=L):

$$I_{ds} = \frac{W\varepsilon\mu v_{sat}}{d}\left[\frac{V_{geff}V_{ds} - \frac{V_{ds}^2}{2}}{v_{sat}L_g + \mu V_{ds}}\right] = \frac{1}{1 + \frac{\mu V_{ds}}{v_{sat}L_g}}\left\{\frac{\mu W}{L_g}\frac{\varepsilon}{d}\left[\left(V_g - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2}\right]\right\} \tag{2.20}$$

It can be noticed that for large values of L_g or small values of V_{ds} or when the saturation velocity approaches infinity, Eq. 2.20 is simplified to Eq. 2.15 which is valid when the mobility is constant and for long channel transistors (L_g>1 µm). For short channel devices (small gate lengths) the current is smaller than what would be expected due to the velocity saturation effect.

When the transistor operates as an amplifier, an estimation of the maximum power density can be obtained through the relationship [1] $P_{max} = I_{max} * (V_{br} - V_{knee})/8$, where V_{br} is the breakdown voltage and I_{max} and V_{knee} are the maximum current density and the knee voltage values, respectively, based on the values measured at DC (Fig. 2.5). Thus, a high power density is obtained if V_{br} is high and if the on-resistance is minimized in order to have a low V_{knee} value. It is noted that a high N_s value is also desirable because it translates to a high I_{max}.

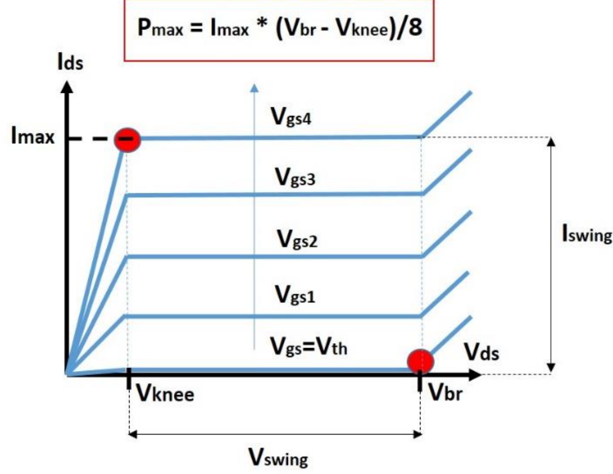


Fig. 2.5 Schematic of I_{ds}-V_{ds} characteristics of a HEMT with basic parameters defined in the graph. The maximum output current I_{max}, the knee voltage V_{knee} and the breakdown voltage V_{br} may be used to estimate the maximum output power P_{max} when the transistor operates as an amplifier.

2.2.3 Transconductance and parasitic resistance

The transconductance is an important parameter in HEMTs and is defined by $g_m = \partial I_{ds} / \partial V_{gs}$ at a fixed value of V_{ds}. The extrinsic (measured) $g_{m(ext)}$ is always smaller than the intrinsic transonductance $g_{m(int)}$ due to the effect of source series resistance [10] as explained in the following. Suppose that the HEMT has a parasitic source-drain series resistance $R_{sd}=R_s+R_d$ where $R_s = R_c + R_{s(a)}$, $R_d = R_c + R_{d(a)}$, R_c is the contact resistance of the source/drain electrode and $R_{s(a)}$, $R_{d(a)}$ are the access resistances of the gate-to-source and gate-to-drain channel regions, respectively. The differential of the drain-source current dI_{ds} is given by [10]

$$dI_{ds} = \left(\frac{\partial I_{ds}}{\partial V'_{gs}}\right)|_{V'_{ds}} dV'_{gs} + \left(\frac{\partial I_{ds}}{\partial V'_{ds}}\right)|_{V'_{gs}} dV'_{ds} = g_{m(int)} dV'_{gs} + g_{d(int)} dV'_{ds} \quad (2.21)$$

where $g_{d(int)} = \frac{\partial I_{ds}}{\partial V'_{ds}}$ is by definition the intrinsic drain conductance and V'_{gs} , V'_{ds} are the internal effective voltages:

$$V'_{ds} = V_{ds} - R_{sd} I_{ds} \quad (2.22)$$

$$V'_{gs} = V_{gs} - R_s I_{ds} \tag{2.23}$$

At constant V_{ds} (i.e., $dV_{ds}=0$)

$$dV'_{ds} = -R_{sd} dI_{ds} \tag{2.24}$$

$$dV'_{gs} = dV_{gs} - R_s dI_{ds} \tag{2.25}$$

By substituting Eqs. (2.24) and (2.25) into Eq. (2.21)

$$\boldsymbol{g_{m(int)} = \frac{(1 + R_{sd} g_{d(int)}) g_{m(ext)}}{1 - R_s g_{m(ext)}}} \tag{2.26}$$

where the extrinsic (measured) transconductance is

$$g_{m(ext)} = \left(\frac{\partial I_{ds}}{\partial V_{gs}}\right)|_{V_{ds}}$$

Similarly, it can be shown [10] that

$$g_{d(int)} = \frac{(1 + R_s g_{m(int)}) g_{d(ext)}}{1 - R_{sd} g_{d(ext)}} \tag{2.27}$$

where $g_{d(ext)} = \left(\frac{\partial I_{ds}}{\partial V_{ds}}\right)|_{V_{gs}}$ is the measured (extrinsic) drain conductance.

When the measured drain conductance $g_{d(ext)}$ becomes zero (in saturation), Eq. (2.26) yields

$$\boldsymbol{g_{m(int)} = \frac{g_{m(ext)}}{1 - R_s g_{m(ext)}}} \tag{2.28}$$

Typically, in GaN-based devices $R_c >> R_{a(s)}$ [11] which means $R_s \approx R_c$. This approximation has a higher validity in AlN/GaN HEMTs due to the very low sheet resistances and high contact resistances in these devices [11]. Moreover, $g_{m(ext)}$ can be expressed as follows [11]

$$g_{m(ext)} = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}}(eN_s v) = e\left(v \frac{\partial N_s}{\partial V_{gs}} + N_s \frac{\partial v}{\partial V_{gs}}\right) \tag{2.29}$$

By taking into account that $\sigma_n = eN_s = C_g V$ it can be obtained that $e\partial N_s/\partial V = C_g$, where C_g is the "intrinsic" gate capacitance. Therefore, in the velocity saturation region, the transconductance is directly proportional to the gate capacitance and is given by:

$$g_m = ev_{sat}\frac{\partial N_s}{\partial V_{gs}} = ev_{sat}C_g \tag{2.30}$$

Transconductance has a strong dependence on the gate voltage, as will be demonstrated in chapter 4. It has been proposed that the non-linear increase in the differential source access resistance (defined as dV_{gs}/I_{ds}) is the cause for the decrease in transconductance with increase in drain current (or equivalently, when increasing the gate voltage) [12]. Palacios et al. [12] showed, by simulating the electric field in the source access region for different gate voltages, that an early or "quasi-saturation" occurs in nitride-based structures that causes a reduction in the electron mobility which translates into an increase in the differential access resistance [12]. The origin for the quasi-saturation in the electron velocity profile is generally related to the high optical phonon energy in nitride-based semiconductors, which is much lower in other semiconductors, like Si or GaAs, and this early saturation cannot be distinguished from the standard saturation [12].

2.2.4 Breakdown voltage

Many different physical effects are limiting the power performance of GaN-based HEMTs. The most important GaN-related breakdown mechanisms have been discussed in detail in the book of F. Medjdoub and K. Iniewski [13]. The breakdown voltage of GaN devices is usually defined as the voltage level at which the drain current of pinched-off transistors exceeds a normalized value of 1mA per millimeter of device width [13]. V_{br} depends on many parameters, such as the epitaxial design of the buffer layer, its material quality and the lateral geometrical design of the devices. Specifically, short gate lengths and short gate-drain distances reduce V_{br} as a consequence of the increase of the peak electric field at the drain side of the gate [13]. Thus, transistors designed for operation at high frequencies (which require short gate lengths) can reach lower power densities when compared to the ones operating at lower frequencies [13]. Usually, the maximum operation voltage is limited by excessive gate or drain leakage currents, which may origin from several technological issues. Leakage current originating from the gate usually concerns leakage through the Al(Ga)N barrier [13,14], strain-induced leakage [13,15] and/or surface leakage, which may be

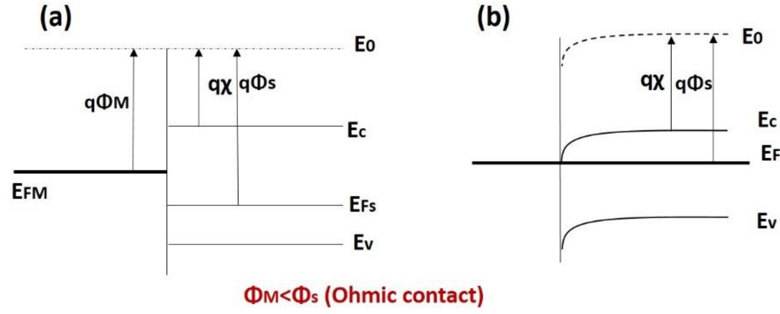


Fig. 2.6 Energy-band diagrams of metal-semiconductor contact for n-type semiconductor, for the case $\Phi_M<\Phi_S$ where an ohmic contact is formed. (a) corresponds to separate metal and semiconductor, while (b) gives the thermal equilibrium energy band diagram.

---

introduced when a passivation layer is adopted to alleviate the surface-state-induced current collapse problem [13,16]. The punch-through short channel effect [13,17] can substantially increase subthreshold leakage current. In this case, even at low drain voltages and closed-channel conditions, electrons are bypassing the gate control region via the buffer [13,17,18]. In standard GaN devices, where a GaN buffer layer is adopted, there is an insufficient confinement to the bottom side which may give rise to this punch-through phenomenon. If high leakage paths are suppressed through proper technological advancements, the breakdown voltage of GaN-based HEMTs scales with increasing gate to drain distance, d_{gd} [13]. Therefore, d_{gd} defines the highest HEMT voltage operation.

2.2.5 Ohmic and Schottky contacts

a) Ohmic contacts

By definition, an ohmic contact is defined as a metal-semiconductor contact that has a negligible junction resistance relative to the total resistance of the semiconductor device [19]. The work function Φ of a crystal is defined as the energy required to remove an electron from the Fermi level to the vacuum level E_0, respectively. In the case of n-type semiconductor, and for an ideal ohmic contact, the work function of the semiconductor should be greater than the work function of the metal ($\Phi_S > \Phi_M$) (Fig. 2.6).

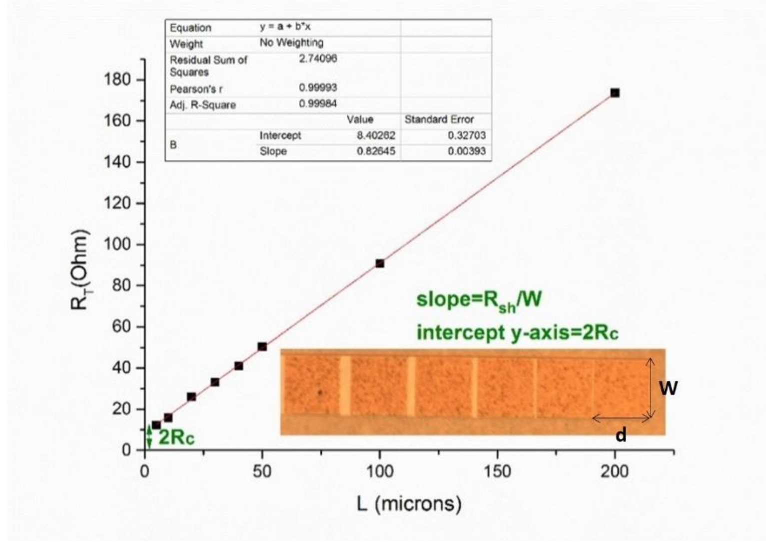


Fig. 2.7 Total resistance R_T plot with TLM pad spacing for an AlN/GaN HEMT structure. Inset shows an optical microscope image of a TLM pattern.

The transmission line model (TLM) method is commonly used to assess the quality of the ohmic contacts, as well as the electrical properties of the structure [20]. An optical microscope image of a TLM test pattern is shown in the inset of Fig. 2.7. It consists of rectangular metal contact pads with increasing spacing between them, L, while W is the contact pad width, d is the contact pad length. The total resistance, R_T, is given by [20]

$$R_T = \frac{2R_{sh1}L_T}{W} + R_{sh2}\frac{L}{W} = 2R_c + R_{sh2}\frac{L}{W} \tag{2.31}$$

where R_c is the contact resistance, R_{sh1} and R_{sh2} the semiconductor sheet resistance under the contact pads and between the contact pads, respectively, and L_T is the transfer length which refers to the distance across which most of the current transfers into the contact pads from the semiconductor and vice versa [20]. By the assumption that the deposition of the metal does not change the sheet resistance of the semiconductor: $R_{sh1}=R_{sh2}=R_{sh}$, Eq. 2.31 becomes

$$R_T = \frac{2R_{sh}L_T}{W} + R_{sh}\frac{L}{W} = 2R_c + R_{sh}\frac{L}{W} \tag{2.32}$$

where $R_c = R_{sh}L_T/W$. By plotting R_T as a function of L, a linear fit to the data can be obtained as shown in Fig. 2.7. The slope of the line gives the value of R_{sh}/W and the intercept with y-axis gives the value of $2R_c$. It should be noted that the value of R_c is independent of the contact length d, and only depends on its width i.e. only on the dimension perpendicular to the current flow. In order to normalize the contact resistance, the value of R_c is multiplied with W to obtain a value in Ohm.mm.

As far as it concerns the contact metal scheme in Al(Ga)N/GaN structures, the most popular metallization is based on the Ti/Al/Ni/Au system [21-23]. The first explanation for the formation of ohmic contact on Al(Ga)N or GaN by annealing a Ti/Al/Ni/Au metallization is based on the formation of a TiN alloy at the interface, which leaves in the III-Nitride an excess of N-vacancies that provide a highly n-doped region underneath the metal contact [21-23]. Al reacts with Ti and forms an Al_3Ti layer that prevents oxidation of the underlying Ti metal [23] and helps in contact formation. It also reacts with the semiconductor to form AlN, resulting in N vacancies, which contribute to the increase of n-type doping in the underlying semiconductor, enabling electrons to tunnel easily to the 2DEG [24].

The second explanation of ohmic contact formation with Ti/Al/Ni/Au deposition approaches the subject from the standpoint of differences in work functions between the metal and semiconductor [21]. Taking into account that the work function of GaN is 4.1 eV, very close to that of Al, the Al-containing contacts should be ohmic due to the low barrier between the two materials. Researchers in the recent years, supported the first explanation since cross sectional TEM has shown the formation of TiN alloyed layers and spiking at the contact-semiconductor annealed interface [25, 26].

Ni (or Pt, Ti, Mo) is used to avoid the Au indiffusion and the Al outdiffusion and the intermixing between Al and Au, and Au is used to protect from oxidation the Ti and Al metals during high annealing temperatures and to improve the ohmic contacts conductivity [27].

While the metallization combination is important, another issue in ohmic contact formation is the thickness of the AlN barrier the metal stack should penetrate during annealing. In Ga-polar III-Nitrides the thickness of the barrier is proportional to the 2DEG density. This means that the barrier must be thick enough to create the 2DEG, and on the other hand at the same time the barrier should be thin enough for sufficient metal diffusion to occur at high annealing temperatures to contact the

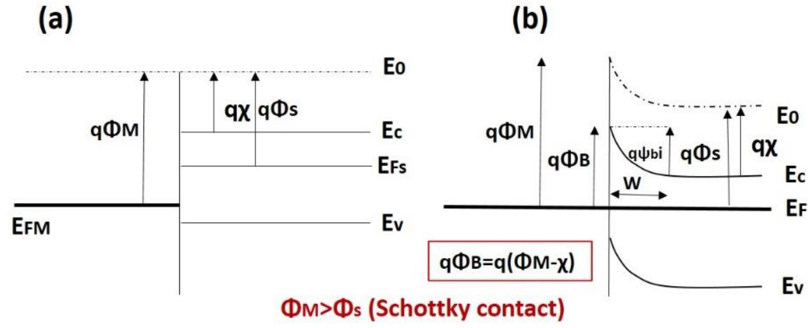


Fig. 2.8 Energy-band diagrams of metal-semiconductor contact for n-type semiconductor, for the case $\Phi_M>\Phi_S$ where a Schottky contact is formed. (a) corresponds to separate metal and semiconductor, while (b) gives the thermal equilibrium energy band diagram.

2DEG [11]. In the case of AlN, the barrier is much thinner than AlGaN but it also has a much wider bandgap (stronger atomic bonds) making the anneal-diffusion of the contact metals a more difficult case.

b) Schottky contacts

The Schottky contact, the gate electrode in HEMT, is formed when a metal with work function greater than the semiconductor ($\Phi_M > \Phi_S$) contacts the respective semiconductor as shown in Fig. 2.8. Unlike the case of ohmic contacts, the gate metals are not annealed in order to form the barrier. Under equilibrium, a barrier height, $\Phi_B=\Phi_M-X$, according to the ideal theory, forms for electrons to flow from metal to semiconductor. Thus, the barrier height depends both on the metal work function as well as on the electron affinity X of the semiconductor. A high Φ_B associated with a low reverse leakage current is an essential condition for high power radio frequency applications. The commonly used metal combination for Schottky contacts in Al(Ga)N/GaN HEMTs is a Ni/Au metal stack due to the highest work function (~5.15 eV) compared to other metals. The electron affinity, X, of $Al_xGa_{1-x}N$ decreases with increasing Al content (mole fraction x) [28]. Therefore, the barrier height of a metal on (Al)GaN should increase with increasing Al content of the barrier layer. However, the Schottky barrier in III-Nitrides, as it is usually for many semiconductors, is mainly defined by Fermi level pinning at the surface due to a high density of surface states [6]. In the presence of Fermi-level pinning, the barrier height is given by $\Phi_B=S(\Phi_M- \Phi_s) + (\Phi_s - X)$, where

S is the pinning factor (0<S<1) and Φ_s is the pinning energy at the semiconductor surface in reference to the vacuum level [29]. S=0 describes the case of strong pinning, while S=1 denotes the absence of pinning. The Fermi level pinning typically results in a fixed Φ_B, independent of the used gate metal.

The low conductivity of AlN layers and the formation of 2DEG complicates the analysis of I-V measurements for the extraction of Schottky barrier height on AlN. In AlN/GaN structures the analysis of the I-V curve is inadequate since the leakage current consists not only of thermionic emission current but also of tunneling and/or other residual leakage currents [29,30]. Up to now, there are no reports on measured Schottky barrier heights of AlN/GaN structures. A surface potential (or surface barrier height, given by the position of the surface Fermi level, relatively to the conduction band minimum) of ~1.9 eV, independent of the AlN barrier layer thickness, has been reported [30] which is an evidence of Fermi level pinning; however, the Schottky barrier may be different than the barrier on the free AlN surface [30]. Non-published experimental results in our lab for Al-rich AlGaN and InAlN compounds suggest a Schottky barrier height close to 3.0 eV. This barrier height has been assumed in charge control modeling of the AlN/GaN HEMT structures by self-consistent solution of the Poisson and Schrodinger equations and resulted to a good agreement with the experimental measured N_s of the 2DEG.

2.3 Metal-Insulator-Semiconductor Capacitors

A brief analysis on the characteristics and operation of the metal-insulator-semiconductor capacitor (MISCAP), for an ideal n-type semiconductor ($n \approx N_d$, N_d is the doping carrier concentration), will be followed, which is the most useful device in the study of semiconductor surfaces. A comprehensive and in-depth analysis of the MOS capacitor can be found in many well respected texts [19,31,32].

2.3.1 Ideal MIS Capacitor

The ideal MISCAP is shown in Fig. 2.9 and has the following characteristics [19]: (a) The only charges that are present in the structure under any applied bias are those in the semiconductor and those on the metal surface adjacent to the insulator, with an equal but opposite sign; this means that it is assumed that no interface trap nor any kind of oxide charge exists; (b) When a dc bias is

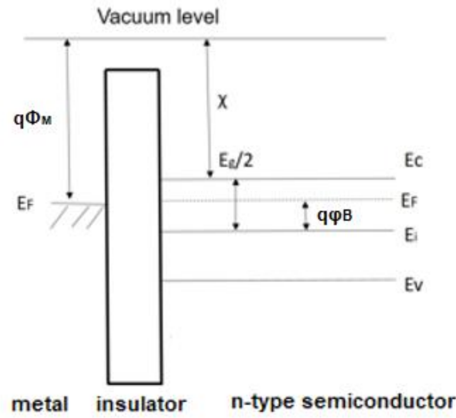


Fig. 2.9 Energy-band diagram of ideal MIS capacitor at equilibrium (V= 0) for n-type semiconductor. The difference between the metal work function Φ_M and the semiconductor work function was assumed to be zero (Φ_{MS}= 0). Adapted from *Physics of semiconductor devices - S.M. Sze* (ref. [19]).

---

applied, there is no carrier transport through the insulator or the resistivity of the insulator is infinite. The difference between Φ_M and the semiconductor work function Φ_{MS} (or ideal flat band voltage V_{FB}) is given by [19] (Fig. 2.9):

$$\Phi_{MS} = \Phi_M - \left(X + \frac{E_G}{2q} - \varphi_B\right) = \Phi_M - [X + \left(\frac{E_C - E_F}{q}\right)] \tag{2.33}$$

where φ_B is the bulk potential given by [19]

$$E_F - E_i = kT\ln(N_d/n_i) = q\varphi_B \tag{2.34}$$

n_i is the semiconductor intrinsic carrier concentration (for GaN n_i=2 x 10^{-10} cm^{-3}). E_i is the intrinsic Fermi level which is always parallel to both E_c and E_v, everywhere in the semiconductor. Now, if a positive voltage (V > 0) is applied to the metal plate, the conduction-band edge E_c, bends downwards near the surface and is closer to the Fermi level (Fig. 2.10). For an ideal MISCAP, no current flows in the structure (or $dE_F/dx = 0$), so E_F remains flat in the semiconductor [19].

Since the carrier density depends exponentially on the energy difference ($E_c - E_F$), this band bending causes an accumulation of electrons near the semiconductor surface. This is the accumulation condition. In the depletion case, when a negative voltage (V<0) is applied, the bands

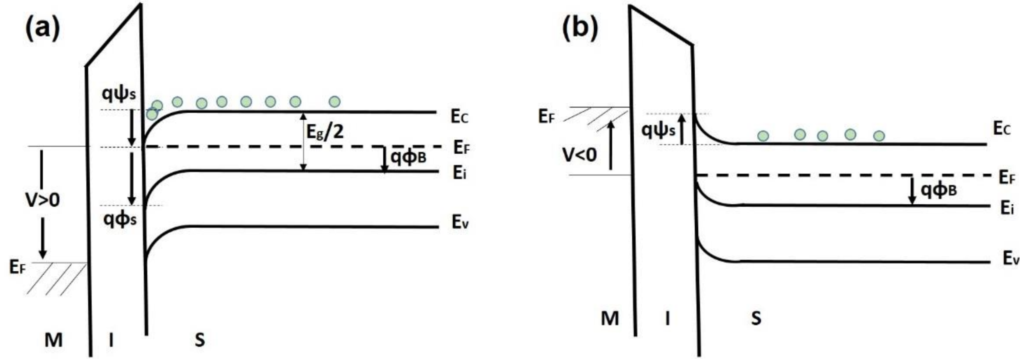


Fig. 2.10 Energy-band diagrams for an ideal MIS capacitor. (a) When V > 0 the metal fermi-energy is lowered (E=-qV) and the capacitor is under accumulation, and (b) when V < 0 the metal fermi-energy is raised (E=-qV) and the capacitor is under depletion. Adapted from *Physics of semiconductor devices - S.M. Sze* (ref. [19]).

---

bend upward, and the electrons are depleted (Fig. 2.10). The inversion characteristic can be expected when a large negative voltage is applied. In that case, the energy bands would bend upwards furthermore, so that the intrinsic level at the surface would cross over the Fermi level. As a result, the concentration of minority carriers (holes) would be larger near the semiconductor surface. However, the formation of surface inversion is impossible in wide gap semiconductors due to the extremely low generation rate of holes at room temperature [33], and typically the deep-depletion behavior (in the highly negative bias region) is observed.

2.3.2 Interface traps

In real MISCAPs, interface traps exist affecting significantly the ideal MISCAP characteristics. Interface traps of density D_{it} and trapped charge Q_{it}, located at the insulator/semiconductor interface with trap states within the semiconductor forbitten bandgap, can be charged or discharged, depending on the surface potential [19]. Thus, unlike fixed charge, interface trapped charge is in electrical communication with the underlying semiconductor and its amount is bias dependent. Q_{it} is present in the forbidden bandgap due to the interruption of the lattice structure at the surface of a crystal (defects caused by bond breaking processes), structural defects, oxidation-induced defects and metal impurities [19,32]. The donor-type interface states filled with electrons

are neutral and become positively charged by giving up electrons, while acceptor-type interface traps are neutral when they are empty and become negatively charged when they are filled with electrons. In the case of MIS-HEMTs, a high amount of acceptor-like interface traps existing close to the insulator/semiconductor interface may cause a serious problem in device operation, since such interface traps can result in Fermi level pinning under the gate and the gate voltage may not be able to modulate sufficiently the overwhelming charge densities (2DEG density plus interface trap state density) [11].

2.3.3 Insulator charges

Insulator charges, other than interface trapped charge, include (a) the fixed insulator charge, (b) the insulator trapped charge and (c) mobile ionic charge [19,32]. The fixed insulator charge is generally a positive charge, located very near the semiconductor-insulator interface and is considered to be at that interface. Its density is not greatly affected by the insulator thickness but it depends on deposition conditions [19]. Fixed charge is stable and immobile under an applied electric field [32]. The insulator trapped charge (may be positive or negative), may be distributed inside the insulator layer and exists due to carriers trapped in the insulator. Trapping may result from avalanche injection, Fowler-Nordheim tunneling, or any current passing through the insulator [19,32]. The mobile ionic charge, which may be distributed throughout the insulator, is mainly caused by mobile positive ions of Na^+, K^+, in the case of silicon dioxide, and possibly H^+. Negative ions and heavy metals may also contribute to this charge [32].

2.3.4 Flat-band voltage

The flat-band voltage is determined by the metal-semiconductor work function difference Φ_{MS} and the various insulator charges through the relationship [32]

$$V_{FB} = \Phi_{MS} - \frac{Q_{it(\psi_s)}}{C_{ins}} - \frac{Q_f}{C_{ins}} - \frac{1}{C_{ins}}\int_0^d \frac{x}{d}\rho(x)\,dx \qquad (2.35)$$

where d is the insulator thickness, Q_f is the fixed trapped charge and $\rho(x)$ is the charge density (per unit volume) from trapped and mobile charge, which may be distributed throughout the insulator. Q_{it} is designated as $Q_{it}(\psi_s)$, because the occupancy of the interface trapped charge depends on the surface potential ψ_s [32]. It should be noted that the intrinsic energy level E_i (which is everywhere

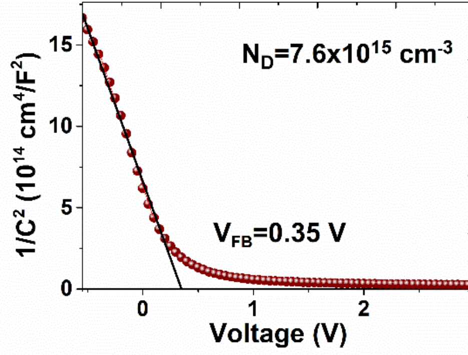


Fig. 2.11 $1/C^2$ vs bias voltage plot showing the extraction of flat band voltage of a SiN_x/GaN MISCAP device at f = 1 MHz.

---

parallel to E_c and E_v) in the neutral part of the device is taken as the zero reference potential and the surface potential ψ_s is measured from this reference level [32]. The effect of charges on V_{FB} depends on the location of the charge. When the charge is located at the insulator-semiconductor interface, the effect on V_{FB} is greatest because then it images all of its charge in the semiconductor [32]. On the other hand, when the charge is located at the gate-insulator interface, it images all of its charge in the gate and has no effect on the flat-band voltage [32].In the case of MISCAPs where a III-Nitride is studied, the spontaneous polarization along the $[000\bar{1}]$ direction leads to a negative-bound surface charge P_{sp} (≈ -1.8 x 10^{13} cm^2 for Ga-face GaN) which should be included in Eq. (2.35) [33]. Thus, by assuming negligible insulator-trapped charge and mobile charge, Eq. (2.35) is given by [33,34]

$$V_{FB} = \Phi_{MS} - \frac{Q_{it(\psi_s)} + Q_f + P_{sp}}{C_{ins}} = \Phi_{MS} - \frac{Q_{eff}}{C_{ins}} \quad (2.36)$$

where Q_{eff}, is the total (or effective) charge at the insulator/III-nitride interface. To calculate Q_{eff} from Eq. (2.36) the experimental V_{FB} should be calculated from the C_{FB} value given by [19]

$$C_{FB} = \frac{1}{C_{ins}} + \frac{1}{C_{d(FB)}} \quad (2.37)$$

where $C_{d(FB)} = \varepsilon_s\varepsilon_0/L_D$, is the capacitance of the semiconductor depletion layer at flat-band condition (ψ_s=0), ε_s is the permittivity of the semiconductor and L_D is the extrinsic Debye length

$$L_D = \left(\frac{\varepsilon_s \varepsilon_0 kT}{q^2 N_d}\right)^{\frac{1}{2}} \quad (2.38)$$

Another way to determine V_{FB} experimentally is to plot $1/C^2$ versus V, measured at a high frequency, as shown in Fig. 2.11, where the lower knee of this curve occurs at $V=V_{FB}$ [32].

By taking into account that $C_{ins}=\varepsilon_0\varepsilon_{ins}/d$ (ε_0 and ε_{ins} are the vacuum permittivity and dielectric constant, respectively), Eq. (2.36) yields

$$V_{FB} = \Phi_{MS} - \frac{Q_{eff} d}{\varepsilon_0 \varepsilon_{ins}} \quad (2.39)$$

Thus, for a given interfacial charge density, the flatband voltage is reduced as the insulator capacitance increases, i.e., for thinner oxides. Hence, oxide charges usually contribute little to flat-band or threshold voltage shifts for MIS devices with thin insulators [32].

2.3.5 Charge conduction mechanisms

In the case of an ideal MISCAP, the conduction of the insulator is assumed to be zero. However, a real insulator may exhibit some degree of charge conduction when an electric field is applied. An estimation of the electric field in an insulator under bias is given by $E_i \approx E_s (\varepsilon_s/\varepsilon_i) \approx V/d$, where E_i, E_s are the electric fields in the insulator and the semiconductor, respectively, and ε_s, ε_i are the corresponding permittivities [19]. This equation assumes that oxide charges are negligible and that V_{FB} and the semiconductor band bending ψ_s are small compared to the applied bias voltage.

The following is foced to the electrical conduction mechanisms of silicon nitride (SiN_x) dielectric which comprises a significant part of this research work. The electrical conduction of SiN_x may be divided into three components: $I=I_1+I_2+I_3$, [19,35] where

$$I_1 = C_1 E exp\left\{-\frac{q\left[\varphi_1 - \left(\frac{qE}{\pi\varepsilon_0\varepsilon_d}\right)^{\frac{1}{2}}\right]}{kT}\right\} \quad (2.39)$$

$$I_2 = C_2 E^2 \exp(-E_2/E) \quad (2.40)$$

$$I_3 = C_3 E \exp(-\frac{q\varphi_3}{kT}) \quad (2.41)$$

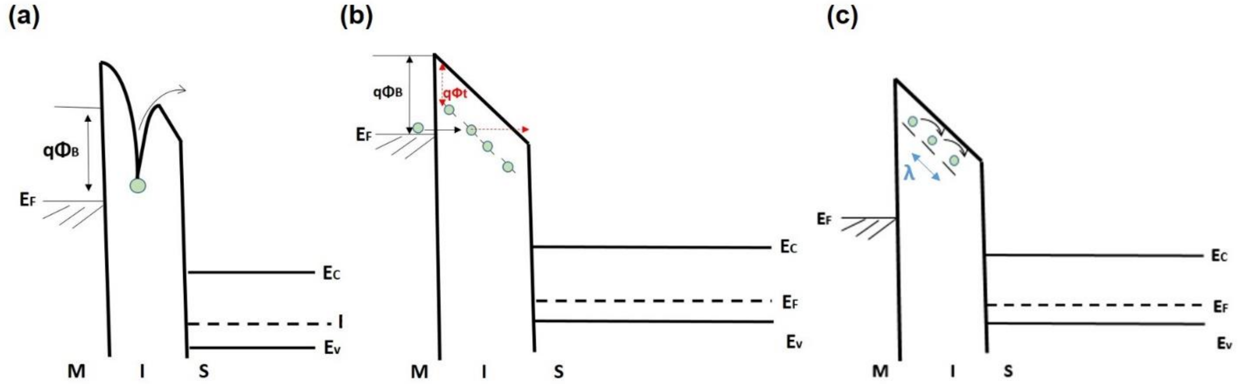


Fig. 2.12 Energy band diagrams exhibiting the basic conduction mechanisms (a) Poole-Frenkel emission, (b) field emission tunneling and (c) ohmic (hopping) conduction. When the insulator has a non-negligible number of traps, the tunneling emission is prevailed by field ionization of trapped electron into the conduction band of the insulator [19,36,37]; in that case, the measured barrier height Φ_B is lower than the ideal (theoretical) expected value and Φ_B may be replaced by the trap barrier height Φ_t [36,37].

The process described by Eq. (2.39) is known as the Poole–Frenkel (PF) effect and is due to field-enhanced thermal emission of trapped electrons into the conduction band of the SiN_x (Fig. 2.12). E is the electric field, q is the electron charge, φ_1 the depth of the trap potential well, ε_d is the dynamic electric constant, and C_1 a proportionality constant [35]. The PF emission is somehow like an internal Schottky emission. Considering an electron in a trapping center, the barrier height for the electron emission from the trap state equals to the trap energy level without an external electric field. With an external electric field applied, the Coulomb potential energy can be reduced by a mechanism similar to that of the Schottky effect in the thermionic emission, which results in a lower potential barrier height for an electron being thermally excited out of the traps into the conduction band [19,35].

The second component I_2 is associated with field emission of electrons tunneling from trap centers in the dielectric [19,35], or by electrons tunneling from the metal Fermi energy into the insulator conduction band [19], (Fig. 2.12). C_2 is a function of effective mass m* and the barrier height Φ_B and $E_2=8\pi(2m^*)^{1/2}(\Phi_B)^{3/2}/3hq$, where h is the Planck's constant. When the insulator has a non-negligible number of traps, the tunneling emission is prevailed by field ionization of trapped

electron into the conduction band of the insulator [19,36,37]; in that case, the measured barrier height Φ_B is lower than the ideal (theoretical) expected value and Φ_B may be replaced by the trap barrier height Φ_t [36,37].

I_3 corresponds to ohmic current conduction, under low electric fields (low voltages), by hopping of thermally excited electrons from one isolated (localized) state to another [35]. C_3 is a constant and $q\varphi_3$ is the activation energy. When the mean hopping distance λ (the spacing between trap sites) for electrons is short (Fig. 2.11), the thermal activation energy $q\varphi_3$ is small, and the movement of electrons from one occupied trap state to another is frequent [38]. On the other hand, when σ is large, $q\varphi_3$ is high, and the hopping probability from one localized state to another is low. Generally, larger hopping distances for electrons in the dielectric means larger increase in the thermal activation energy for hopping to occur and lower ohmic currents [38].

2.4 Literature summary for III-nitride HEMTs

In 1992, the first observation of a 2DEG was reported for an AlGaN/GaN heterojunction with a carrier concentration of the order of 10^{11} cm^{-2} and a room temperature mobility of 400–800 cm^2/Vs [39]. The first DC performance of AlGaN/GaN HEMT was exhibited in 1993 with a saturation drain current of 40 mA/mm [40]. Nowadays, an enormous progress has been made in the growth of nitride materials and after intensive GaN technological advancements, researchers managed to reach carrier concentrations of the order of 10^{13} cm^{-2} and high breakdown voltages of over 2 kV [41-46], exploiting GaN's high critical electric field of over 3 MV cm^{-1}, which is a direct consequence of its 3.4 eV wide bandgap. Although AlGaN/GaN HEMTs have been established as the best candidate for microwave power applications, the significant drop of the 2DEG carrier density with the decrease of AlGaN barrier thickness prevents to benefit from ultrashort gate lengths in order to boost GaN-based device frequency of operation. In that case, AlN barrier can be used because the higher polarization effect resulting from the AlN barrier can compensate the decrease of 2DEG density caused by the barrier thinning [11]. Furthermore, the AlN barrier allows transport without alloy scattering and can enhance the transconductance, as well as, decrease the short-channel detrimental effects [11]. Therefore, AlN/GaN HEMTs can be ideal candidates for high frequency GaN-based devices.

2.4.1 Overview of the AlN/GaN heterostructure system

The study of the AlN/GaN heterostructure system began back in the 1990's [47-50]. However, high quality AlN/GaN structures utilizing thin (d < 50Å) AlN layers with relatively high electron mobilities were first reported in 2000 by Smorchkova [4]. In the next years, with the advanced improvement in AlN/GaN material growth and device process technology, outstanding record performances for both the 2DEG structures and HEMT devices have been demonstrated. The AlN barrier thickness range was defined between 2-5 nm by the lack of 2DEG formation at the low limit and strain relaxation, which led to cracking of the AlN barrier and mobility degradation, at the high limit [4,51,52]. Adikimenakis et al. reported a critical AlN thickness of 5 nm, beyond which microcracking occurs, deteriorating the electrical characteristics of the 2DEG [52]. AlN/GaN HEMT structures exhibited a 2DEG density and mobility of 3.6×10^{13} cm^{-2} and 1200 cm^2/Vs, respectively, and 1 μm gate length transistors reached a current density of 1.8 A/mm [52]. In 2015, Y. Tang et al exhibited deeply-scaled devices with maximum drain currents over 3 A/mm and impressive high f_t of 454 GHz and simultaneous f_{max} of 444 GHz on a 20-nm gate AlN/GaN HEMT with 50-nm gate-source and gate-drain separation [53]. However, this achievement which has been primarily accomplished through both vertical and lateral dimension scaling generally suffered from a low breakdown voltage of 10 V due to the extremely high electric field near the gate [53].

2.4.2 InN-based heterostructures background

InN has been suggested as a channel material for future ultrahigh speed transistors that would boost performance over GaN-based devices and pave the way for terahertz frequency electronics [54,55]. During the last years, a number of extensive studies on the heteroepitaxial growth of InN films by Plasma-Assisted MBE and their structural and optoelectronic properties have been reported by the Microelectronics Research Group of University of Crete and FORTH [56-68] and others [69-72]. The understanding of the physical mechanisms of MBE growth permitted the realization of structurally optimized InN layers, and important material properties such as the α and c lattice parameters have been determined [67]. However, a number of impediments related to material issues has prevented the development of any kind of device applications, despite the recent improvements.

One of the key issues that needs to be resolved is the inability to control the surface conductivity of InN. Fermi-level pining within the conduction band and an intrinsic electron accumulation layer at the surface of InN (with an electron density estimated to be ~2.5×10^{13} cm^{-2}) due to the presence of donor-type surface states [73], hinders the fabrication of metal-semiconductor Schottky contacts. The modification of the electronic properties of InN surface by using anodic or ozone-assisted oxidation treatment as possible solutions for the depletion of the surface electron accumulation and the passivation of InN surface donors has been investigated by several authors [74-76]. Moreover, the effect of polarity and GaN capping on the energy band bending at the InN surface were reported recently by Kuzmik et al. [77].

From the standpoint of InN-based devices, one of the first experimental attempts in this direction was reported by Dimakis et al. [62]. GaN cap layers were used to modify the surface electronic properties and to allow for the fabrication of Schottky barrier gate contacts. C-V measurements revealed the confinement of electrons within an InN/GaN quantum well heterostrusture and exhibited the capability to modulate the electron density within a 19 nm thick InN channel [62]. The C-V and I-V characteristics of InN/Al_2O_3 metal-oxide-semiconductor capacitors with different ex situ surface treatments were explored by Y. Jia et al [78] and although the I-V measurements showed low leakage currents, C-V profile indicated no significant change in the pinning of InN surface due to these surface treatments [78].

InN channel HFET transistors were reported recently with a 2–5 nm thick InN grown on zirconia substrates [79]; however, these transistors exhibited low mobilities (~58 cm^2/Vs), indicating a degraded InN structural quality, and very low current densities (25 mA/mm) [79]. The same group from the University of Tokyo, to solve the problem of high density of electrons in InN, explored the increase of the bandgap energy through alloying with a small amount of GaN [80]. Also in this approach, the reported values of device characteristics were disappointing; the on/off ratio of channel current was ~10^2, the mobility was 4.1 cm^2/Vs, and a drain current of 600 μA (non-normalized value) with a highly negative pinch-off voltage of -40 V was measured [80]. The best results, until the writing of this thesis, have been reported by Y. S. Lin et al [81] with a 26 nm thick InN grown on AlN, but also in this case their performance was far from the anticipated one, exhibiting an early breakdown and no saturation characteristics [81].

2.5 Chapter 2 references

[1] C. Wood, D. Jena. Polarization effects in semiconductors. Springer, New York, 2008.

[2] D. Jena. Polarization induced electron populations in III-V nitride semiconductors; Transport, growth, and device applications. Ph.D. dissertation, University of California, Santa Barbara, 2003.

[3] O. Ambacher, J. Smart, J. R. Shealey, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, and L. F. Eastman. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures. J. Appl. Phys. 85, 3222, 1999.

[4] I. P. Smorchkova, S. Keller, S. Heikman, C.R. Elsass, B. Heying, P. Fini, J. Speck, U.K. Mishra. Two-dimensional electron-gas AlN/GaN heterostructures with extremely thin AlN barriers. Appl. Phys. Lett. 77, 3998, 2000.

[5] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra. Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors. Appl. Phys. Lett. 77, 250, 2000.

[6] J. R. Shealy, T.R. Prunty, E.M. Chumbes, B.K. Ridley. Growth and passivation of AlGaN/GaN heterostructures. J. Cryst. Growth 250, 7, 2003.

[7] T. R. Prunty, J. A. Smart, E. M. Chumbes, B. K. Ridley, L. F. Eastman, and J.R. Shealy. Passivation of AlGaN/GaN heterostructures with silicon nitride for insulated gate transistors. In Proc. IEEE/Cornell Conf. High Perform. Devices, pp. 208–214, 2000.

[8] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. G. Xing. AlN/GaN insulated-gate HEMTs with 2.3 A/mm output current and 480 mS/mm transconductance. IEEE Electron Device Lett. 29, 661, 2008.

[9] Y. Cao and D. Jena. High-mobility window for two-dimensional electron gases at ultrathin AlN/GaN heterojunctions. Appl. Phys. Lett. 90, 182112, 2007.

[10] Relationship between measured and intrinsic transconductance of FET's. S. Y. Chou, and D. A. Antoniadis. IEEE Trans. Electron Devices 34, 448, 1987.

[11] D. A. Deen. Advanced design of ultra-thin barrier AlN/GaN HEMTs; A study of device design, modeling, and analysis. Ph.D. Dissertation, University of Notre Dame, 2011.

[12] T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra. Influence of the dynamic access resistance in the g_m and f_t linearity of AlGaN/GaN HEMTs. IEEE Trans. Electron Devices 52, 2117, 2005.

[13] F. Medjdoub, K. Iniewski. Gallium Nitride, Physics, Devices and Technology, Taylor & Francis Group, LLC, 2016.

[14] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso. AlGaN/GaN-based HEMTs failure physics and reliability: mechanisms affecting gate edge and schottky junction. IEEE Trans. Electron Devices 60, 3119, 2013.

[15] S.A Chevtchenko, P. Kurpas, N. Chaturvedi, R. Lossy, J. Würfl. Investigation and reduction of leakage current associated with gate encapsulation by SiN_x in AlGaN/GaN HFETs. International Conference on Compound Semiconductor Manufacturing Technology (CS ManTech 2011), Proceedings, pp. 237–240.

[16] G. I. Ng, H. Zhou, S. Arulkumaran, Y. K. T. Maung. Reduced surface leakage current and trapping effects in AlGaN/GaN high electron mobility transistors on silicon with SiN/Al_2O_3 passivation. Appl. Phys. Lett. 98, 113506, 2011.

[17] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert, and J. C. De Jaeger. Punchthrough in short-channel AlGaN/GaN HFETs. IEEE Trans. Electron Devices 53, 395, 2006.

[18] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, G. Tränkle. Punch-through-voltage enhancement of AlGaN/GaN HEMTs using AlGaN double-heterojunction confinement. IEEE Trans. Electron Devices 55, 3354, 2010.

[19] S. M. Sze, Physics of Semiconductor Devices, 2nd edition, Wiley, New York, 1981.

[20] R. Williams, Modern GaAs Processing Methods, Artech House Publishers, 1990.

[21] Z.M. Zhao, R.L. Jiang, P. Chen, W.P. Li, D.J. Xi, S.Y. Xie, B. Shen, R. Zhang, Y.D. Zheng. Aluminum and GaN contacts on Si (111) and sapphire. Appl. Phys. Lett. 77, 3140, 2000.

[22] S. Ruvimov, Z. Liliental-Weber, J. Washburn, K.J. Duxstad, E.E. Haller, Z.F. Fan, S.N. Mohammad, W. Kim, A.E. Botchkarev, H. Morkoc. Microstructure of Ti/Al and Ti/Al/Ni/Au Ohmic contacts for n-GaN. Appl. Phys. Lett. 69, 1556, 1996.

[23] B. Van Daele, G. Van Tendeloo, W. Ruythooren, J. Derluyn, M. R. Leys and M. Germain. The role of Al on Ohmic contact formation on n-type GaN and AlGaN/GaN. Appl. Phys. Lett. 87, 061905, 2005.

[24] B. P. Luther, S. E. Mohney, T. N. Jackson, M. Asif Khan, Q. Chen, and J. W. Yang. Investigation of the mechanism for Ohmic contact formation in Al and Ti/Al contacts to n-type GaN. Appl. Phys. Lett. 70, 57, 1997.

[25] Y. Dora, A. Chakraborty, S. Heikman, L. McCarthy, S. Keller, S.P. DenBaars, U.K. Mishra. Effect of Ohmic Contacts on Buffer Leakage of GaN Transistors. IEEE Electron Device Lett. 27, 529, 2006.

[26] L. Wang, I. Adesida, A.M. Dabiran, A.M. Wowchak, P.P. Chow. Ti/Al/Mo/Au Ohmic contacts to all-binary AlN/GaN high electron mobility transitors. Appl. Phys. Lett. 93, 032109, 2008.

[27] Z. Qin, Z. Chen, Y. Tong, X. Ding, X. Hu, T. Yu, and G. Zhang. Study of Ti/Au, Ti/Al/Au, and Ti/Al/Ni/Au Ohmic contacts to n-GaN. Appl. Phys. A 78, 729, 2004.

[28] D. Qiao, L. S. Yu, S. S. Lau, J. M. Redwing, J. Y. Lin, and H. X. Jiang. Dependence of Ni/AlGaN Schottky barrier height on Al mole fraction. J. Appl. Phys. 87, 801, 2000.

[29] H. Hahn, B. Reuters, H. Kalisch and A. Vescan. AlN barrier HFETs with AlGaN channels to shift the threshold voltage to higher positive values: a proposal. Semicond. Sci. Technol. 28, 074017, 2013.

[30] C. Pietzka, G. Li, M. Alomari, H. Xing, D. Jena, and E. Kohn. Surface potential analysis of AlN/GaN heterostructures by electrochemical capacitance-voltage measurements. J. Appl. Phys. 112, 074508, 2012.

[31] E. H. Nicollian and J. R. Brews, MOS Physics and Technologv, Wiley, New York, 1982.

[32] D. K. Schroder, Semiconductor Material and Device Characterization, Wiley-IEEE Press, 2006.

[33] C. Bae, C. Krug, G. Lucovsky, A. Chakraborty and U. Mishra. Surface passivation of n -GaN by nitrided-thin-Ga_2O_3/SiO_2 and Si_3N_4 film. J. Appl. Phys. 96, 2674, 2004.

[34] X. Liu, J. Kim, R. Yeluri, S. Lal, H. Li, J. Lu, S. Keller, B. Mazumder, J. S. Speck, and U. K. Mishra. Fixed charge and trap states of in situ Al_2O_3 on Ga-face GaN metal-oxide- semiconductor capacitors grown by metalorganic chemical vapor deposition. J. Appl. Phys. 114, 164507, 2013.

[35] S. M. Sze. Current transport and maximum dielectric strength of silicon nitride films. J. Appl. Phys. 38, 2951, 1967.

[36] T. L. Qu, J. Li, Y. G. Zhao, J. W. Mei, X. Liu, H. F. Tian, J. P. Shi, S. M. Guo, J. Li, D. N. Zheng, and J. Q. Li. Nonlinear current-voltage behavior and giant positive magnetoresistance in nonmagnetic Au/Yttria-stabilized zirconia/Si heterostructures. Appl. Phys. Lett. 95, 242113, 2009.

[37] M. Tapajna, L. Valik, F. Gucmann, D. Gregusova, K. Frohlich, S. Hascık, E. Dobrocka, L. Toth, B. Pecz and J. Kuzmik. Low-temperature atomic layer deposition-grown Al_2O_3 gate dielectric for GaN/AlGaN/GaN MOS HEMTs: Impact of deposition conditions on interface state density. J. Vac. Sci. Technol. B 35, 01A107, 2017.

[38] M. Tao, D. Park, S. N. Mohammad, D. Li, A. E. Botchkerav, and H. Morkoc. Electrical conduction in silicon nitrides deposited by plasma enhanced chemical vapour deposition. Philos. Mag. B 73, 723, 1996.

[39] M. A. Khan, A. Bhattarai, J. N. Kuznia, D. T. Olson. High electron mobility transistor based on a GaN-$Al_xGa_{1-x}N$ heterojunction. Appl. Phys. Lett. 63, 1214, 1993.

[40] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia. Current-voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias. Electronics Letters, 30, 2175, 1994.

[41] Y. C. Choi, M. Pophristic, B. Peres, M. G. Spencer, and L. F. Eastman. Fabrication and characterization of high breakdown voltage AlGaN/GaN heterojunction field effect transistors on sapphire substrates. J. Vac. Sci. Technol. B, 24, 2601, 2006.

[42] N. Ikeda, K. Kato, K. Kondoh, H. Kambayashi, J. Li, and S. Yoshida. Over 55 A, 800 V high power AlGaN/GaN HFETs for power switching application. Phys. Status Solidi A, 204, 2028, 2007.

[43] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Würfl, and G. Tränkle. AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low $R_{on}\times A$. IEEE Trans. Electron Devices 57, 3050, 2010.

[44] P. Srivastava, J. Das, D. Visalli, M. V. Hove, P. E. Malinowski, D. Marcon, S. Lenci, K. Geens, K. Cheng, M. Leys, S. Decoutere, R. P. Mertens, and G. Borghs. Record breakdown voltage (2200 V) of GaN DHFETs on Si with 2-μm buffer thickness by local substrate removal. IEEE Electron Device Lett. 32, 30, 2011.

[45] M. Wang, Y. Wang, C. Zhang, B. Xie, C. Wen, J. Wang, Y. Hao, W. Wu, K. J. Chen and B. Shen. 900 V/1.6 $m\cdot cm^2$ normally off Al_2O_3/GaN MOSFET on silicon substrate. IEEE Trans. Electron Devices 61, 2035, 2014.

[46] M. Kuzuhara and H. Tokuda. Low-Loss and High-Voltage III-Nitride Transistors for Power Switching Applications. IEEE Trans. Electron Devices 62, 405 2015.

[47] S.C. Binari, L.B. Rowland, W. Kruppa, G. Kelner, K. Doverspike, D.K. Gaskill. Microwave performance of GaN MESFETs. Elec. Lett. 30, 1248, 1994.

[48] H. Kawai, M. Hara, F. Nakamura, S. Imanaga. AlN/GaN insulated gate heterostructure FET with regrown n+GaN ohmic contact. Elec. Lett. 34, 592, 1998.

[49] I. Daumiller, P. Schmid, E. Kohn, C. Kirchner, M. Kamp, K.J. Ebeling, L.L. Pond, C. Weitzel. DC and RF characteristics of AlN/GaN doped channel heterostructure field effect transistor. Elec. Lett. 35, 1588, 1999.

[50] E. Alekseev, A. Eisenbach, D. Pavlidis. Low interface state density AlN/GaN MISFETs. Elec. Lett. 35, 2145, 1999.

[51] A. M. Dabiran, A. M. Wowchak, A. Osinsky, J. Xie, B. Hertog, B. Cui, D. C. Look, and P. P. Chow. Very high channel conductivity in low-defect AlN/GaN high electron mobility transistor structures. App. Phys. Lett. 93, 082111, 2008.

[52] A. Adikimenakis, K. E. Aretouli, E. Iliopoulos, A. Kostopoulos, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas. High electron mobility transistors based on the AlN/GaN heterojunction. Microelectron. Eng. 86, 1071, 2009.

[53] Y. Tang, K. Shinohara, D. Regan, A. Corrion, D. Brown, J. Wong, A. Schmitz, H. Fung, S. Kim, and M. Micovic. Ultrahigh-speed GaN high-electron-mobility transistors with f_T/f_{max} of 454/444 GHz. IEEE Electron Device Lett. 36, 549, 2015.

[54] J. Kuzmik and A. Georgakilas. Proposal of high-electron mobility transistors with strained InN channel. IEEE Trans. Electron Devices 58, 720, 2011.

[55] V. M. Polyakov and F. Schwierz. Low-field electron mobility in wurtzite InN. Appl. Phys. Lett. 88, 032101, 2006.

[56] E. Dimakis, G. Konstantinidis, K. Tsagaraki, A. Adikimenakis, E. Iliopoulos and A. Georgakilas. The role of nucleation temperature in In-face InN- on-GaN (0001) growth by plasma-assisted molecular beam epitaxy. Superlatt. Microstruct. 36, 497, 2004.

[57] E. Dimakis, E. Iliopoulos, K. Tsagaraki, Th. Kehagias, Ph. Komninou and A. Georgakilas. Heteroepitaxial growth of In-face InN on GaN (0001) by plasma assisted molecular beam epitaxy. J. Appl. Phys. 97, 113520, 2005.

[58] E. Dimakis, E. Iliopoulos, K. Tsagaraki, Ph. Komninou, Ph. Kehagias, A. Delimitis, A. Georgakilas. Correlation between nucleation, morphology and residual strain of InN grown on Ga-face GaN (0001). J. Cryst. Growth 278, 367, 2005.

[59] E. Dimakis, E. Iliopoulos, K. Tsagaraki, and A. Georgakilas. Physical model of InN growth on Ga- face GaN (0001) by molecular beam epitaxy. Appl. Phys. Lett. 86, 133104, 2005.

[60] E. Dimakis, E. Iliopoulos, K. Tsagaraki and A. Georgakilas. Self-regulating mechanism of InN growth on GaN (0001) by molecular beam epitaxy; from nanostructures to films. Phys. Stat. Sol. (a) 203, 1686, 2006.

[61] E. Dimakis, J. Domagała, A. Delimitis, Ph. Komninou, A. Adikimenakis, E. Iliopoulos, and A. Georgakilas. Structural properties of 10 μm thick InN grown on sapphire (0001). Superlattices and Microstructures 40, 246, 2006.

[62] E. Dimakis, E. Iliopoulos, M. Kayambaki, K. Tsagaraki, A. Kostopoulos, G. Konstantinidis and A. Georgakilas. Growth optimization of electron confining InN/GaN quantum well heterostructure. Electronic Materials 36, 373, 2007.

[63] Th. Kehagias, E. Iliopoulos, A. Delimitis, G. Nouet, E. Dimakis, A. Georgakilas and Ph. Komninou. Interfacial structure of MBE grown InN on GaN. Phys. Stat. Sol. (a) 205,777, 2005.

[64] A. Delimitis, P. Gladkov, Ph. Komninou, Th. Kehagias, J. Arvanitidis, S. Ves, M. Katsikini, E. Dimakis and A. Georgakilas. Structural and optical characterization of thick InN epilayers grown with a single or two step growth process on GaN (0001). Phys. Stat. Sol. (a) 203, pp. 162, 2006.

[65] J. Arvanitidis, M. Katsikini, S. Ves, A. Delimitis, Th. Kehagias, Ph. Komninou, E. Dimakis, E. Iliopoulos and A. Georgakilas. Raman and transmission electron microscopy characterization of InN samples grown on GaN/Al_2O_3 by molecular beam epitaxy. Phys. Stat. Sol. (b) 243, 1588, 2006.

[66] J. Arvanitidis, D. Christofilos, G. A. Kourouklis, A. Delimitis, M. Katsikini, Ph. Komninou, S. Ves, E. Dimakis and A. Georgakilas. Depth profile of the biaxial strain in a 10 μm thick InN (0001) film. J. Appl. Phys. 100, 113516, 2006.

[67] E. Dimakis, E. Iliopoulos, K. Tsagaraki, A. Adikimenakis and A. Georgakilas. Biaxial strain and lattice constants of InN (0001) films grown by plasma-assisted molecular beam epitaxy. Appl. Phys. Lett. 88, 191918, 2006.

[68] E. Dimakis, J. Domagala, E. Iliopoulos, A. Adikimenakis and A. Georgakilas. Analysis of biaxial strain in InN (0001) epilayers grown by molecular beam epitaxy. Phys. Stat. Sol. (a) 204, 1996, 2007.

[69] H. Lu, W. J. Schaff, L. F. Eastman, J. Wu, W. Walukiewicz, V. Cimalla, and O. Ambacher. Growth of a-plane InN on r-plane sapphire with a GaN buffer by molecular-beam epitaxy. Appl. Phys. Lett. 83, 1136, 2003.

[70] H. Naoi, F. Matsuda, T. Araki, A. Suzuki, and Y. Nanishi. The effect of substrate polarity on the growth of InN by RF-MBE. J. Cryst. Growth 269, 155, 2004.

[71] X. Q. Wang, S. B. Che, Y. Ishitani, and A. Yoshikawa. Step-flow growth of In polar InN by molecular beam epitaxy. Jpn. J. Appl. Phys., Part 2 45, L730, 2006.

[72] S. V. Ivanov, T. V. Shubina, V. N. Jmerik, V. A. Vekshin, P. S. Kop'ev, and B. Monemar. Plasma-assisted MBE growth and characterization of InN on sapphire J. Cryst. Growth 269, 1, 2004.

[73] I. Mahboob, T. D. Veal, C. F. McConville, H. Lu, and W. J. Schaff. Intrinsic Electron Accumulation at Clean InN Surfaces. Phys. Rev. Lett. 92, 036804, 2004.

[74] A. Denisenko, C. Pietzka, A. Chuvilin, U. Kaiser, H. Lu, W. J. Schaff, and E. Kohn. Depletion of surface accumulation charge in InN by anodic oxidation. J. Appl. Phys. 105, 033702, 2009.

[75] V. Lebedev, Ch. Y. Wang, V. Cimalla, S. Hauguth, T. Kups, M. Ali, G. Ecke, M. Himmerlich, S. Krischok, J. A. Schaefer, and O. Ambacher. Effect of surface oxidation on electron transport in InN thin films. J. Appl. Phys. 101, 123705, 2007.

[76] V. Cimalla, V. Lebedev, C. Y. Wang, M. Ali, G. Ecke, V. M. Polyakov, F. Schwierz, O. Ambacher, H. Lu, and W. J. Schaff. Reduced surface electron accumulation at InN films by ozone induced oxidation. Appl. Phys. Lett. 90, 152106, 2007.

[77] J. Kuzmık, S. Hascık, M. Kucera, R. Kudela, E. Dobrocka, A. Adikimenakis, M. Micusık, M. Gregor, A. Plecenik, and A. Georgakilas. Elimination of surface band bending on N-polar InN with thin GaN capping. Appl. Phys. Lett. 107, 191605, 2015.

[78] Y. Jia, A. M. Dabiran, and U. Singisetti. Electrical characterization of atomic layer deposited Al_2O_3/InN interfaces J. Vac. Sci. Technol. A 34, 01A133, 2016.

[79] M. Oseki, K. Okubo, A. Kobayashi, J. Ohta, and H. Fujioka. Field-effect transistors based on cubic InN. Sci. Rep. 4, 3951, 2014.

[80] A. Kobayashi, K. S. Lye, K. Ueno, J. Ohta, and H. Fujioka. Epitaxial growth of In-rich InGaN on yttria-stabilized zirconia and its application to metal-insulator-semiconductor field-effect transistors. J. Appl. Phys. 120, 085709, 2016.

[81] Y. S. Lin, S. H. Koa, C. Y. Chan, S. H. Hsu, H. M. Lee, and S. Gwo. High current density InN/AlN heterojunction field-effect transistor with a SiN_x gate dielectric layer. Appl. Phys. Lett. 90, 142111, 2007.

CHAPTER 3

Device Processing and Characterization

3.1 Device fabrication

All samples that will be discussed were grown by PAMBE and processed at the Microelectronics Research Group lab in the Institute of Electronic Structure and Laser (IESL-FORTH). The process technology of III-Nitrides and GaN HEMTs, that had been developed in the MRG lab from previous projects, was adapted and optimized for the fabrication of thin AlN/GaN/AlN double heterostructure HEMTs and ultrathin InN-channel transistors with the optimum electrical characteristics.

The process of device fabrication to produce the transistors and electrical test structures in this research project required three or four contact photolithography steps. The defined patterned structures were produced by optical lithography using the Karl Suss MA6 mask aligner. Lithography is a process of transferring geometric patterns defined by a mask on the surface of a sample. In photolithography, a photosensitive polymer is spun on the substrate, dried, and then exposed to ultraviolet (UV) light through a photo mask with the proper geometrical pattern [1]. After exposure, the sample is soaked in a solution that develops the mask pattern in the selectively exposed photosensitive material. Fig. 3.1 shows the basic idea of photolithography and the Karl Suss MA6 mask aligner used in this work. Depending on the type of polymer used, either exposed or unexposed areas of the film are removed in the developing process. The sample is then placed in an ambient that etches the semiconductor surface area that is not protected by the polymer pattern. Due to the ability of the polymeric material to resist the etching process, these polymers are called photoresists (PRs). Negative PRs become less soluble in developer when they are exposed to radiation, while positive PRs become more soluble after exposure (Fig. 3.1). Positive PRs are suitable for lift-off processes to only a limited extent due to the formation of positive sidewalls, which promotes the metal coverage of the sidewalls during deposition making lift-off difficult [1]. If the use of positive PRs cannot be avoided, PRs with sidewalls as steep as possible should be considered. Negative PRs are generally, the best choice for lift-off processes because they are designed to produce lift-off with a reproducible undercut. Such an undercut help to prevent the resist sidewalls from being coated, which makes the subsequent lift-off easier [1].

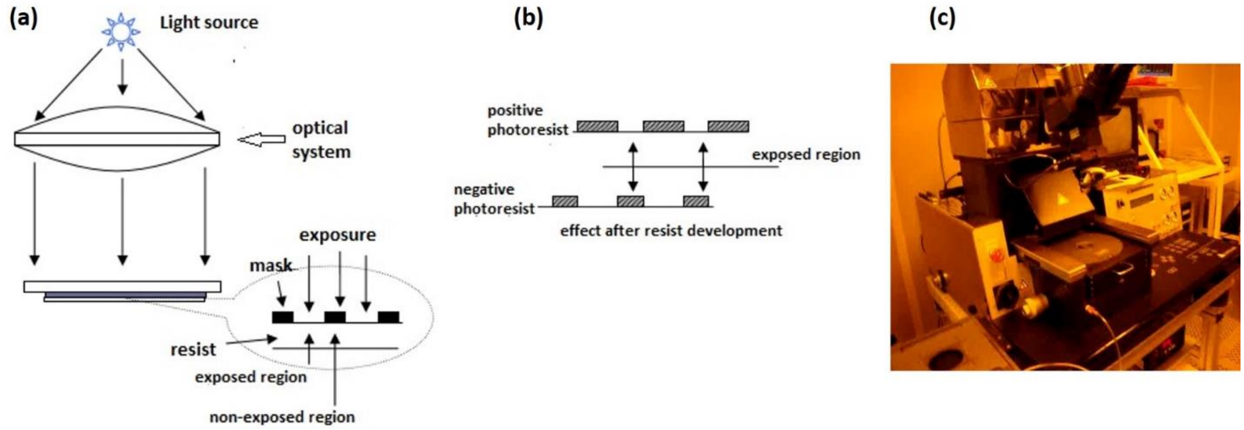


Fig. 3.1 (a) Schematic of contact lithography. Note that mask and sample are physically in contact with each other, (b) different photo resist development process. (c) The Karl Suss MA6 mask aligner used in this work.

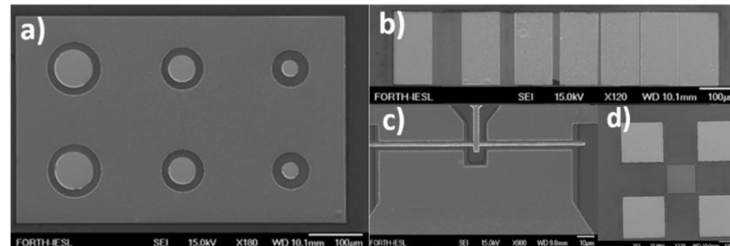


Fig. 3.2 SEM images showing a) circular diodes of 30-100 μm diameter, b) TLM patterns, c) transistor and d) Hall-effect structure.

Due to the diffraction limit of the light, the resolution (R), defined as the minimum feature that can be achieved, is approximately the same order of magnitude of the wavelength of light (λ) used in the UV exposure optics of the system, and is given by $R=k_1\lambda/NA$, where $k_1=0.6\text{-}0.8$ and NA is the numerical aperture of the exposure system. However, in real samples (exposed under hard contact mode in our case) the best resolution which can be achieved repeatedly is ~1 μm. Devices for Hall-effect measurements, TLM patterns, circular diodes with 30-100 μm diameters and transistors with gate width and length of 2 x 50 and 1 μm, respectively, were fabricated, as shown in Fig. 3.2.

Although the device fabrication is strongly dependent on the final purpose of the device and the processed material, there are basic common processing steps to almost all kind of devices and will be briefly discussed.

3.1.1 Surface cleaning

Cleaning of samples is necessary before the fabrication process starts and after each lithography step. Samples were first rinsed by organic solvents (acetone, isopropanol) to remove organic species, then dipped into HCl or HF solution for ~2 minutes to remove native oxide and metal contaminants and followed by DI water rinse. The same procedure was used before several processing steps like metallization, to improve adherence and reduce impurity and interface defects at the metal/semiconductor interface.

3.1.2 Mesa isolation

The usual approach in semiconductor fabrication technology is to process many devices on the same sample at the same time. By mesa insulation the individual devices (transistors, diodes, etc.) are isolated from each other by removing the conducting regions between them, i.e. the 2DEG channel must be removed around each device to exclude conductive interconnections. Mesa isolation is typically achieved with dry etching, since group III-N materials are very resistant to wet chemical etching and also produce rough surfaces. This step involves lithographic patterning of a PR, reactive ion etching (RIE) of the sample and removal of the PR.

Once a sample was loaded on the vacuum spinner chuck, PR AZ 5214, which was mainly used, was dispersed to cover the whole sample before spinning began. The final spin speed was 4000 rpm with a spin time of 20 seconds resulting to a ~1.4 µm PR thickness. After PR spinning, the sample was soft baked at 110 ºC for 1 minute to remove the solvent and then loaded onto the mask aligner. Being the first step in the HEMT fabrication process, the mesa level lithography did not require fine alignment, instead only a rough alignment was made, to make sure that the pattern fits well on the sample. In this step, alignment markers were also placed on the sample for the alignment of the subsequent photolithography steps. The duration of the UV exposure of the PR was optimized at ~4.5 seconds. After UV exposure, the sample was immersed in the AZ 400 K developer for ~20 seconds, followed by DI water rinsing and N_2 drying. After microscope inspection of developed feautures, the sample was loaded in the RIE chamber to create the device

RIE parameters	AlN/GaN structures	InN-based structures
Gases flow rate	BCl_3/Cl_2 : 7/1 sccm	BCl_3/Ar : 7/25 sccm
RF power	50 W	100 W
Pressure	10 mTorr	10 mTorr
DC bias measured	-200 V	-300 V

Table I: RIE recipe parameters for structures processed in this work.

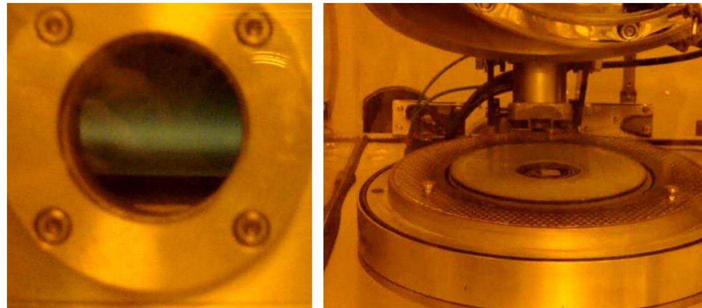


Fig. 3.3 RIE chamber during plasma etching (left), loading of the sample in the RIE chamber (right).

mesas (Fig. 3.3). In conventional RIE, physical and chemical components of etching cannot be independently controlled [2]. Etch rates depend strongly on the plasma self-bias voltage. The gases for the dry etching of III-nitrides are mostly halogen-based with the most prevalent being chlorine-based. If III-nitrides are etched in Cl-based gases, the etch-products are $GaCl_x$, $InCl_x$, and $AlCl_x$ for the Group III elements, while nitrogen is removed in the form of NCl_3 or perhaps free N_2 [2]. Table I shows the basic RIE recipe parameters for the optimized processing used in this work. Once etching was completed, the sample was unloaded and the PR was removed by dipping in acetone (or other solvents) and transferred to the optical microscope for inspection. In order to determine the etch depth, the Veeco Dektak surface profiler was used for step height measurement. To confirm electrical isolation had been attained, interdevice currents were measured between isolated mesa islands.

3.1.3 Ohmic metallization

The second level of device fabrication was the formation of ohmic contacts. This level involved lithographic patterning of a PR coating, electron beam (e-beam) evaporation of a metal stack combination, lift-off of the metals and rapid thermal annealing (RTA). After PR soft baking, similar to the first step, the sample was carefully aligned manually, using x, y, and theta controls, and exposed to irradiation using the MA6 mask aligner. After PR development, the sample was loaded in the e-beam evaporator and the chamber was allowed to pump down to base pressure of approximately 2×10^{-7} Torr before metal deposition begins. Metal deposition was performed using a Temescal e-beam evaporation system. Ti/Al/Ni/Au (30/170/40/50 nm) ohmic metal stacks were deposited; see 2.2.5 for details about the role of metals. The metals deposition was followed by lift-off, typically in an acetone bath. Lift-off times varied, but usually lasted at least 30 – 60 minutes if no ultrasonics were used. A DI water bath was followed and finally the sample was rinsed and N_2 dried. Microscope inspection was used to verify that the lift-off process was successful. Finally, RTA of the ohmic contacts was performed. Samples were loaded onto a Si carrier wafer in the annealing chamber and annealed at 750 °C for 2 minutes under vacuum, in the case of AlN/GaN HEMT structures.

3.1.4 Gate metallization

The gate lithography was the final and most challenging step of the HEMT fabrication process due to the difficulty of creating 1 μm sized features with contact lithography. In addition to this, great care was taken to avoid misalignment shifts and be as accurate as possible during this step. Since the nominal source-gate and gate-drain spacings were 1 and 2 μm, respectively, misalignment shifts could result to inconsistency in the lateral electric field strength between gate and drain electrodes from sample to sample, and thus complicating the comparative evaluation of different devices. The same photolithography process that was used for previous steps was also followed for the gate lithography. After careful alignment, exposure and development, the sample was loaded into the Temescal e-beam evaporator. After deposition, metal lift-off was performed, the sample was soaked and rinsed with DI water, dried by N_2 blow and then its surface was inspected under an optical microscope.

3.2 Electrical characterization methods

For the electrical characterization of the fabricated devices, DC, pulsed I–V, and C-V measurements were conducted. For I-V measurements a Keithley 4200 semiconductor characterization system and a Keithley 2602A System SourceMeter were used, while C-V measurements were carried out by a HP 4284A Precision LCR meter.

3.2.1 DC characterization

The dc I-V characteristics of a transistor provide the main information for its operation capabilities. A DC I-V test configuration incorporates Source Measurement Units (SMUs) which are capable of sourcing and measuring both current and voltage and can be current-limited to prevent damage to the device. This can be done in the software by setting the current compliance of each SMU to a safe level. The measurement is carried out by a voltage or current sweep with discrete increment steps that are pre-set by the user (Fig. 3.4).

3.2.2 Pulsed characterization

Pulsed I−V characterization has been used as a method to overcome thermal effects as well as to evaluate trapping phenomena that influence the transient response of the transistors [3]. The application of high voltage and high current results to a great amount of heat generation in the 2DEG channel of the device, and a corresponding rise of lattice temperature. Thus, a degradation of device performance can be observed due to degradation in mobility, which in turn causes reduction in drain current [4]. In pulsed I-V measurements, square voltage pulses are applied from a quiescent bias (QB) point to obtain current measurements at the latter part of the pulse as shown in Figs 3.5 and 3.6. Then, the device under test returns and remains at the initial QB point until the next voltage pulse is applied. If the pulse duration (width) is short enough compared to the separation time between consecutive voltage pulses (period), both temperature and trapping effects are dependent mainly on QB point. In case of a very short pulse duration, thermal effects can be minimized and trapping effects are frozen when emission/capture time constants are smaller than the pulse duration. Thus, by appropriately choosing QB points and pulse width/period, trapping effects can be analyzed with minimal thermal effect, as we will see analytically in the next chapter.

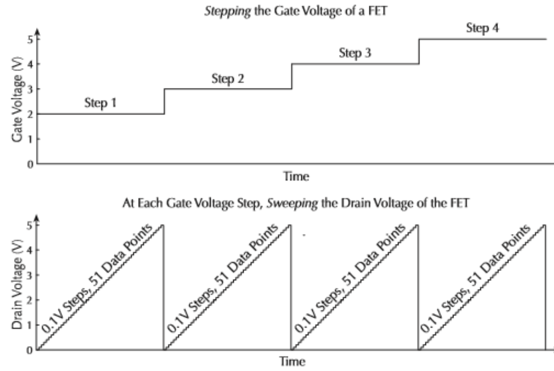


Fig. 3.4 Graphical illustration of 4200-SCS operation during DC I-V transistor measurement (taken from Keithley Model 4200-SCS user's manual).

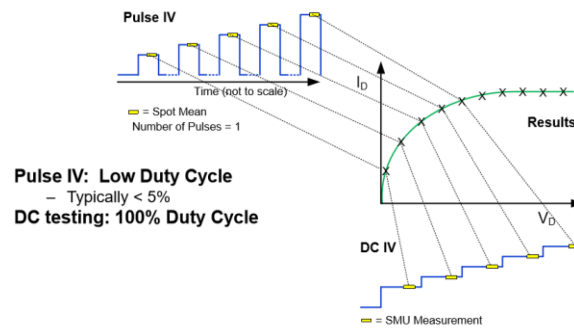


Fig. 3.5 Pulsed I-V versus DC I-V testing diagram (taken from Keithley Model 4200-SCS user's manual). Duty cycle is the fractional amount of time the pulse is "on" during a period.

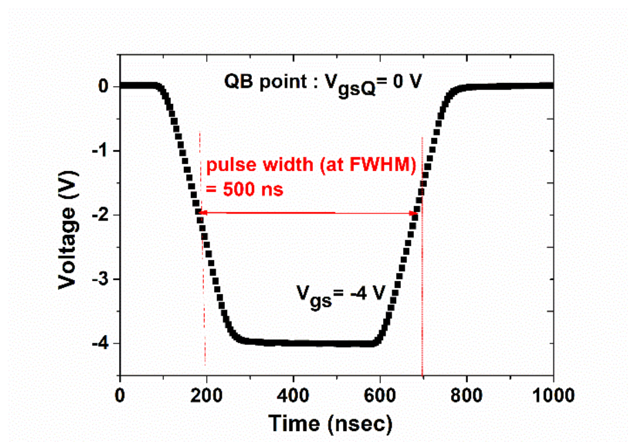


Fig. 3.6 Example of a pulse applied to the gate of an AlN/GaN HEMT with $V_{gsQ} = 0$ V.

3.2.3 Capacitance-Voltage characterization

The C-V technique is the most commonly used method for providing important material information such as the profile of carrier concentration and, in the case of a 2DEG, its sheet carrier concentration N_s and region of formation. It is also a diagnostic tool for interface states characterization by multifrequency measurements using an inductance, capacitance and resistivity (LCR) meter. This method provides physical insight into fundamental properties of the material structures and interfaces without the complications of a full HEMT device fabrication process, since it can be performed on a simple Schottky diode or MIS capacitor structure.

3.2.3.1 Carrier concentration profiling

C-V profiling is widely used to probe the electron concentration in a semiconductor. The C-V techniques are based on the fact that the depletion region width, W, of the reverse biased semiconductor junction depends on the dc reverse applied bias voltage V [5]. The capacitance is determined by superimposing a small sinusoidal small-amplitude ac voltage v_{ac} on the dc voltage V resulting in a semiconductor charge increment dQ_s. The ac voltage frequency is typically 1 kHz to 1 MHz with 10 to 20 mV amplitude, but other frequencies and other voltages can be used.

The application of C-V measurements on Schottky diode contacts has been well analysed in several texts [1,5]. The discussion in the following will be limited to the case of C-V measurements on MIS capacitors [6]. By considering a MIS capacitor driven into depletion and by assuming a negligible effect of interface states, a small increase in the applied voltage dV is given by [6]

$$dV = dV_{ins} + d\psi_s = dQ_s / C_{ins} + d\psi_s \quad (3.1)$$

where V_{ins} is the voltage drop across the insulator, ψ_s the band bending in the semiconductor, C_{ins} the insulator capacitance per unit area and Q_s the space charge density per unit area. The charge increase in the semiconductor depletion region causes an increase in the electric field E [6]

$$dE = dQ_s / \varepsilon_s \quad (3.2)$$

where ε_s is the dielectric permittivity of the semiconductor. The corresponding increase in band bending (or surface potential) is approximately [6]

$$d\psi_s = W\, dE \quad (3.3)$$

Substituting Eqs. (3.2, 3.3) into Eq. (3.1)

$$dV = dQ_s (1/C_{ins} + 1/C_d) = dQ_s / C_{tot} \tag{3.4}$$

where C_{tot} is the total measured capacitance and $C_d = \varepsilon_s / W$. Using $dQ_s = qN(W)\, dW$ where N(W) is the doping concentration as a function of W, it is obtained

$$dV = qN(W)\, dW / C_{tot} \tag{3.5}$$

Also, dW is given by

$$dW = \varepsilon_s d(1/C_d) = \varepsilon_s d(1 / C_{tot}) \text{ (because } 1/C_d = 1/C_{tot} - 1/C_{ins} \text{ and } d(1/C_{ins})=0) \tag{3.6}$$

By substituting Eq. (3.6) into Eq. (3.5) and solving for N(W), it is obtained [6]

$$\boldsymbol{N(W) = -\frac{C_{tot}^3}{q\varepsilon_s}\frac{dV}{dC_{tot}} = \frac{2}{q\varepsilon_s\ d(\frac{1}{C_{tot}^2})/dV}} \tag{3.7}$$

It should be noted that for the derivation of Eq. (3.7) the depletion approximation was used, where the minority carriers are neglected and total depletion of majority carriers in the space-charge region to a depth W, as well as perfect charge neutrality beyond W is assumed [5]. This is a reasonably good approximation when the space charge region is reverse biased and when the doping is uniform [5]. Furthermore, the incremental charge variation of the donor ion density at the edge of the space-charge region was used. The ac probe voltage exposes more or less ionized donors at the space charge edge, and the charges that actually move in response to the ac voltage are the mobile electrons, not the donor ions [5]. Hence, the differential C-V profiling technique determines the carrier density, not the doping density, and what is actually measured is an effective or apparent majority carrier density profile [5,7]. Although in semiconductors and heterostructures with large variations in the doping concentration, and especially in structures with quantum confinement such as in 2DEG heterostructures, the C–V-concentration does not have a direct physical meaning [8], N(W) corresponds roughly to the free carrier concentration n(z), i.e $N(W) \approx n(z)$ [8,9]. Evenmore, it has been reported that conservation of charge is satisfied for C–V-profiles, that is [8,10]

$$N_s = \int_{-\infty}^{+\infty} N(W)(z)dz = \int_{-\infty}^{+\infty} n(z)dz \tag{3.8}$$

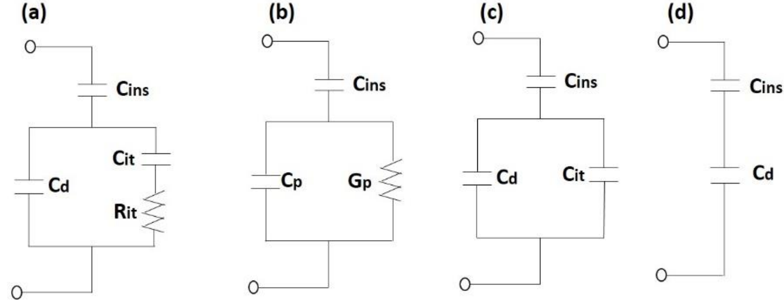


Fig. 3.7 (a)-(b) Equivalent circuits incorporating interface-trap effects, C_{it}, and R_{it}, (c) low-frequency limit (d) high-frequency limit. (Adapted from *Physics of semiconductor devices - S.M. Sze,* ref. [11]).

3.2.3.2 Effect of frequency dispersion in C-V measurements

Interface trap levels are generally distributed across the energy bandgap. A change of charge in the interface traps occurs when a bias voltage is applied, resulting in a movement of the Fermi level, up or down with respect to the interface-trap levels [11]. This change of charge influences the MIS capacitance and alters the characteristics of the ideal MIS curve. The basic equivalent circuit incorporating the interface-trap effect is shown in Fig. 3.7(a). In the figure, C_{ins} and C_d, are the insulator capacitance ($C_{ins}=\varepsilon/d$) and the semiconductor depletion-layer capacitance, respectively. C_d is obtained by differentiating the total static charge in the semiconductor side with respect to the semiconductor band bending (built-in potential) ($C_d=dQ_s/d\psi_s$) [11]. C_{it}, and R_{it}, are the capacitance and resistance associated with the interface traps and, thus, are also function functions of energy [11]. The parallel branch of the equivalent circuit in Fig. 3.7(a) can be converted [11] into a frequency-dependent capacitance C_p in parallel with a frequency-dependent conductance G_p, (Fig. 3.7 (b)), where

$$C_p = C_d + \frac{C_{it}}{1+\omega^2\tau_{it}^2} \tag{3.10}$$

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{3.11}$$

The time constant (or characteristic response time) associated with electron emission of trapped electrons for traps is given by $\tau_{it} = \exp(E/kT)/\sigma\upsilon_{th}N_c$, where σ is the trap capture cross section, υ_{th} is the electron thermal velocity, and N_c is the density of states in the semiconductor conduction band [11,12]. The trap energy depth E corresponding to a measurement frequency f_m ($\tau_{it}=2\pi/\omega$, where $\omega=2\pi f_m$) is given by $E = kT \ln(\sigma N_c u_{th}/f_m)$. This means that the lower the measurement frequency, the deeper the trap energy depth at which C_{it} starts to be detected.

When the Fermi level is aligned with interface traps with a characteristic frequency (defined as $1/\tau_e$) equal to the measurement frequency f_m, interface traps respond to the ac signal and contribute to the capacitance leading to the total capacitance increase (overestimation). In other words, only traps near E_F with a response time τ_e equal or below the period of the signal ($1/f_m$, f_m is the measurement frequency) can respond to the ac signal and will have time to capture and emit electrons during one period (fast traps) [12-14]. This occurs in the low-frequency (LF) limit where R_{it} is set to zero and C_d, is in parallel to C_{it} (Fig. 3.7 (c)) [11].

In the high-frequency (HF) limit, the traps are not fast enough to respond to the fast signal (slow traps). The emission time constant of traps τ_e is longer than the period of the ac signal and the measured capacitance cannot capture the charging/discharging behavior of these traps and thus the capacitance remains the same. Thus, they do not introduce a capacitance and the C_{it}-R_{it} branch is ignored (Fig. 3.7 (d)) [11,12]. The total capacitance for these two cases (low-frequency C_{LF} and high-frequency C_{HF}) are

$$C_{LF} = C_{ins}(C_d+C_{it})/ (C_{ins}+C_d+C_{it}) \quad (3.12)$$

$$C_{HF}= C_{ins} C_d / (C_{ins}+C_d) \quad (3.13)$$

However, interface traps can follow the slowly varying dc bias resulting in a stretch-out of the C-V curve in the voltage direction (Fig. 3.8) [11,15]. For a fixed voltage, since some charge will be necessary to fill the traps, the remaining charge to be put in the depletion layer is decreased and this will decrease the surface potential (or band bending) ψ_s [11]. But since the relationship between C_d and ψ_s is fixed ($C_d=dQ_s/d\psi_s$), the change of ψ_s yields also a change of C_d. Thus, due to the fact that extra charge has to fill the traps, more total charge is needed or applied voltage to accomplish the same band bending ψ_s [11]. Consequently, in HF, although interface traps do not

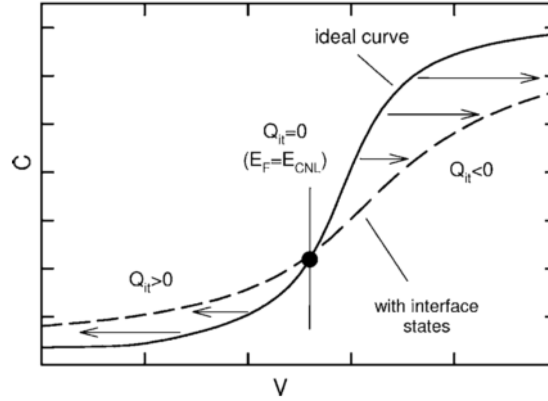


Fig. 3.8 Schematic representation of a typical interface-state-related stretch out of a high frequency C-V curve (e.g., for a SiO_2/Si MIS structure). Image taken from ref. [15].

---

affect directly the total capacitance through the extra elements C_{it}, R_{it}, they have a significant impact through C_d [11]. This can be more obvious by considering the following equations

$$C=dQ/dV \quad \text{(change of charge due to the change of voltage)} \tag{3.14}$$

By assuming no insulator charge $Q = Q_s + Q_{it}$. The bias voltage is partially dropped across the insulator and partially across the semiconductor; thus [5],

$$V = V_{FB} + V_{ins} + \psi_s = V_{FB} + Q/C_{ins} + \psi_s \tag{3.15}$$

where V_{FB} is the flat band voltage (see par. 2.3.4) and V_{ins} the insulator voltage. Eq. (3.14) becomes

$$C = (dQ_s+dQ_{it}) / (dV_{ins}+d\psi_s) \tag{3.16}$$

Therefore, it is clear that for a given band bending ψ_s, V varies when interface traps exist, causing the C-V stretch-out.

In the case of LF C-V curve, interface traps do respond to the frequency and the curve distorts because the interface traps contribute an interface trap capacitance C_{it} and also the curve stretches out along the voltage axis [5,11].

3.3 Chapter 3 references

[1] R. Williams, Modern GaAs Processing Methods, Artech House Publishers, 1990.

[2] I. Adesida, C. Youtsey, A. T. Ping, F. Khan, L. T. Romano, and G. Bulman. Dry and wet etching for group III-Nitrides. MRS Internet J. Nitride Semiconductor Res. 4S1, G1.4, 1999.

[3] C. P. Baylis, II and L. P. Dunleavy. Understanding pulsed IV measurement waveforms. Electron Devices for Microwave and Optoelectronic Applications, 2003. The 11th IEEE International Symposium on, 2003, pp. 223- 228.

[4] W. D. Hu, X. S. Chen, Z. J. Quan, C. S. Xia, W. Lu, and P. D. Ye. Self-heating simulation of GaN-based metal-oxide-semiconductor high-electron-mobility transistors including hot electron and quantum effects. J. Appl. Phys. 100, 074501, 2006.

[5] D. K. Schroder, Semiconductor Material and Device Characterization, Wiley-IEEE Press, 2006.

[6] W. V. Gelder and E. H. Nicollian. Silicon impurity distribution as revealed by pulsed MOS C-V measurements. J. Electrochem. Soc. 118, 138,1971.

[7] W.C. Johnson and P.T. Panousis. The influence of debye length on the C–V measurement of doping profiles. IEEE Trans. Electron Devices 18, 965, 1971.

[8] O. Ambacher, J. Smart, J. R. Shealey, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, and L. F. Eastman. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures. J. Appl. Phys. 85, 3222, 1999.

[9] E. F. Schubert, Doping in III-V Semiconductors. Cambridge University Press, Cambridge 1993, p. 492.

[10] H. Kroemer, Wu-Yi Chien, J. S. Harris, Jr., and D. D. Edwall. Measurement of isotype heterojunction barriers by C-V profiling. Appl. Phys. Lett. 36, 295, 1980.

[11] S. M. Sze, Physics of Semiconductor Devices, 2nd edition, Wiley, New York, 1981.

[12] Y. Lu, Q. Jiang, Z. Tang, S. Yang, C. Liu, and K. J. Chen. Characterization of SiN_x/AlN passivation stack with epitaxial AlN grown on AlGaN/GaN heterojunctions by plasma-enhanced atomic layer deposition. Applied Physics Express 8, 064101, 2015.

[13] N. Ramanan, B. Lee, and V. Misra. Comparison of methods for accurate characterization of interface traps in GaN MOS-HFET devices. IEEE Trans. Electron Devices 62, 546, 2015.

[14] M. Fagerlind, F. Allerstam, E. Ö. Sveinbjörnsson, N. Rorsman, A. Kakanakova-Georgieva, A. Lundskog, U. Forsberg, and E. Janzén. Investigation of the interface between silicon nitride passivations and AlGaN/AlN/GaN heterostructures by C(V) characterization of metal-insulator-semiconductor-heterostructure capacitors. J. Appl. Phys. 108, 014508, 2010.

[15] M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz. Effects of interface states and temperature on the C-V behavior of metal/insulator/AlGaN/GaN heterostructure capacitors J. Appl. Phys. 103, 104510, 2008.

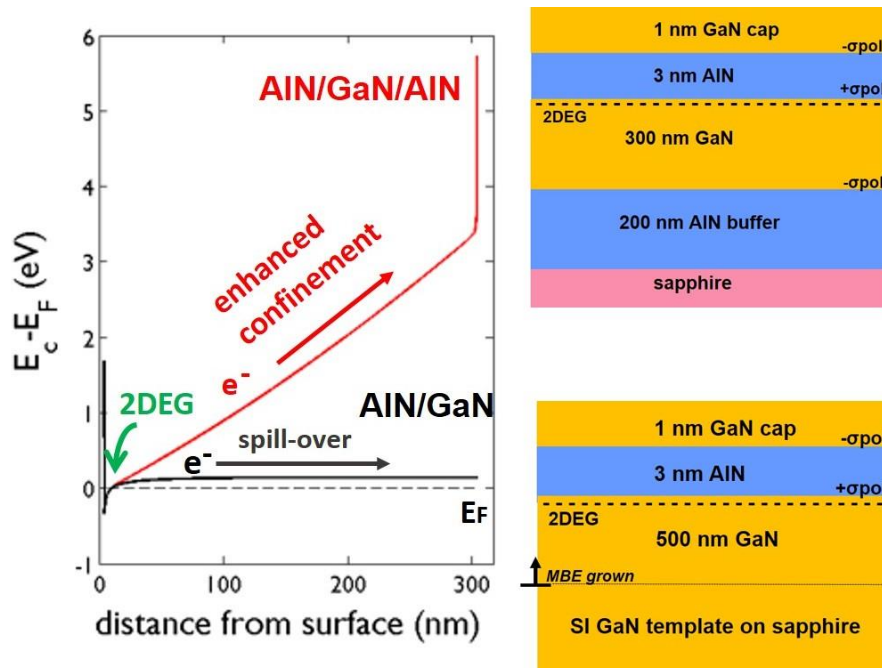
CHAPTER 4

AlN/GaN/AlN HEMTs

4.1 Introduction and motivation of the study

GaN HEMTs are based on heteroepitaxial material, and, typically, a 3–4 μm thick GaN buffer layer is initially grown to reduce the threading dislocation density in the GaN channel. Unintentionally doped GaN buffer layers grown by PAMBE are typically conductive with a background electron concentration in the 10^{15}–10^{16} cm^{-3} range originating from nitrogen vacancies and/or native residual donors such as oxygen [1]. Thus, conduction between source and drain contacts can occur not only through the 2DEG but also through an undesirable leakage path in the GaN buffer underneath the 2DEG channel. For good pinch-off behavior, this parasitic current through the GaN buffer (shown in Fig. 4.1) must be minimal or absent. Therefore, the growth of semi-insulating GaN buffer layers is needed. This can be accomplished by the introduction of acceptor-like deep levels using carbon (C) [2,3] or iron (Fe) [4] doping. The C or Fe doped GaN buffer layer is used as a back barrier underneath a thin undoped GaN channel [3]. This can suppress the off-state leakage current and significantly increase the breakdown voltage and the current on-off ratio of the transistors [3]. However, the incorporation of deep levels in the semi-insulating buffer layers was shown to enhance the current collapse of the transistors due to an increase in defects density and charge trapping in the GaN bulk [3,5,6].

Back barriers can be formed by GaN/AlGaN or GaN/AlN heterojunctions [6–13] without the introduction of deep level dopants. In that case, an energy barrier is created at the bottom interface due to the polarization difference between the channel and back barrier, which can limit the penetration of electrons in the buffer layer under high bias operation by lifting upward the conduction band below the channel [14,15] (Fig. 4.1). This decreases the sub-threshold drain leakage current, increases the breakdown voltage [14,15] and mainly in short gate lengths where very high electric fields are induced close to the gate, a back barrier may decrease current collapse effects [16]. In the case of a single heterojunction AlN/GaN HEMT (SHEMT) without a back barrier, electrons can easily spill over into the buffer since the confinement of electrons is weak because there is no essential barrier towards the buffer (Fig. 4.1). Especially in high-quality GaN buffer layers (typically thicker than 2 μm), where the trap density formed by threading dislocations



NOMINALLY UNDOPED GaN is n-type $(10^{16} cm^{-3})$

For a 2 µm thick GaN buffer :

$$N_{buffer} \sim 10^{16} cm^{-3} \times 2 \cdot 10^{-4} cm = 2 \cdot 10^{12} cm^{-2}$$

$$N_s \sim 10^{13} cm^{-2}$$

$$\frac{I_{buffer}}{I_{channel}} \sim 20\% \ (very\ high)$$

Fig. 4.1 Simulated conduction band diagrams of single heterojunction AlN/GaN HEMT (SHEMT) and double heterojunction AlN/GaN/AlN HEMT (DHEMT) structures. In the SHEMT, spill-over of electrons in the buffer occurs due to their insuffiecient confinement in the quantum well because there is no barrier towards the buffer. In the DHEMT case, the AlN back barrier reduces electron injection into the buffer under high bias voltage by raising the conduction band edge in the buffer with respect to the channel.

is reduced, the electron mobility in the buffer is higher, resulting in an overall higher electrical conductivity and a pronounced sub-threshold leakage current, which causes an early device breakdown [10]. In this work, an AlN buffer layer was used, which offers the maximum electron confinement by providing the optimum back barrier for a GaN channel due to its large band gap and band offset, as well as the high built-in polarization-induced electric field confining carriers inside the GaN [12,17,18]. The proximity of this negative polarization charge to the top AlN/GaN interface, such as in GaN quantum well (QW) structures [12,17], also allows one to modify the 2DEG density for a given AlN top barrier thickness and may be used for the design and realization of normally-off HEMT structures [17].

Another particularly interesting characteristic of the AlN/GaN/AlN double heterostructures studied in this work, is the incorporation of a thin GaN channel/buffer layer and a thin AlN buffer/nucleation layer on an insulating substrate (sapphire). A thin heteroepitaxial layer will contain a higher density of dislocations compared to a thicker buffer layer [19]. However, the reduction of electron mobility due to increased scattering may reduce the leakage current and increase the breakdown voltage for thinner GaN buffers [10,19]. Threading dislocations with an edge type component will also compensate unintentional donors and increase the resistivity of the layers [20]. The early work of Wu et al. [21] demonstrated the increase of breakdown voltage up to 340 V for AlGaN/GaN HEMTs, by reducing to 0.4 μm the thickness of the GaN buffer layer on sapphire substrate. Recently, current on-off ratios higher than 10^9 were demonstrated for InAlN/GaN HEMTs, using ultrathin GaN/AlN buffer layers on sapphire substrates [22-24]. The reduction of the GaN buffer/channel layer thickness from 500 nm to 200 nm was found [22] to reduce the off-state leakage current of InAlN/GaN HEMT devices from 1.2×10^{-9} Amm^{-1} to 1.8×10^{-10} Amm^{-1}, respectively.

Finally, a good insulating substrate is required for high voltage and high frequency operation. The sapphire substrate is attractive for specific applications considering its excellent insulating properties and low cost compared to Si and SiC, respectively. Anyway, it is a convenient (low cost, high quality) insulating substrate to evaluate ideas for heteroepitaxial HEMT structures that could be transferable also to other insulating substrates, such as SiC.

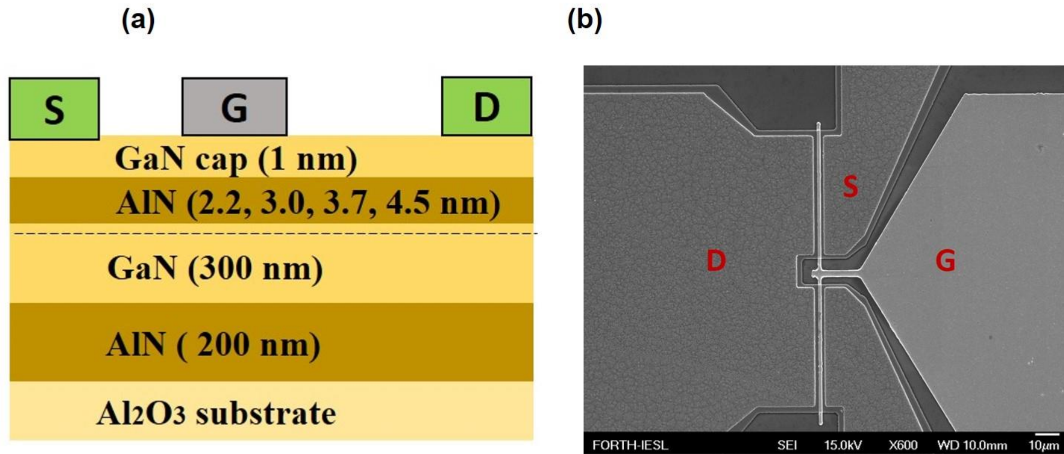


Fig. 4.2 (a) Schematic of the fabricated AlN/GaN/AlN HEMTs and (b) SEM image of a HEMT device.

4.2 Experimental details

The investigated HEMT structures consisted of an ultrathin 2.2 – 4.5 nm AlN barrier and 1 nm GaN cap layer on a thin GaN/AlN buffer layer (Fig. 4.2). The case of a relaxed GaN thin buffer layer on a thin AlN buffer-nucleation layer was considered. The double barrier HEMT structures were analyzed and the effects of AlN (top) barrier thickness on 2DEG density, transport properties and the current and threshold voltage of ~1 μm gate-length HEMT transistors, were evaluated. An extensive study of the current instabilities has been accomplished for evaluating the extent of any trapping effects due to the very thin HEMT heteroepitaxial structure (~0.5 μm total thickness), as well as the intrinsic sensitivity to surface traps of the HEMT structures.

The metal-polarity AlN/GaN/AlN double heterostructures were grown heteroepitaxially on insulating Al_2O_3 (0001) substrates by PAMBE [25,26] and consisted (from top to bottom) of (a) 1 nm GaN cap, (b) an AlN top barrier with nominal thickness (t_b) of either 2.2 nm, or 3 nm, or 3.7 nm, or 4.5 nm, (c) a 300 nm GaN channel-buffer layer, and (d) a 200 nm AlN back barrier and nucleation layer on the sapphire substrate (Fig. 4.2). The substrate preparation and nitridation conditions were according to the optimum conditions determined in previous works [25,26]. The growth of the 200 nm AlN nucleation-buffer layer on sapphire was carefully optimized, to provide a smooth surface for the overgrown layers.

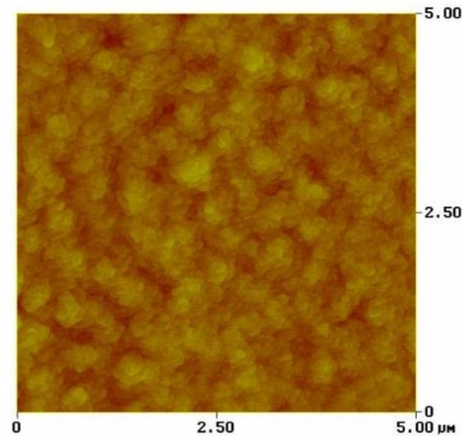


Fig. 4.3 AFM micrograph showing the surface of a 200 nm AlN layer grown by PAMBE on (0001) sapphire substrate. The z-axis range is 2.6 nm.

Figure 4.3 shows an AFM micrograph of the surface morphology of an optimized 200 nm AlN nucleation layer. A very smooth surface is observed with rms roughness of 0.3 nm for a 5 x 5 μm scan. A very smooth AlN nucleation layer surface is very critical for the overgrowth of a thin HEMT structure with a very abrupt AlN/GaN 2DEG interface. The 300 nm thickness of the GaN channel-buffer layer is relaxed on the AlN layer as it is much higher than the critical thickness of the GaN/AlN heterostructure [17,27]. Only a very thin GaN layer forming a QW between the AlN barriers could be grown strained on the AlN lattice, but this would significantly reduce the sheet density and mobility of the 2DEG channel [12,17].

HEMT devices without surface passivation were fabricated, beginning with device isolation by reactive ion etching, using BCl_3/Cl_2, down to the insulating Al_2O_3 substrate. This prevents cross talk between devices through the buffer layer and allows gate probe pads to be placed directly on the insulating substrate. Ti/Al/Ni/Au metal stacks were deposited by e-beam evaporation and annealed for ohmic contact formation, whilst Ni/Au was used as the gate metal. The gate length dimensions were $L_g \sim 1$ μm and width $W_g \sim 50$ μm. The source-drain and gate-drain distances as measured by Field Emission Scanning Electron Microscopy (FE-SEM), were $L_{sd} \sim 4$ μm and $L_{gd} \sim 2$ μm, respectively.

4.3 Polarization effects

To determine the equilibrium energy band profiles and carrier distributions of the HEMT structures and the effects of AlN barrier, a self-consistent Schrödinger-Poisson solver was employed in our research group [28]. All relevant parameters, used in the calculations, were according to Ambacher et al. [29], and the conduction band discontinuities were according to Van de Walle and Neugebauer [30]. For the boundary conditions, the energy distance $(E_C-E_F)_S$ between E_C and E_F at the GaN surface (surface potential) was set at 0.8 eV, while neutrality (flat bands) was considered at the bottom (AlN) side. For donor concentrations, we assumed $N_D=10^{16}cm^{-3}$ for GaN and $N_D=10^{13}cm^{-3}$ for AlN. The calculated conduction band (E_c) profile for the top region of the structure, where the 2DEG forms, is shown in Fig. 4.4 and the electron concentration profiles are shown in the inset of Fig. 4.4 (b). The increase of the AlN barrier thickness, t_b, reduces the built-in electric field within the AlN barrier and deepens the 2DEG QW, with corresponding increase of N_S. The distance of the peak 2DEG concentration from the top AlN/GaN interface is 1.4, 1.1, 1.0, and 0.9 nm for t_b equal to 2.2, 3.0, 3.7, and 4.5 nm, respectively.

Figure 4.4(a) shows the calculated equilibrium band diagram for the HEMT structure with t_b=4.5 nm. The main plot gives an expanded view of the top region of the structure, where the 2DEG confining QW is formed, whilst the inset shows the band profile for the entire HEMT structure (from the surface of the 1 nm GaN cap to the bottom side of the AlN nucleation layer). The bottom GaN/AlN interface induces a strong electric field within the thin 300 nm GaN buffer layer and a large barrier for electron motion toward the substrate. It should be also noticed that at the bottom GaN/AlN interface the valence band crosses the Fermi level, which can cause an accumulation of holes of the order of 10^{13} cm^{-2}. In structures where a two-dimensional hole gas (2DHG) coexist next to the 2DEG, at first glance it may seem possible that both the 2DEG and the 2DHG would be probed by Hall effect measurements. However, due to a much superior mobility of the 2DEG compared to the 2DHG, almost all of the probing current flows through the 2DEG and thus the measured sheet carrier density and mobility are entirely prevailed by the 2DEG [31]. The presence of the theoretically predicted 2DHG would depend on the amount of defect-induced charges, which have been ignored in our calculations. In our thin heteroepitaxial structures, the bottom GaN/AlN interface is located at 200 nm above the highly lattice-mismatched Al_2O_3 substrate. Thus, a high defect density is expected that may compensate the polarization induced charges.

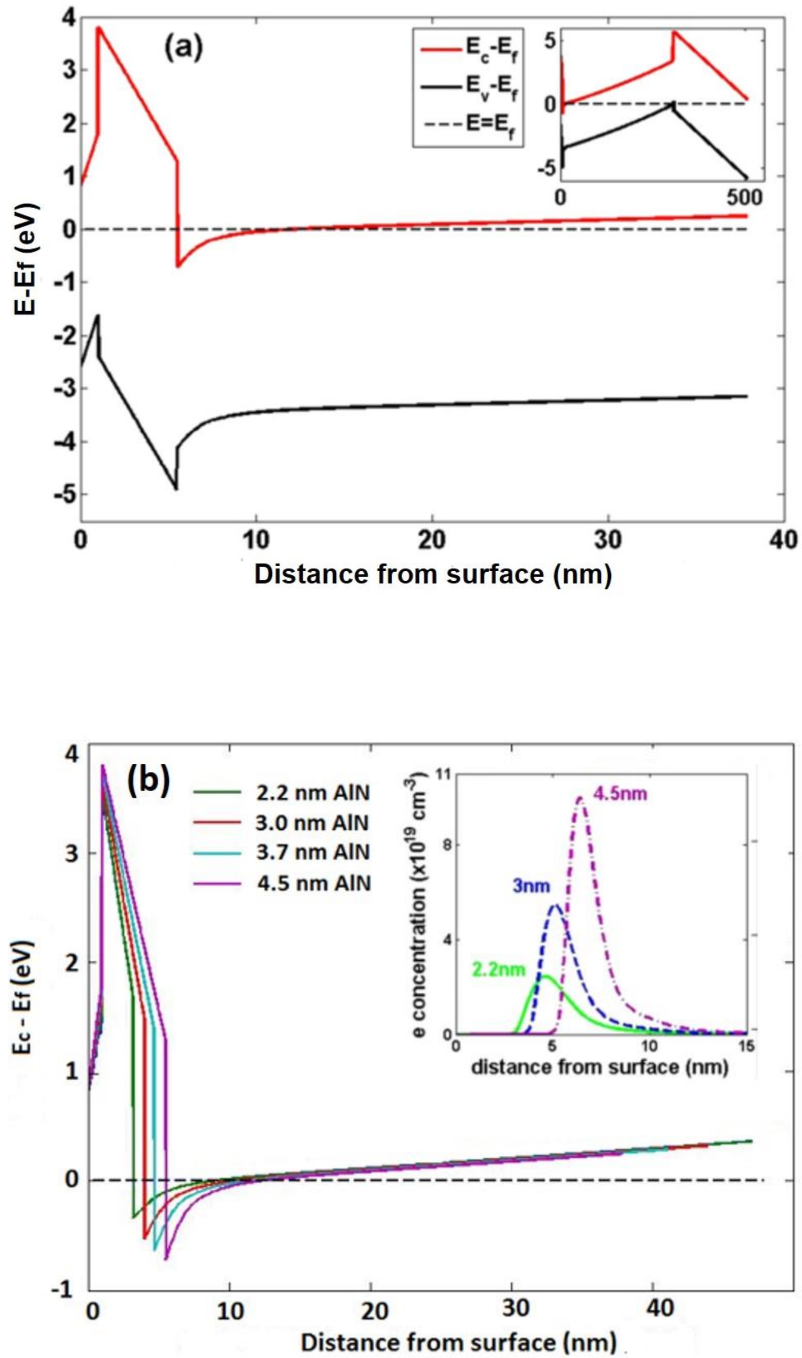


Fig. 4.4 (a) Simulated band diagram for the top region of the structure [1 nm GaN/4.5 nm AlN/300 nm GaN/200 nm AlN]. The insert diagram presents the band profile for the entire structure. (b) Simulated band diagrams for all the thicknesses. The inset shows the electron distribution for t_b = 2.2, 3.0, or 4.5 nm.

4.4 Electrical properties

The 2DEG N_s values were determined experimentally by Hall-effect and C-V measurements and compared with the calculated ones, as shown in Fig. 4.5(a). The N_S values were extracted from C-V measurements (the measurement frequency was 1 MHz) on 100 μm diameter circular Schottky diodes by integrating the electron concentration for diode bias from the negative threshold voltage (V_{th}) that pinches-off the 2DEG up to 0 V. The theoretical and experimental N_S values are in a very good agreement, suggesting a minor impact of the crystalline defects that increase near the heteroepitaxial interface. The highest measured N_s was determined for the HEMT structure with t_b=4.5 nm, and it was 2.2 x 10^{13} cm^{-2} from Hall-effect measurements and 2.0 x 10^{13} cm^{-2} from C-V measurements, whilst SCSP calculation resulted to 2.1 x 10^{13} cm^{-2}.

The electron mobility increases rapidly for AlN barrier thickness above t_b=2.2 nm, with the maximum value among the different samples being 900 cm^2/Vs for t_b=3.0 nm (Fig. 4.5). A small reduction was observed for higher AlN barrier thicknesses, reaching the value of 703 cm^2/Vs for 4.5 nm AlN. This could be attributed to an increase in the interface roughness scattering as the charge distribution shifts closer to the heterointerface at high carrier concentrations [32].

The observed R_{sh}, as obtained from Hall-effect measurements, were in close agreement with values obtained from TLM test patterns (Fig. 4.5). A reduction of R_{sh} with t_b was observed, with the minimum value being 409 Ohm/sq for the 4.5 nm AlN barrier. An exceptional case is the sample with t_b=2.2 nm which exhibited very high variations in R_{sh} possibly due to thickness variations in the ultrathin barrier. Cao reported [33,34] that in such ultrathin barriers (~2 nm) due to the high surface rougness scattering, which causes degradation of mobility, the R_{sh} values can be too high (> 2000 Ohm/sq) to be accurately measured [33,34].

The measured average contact resistance R_c, as obtained from TLM test patterns, increased with AlN t_b, from 0.86 Ohm mm for t_b=2.2 nm to 2.1 Ohm mm for t_b=4.5 nm (Fig. 4.5), as has been also reported by Deen et al. [35]. It is observed that the thickness of the barrier that the metallization must diffuse, during annealing, to contact the 2DEG plays an important role in low ohmic contact formation [36]. Although an opposite trend could be also expected, since a lower 2DEG density below the contacts in thinner barriers could result in a higher R_c, this is not the case here. The thin AlN barriers, possibly, allow metals to diffuse more easily during the temperature

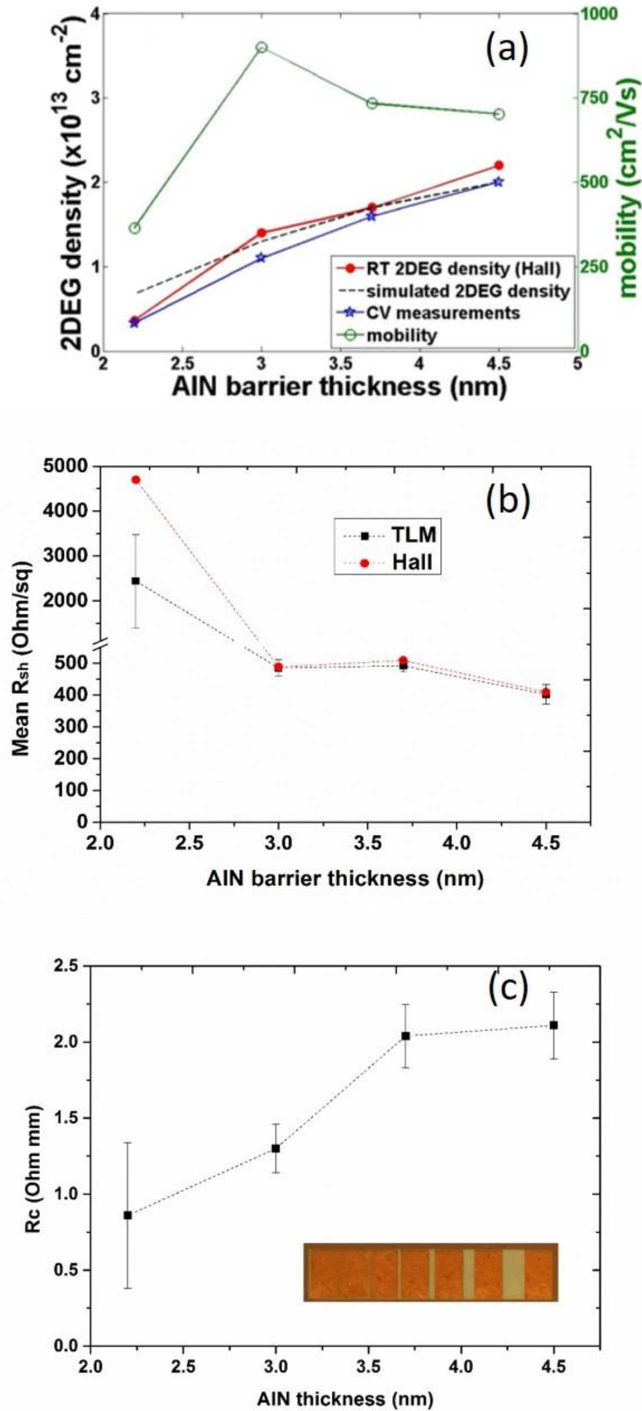


Fig. 4.5 (a) Theoretical and experimental 2DEG density and electron mobility, (b) mean values of sheet resistance R_{sh}, obtained from Hall-effect and TLM measurements, and (c) mean contact resistance R_c (obtained from TLM measurements), as a function of AlN barrier thickness where the inset shows the measured TLM pattern. Error bars are showing the standard deviation range.

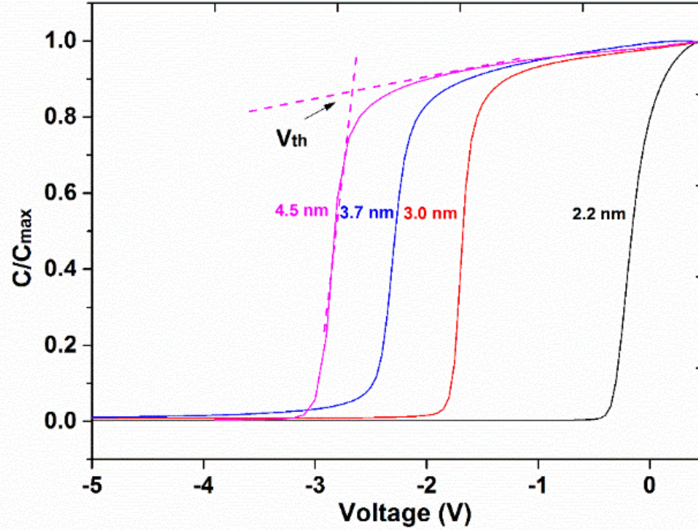


Fig. 4.6 Normalized capacitance-voltage characteristics for the AlN/GaN/AlN heterostructures measured at room temperature and frequency f = 1MHz.

---

annealing and contact with the 2DEG, thus improving R_c [36]. Electron tunneling through the AlN barrier is also dramatically limited by increasing its thickness, considering the large bandgap of AlN.

4.5 C-V characterization of Schottky contacts

All the structures exhibited high quality C-V profiles with sharp pinch-off characteristics and extremely low residual GaN buffer capacitance at high reverse bias voltages (Fig. 4.6). The plateau capacitance of the curve is associated with the 2DEG and corresponds approximately to the capacitance of the parallel plate capacitor with AlN as a dielectric. For a given AlN barrier thickness, the length of the C-V curve plateau depends on the sheet carrier density of the 2DEG. For thicker AlN barriers (higher sheet carrier densities), the capacitance decrease occurs at higher reverse voltages, and thus V_{th} shifts towards higher values. The volume carrier concentration was measured from the C-V profile using $N_{C\text{-}V} = (C^3/q\varepsilon_0\varepsilon)(dV/dC)$ as a function of depth $z = \varepsilon_0\varepsilon/C$. From the volume profile, the apparent sheet electron density can be computed by integration as a function of applied bias voltage.

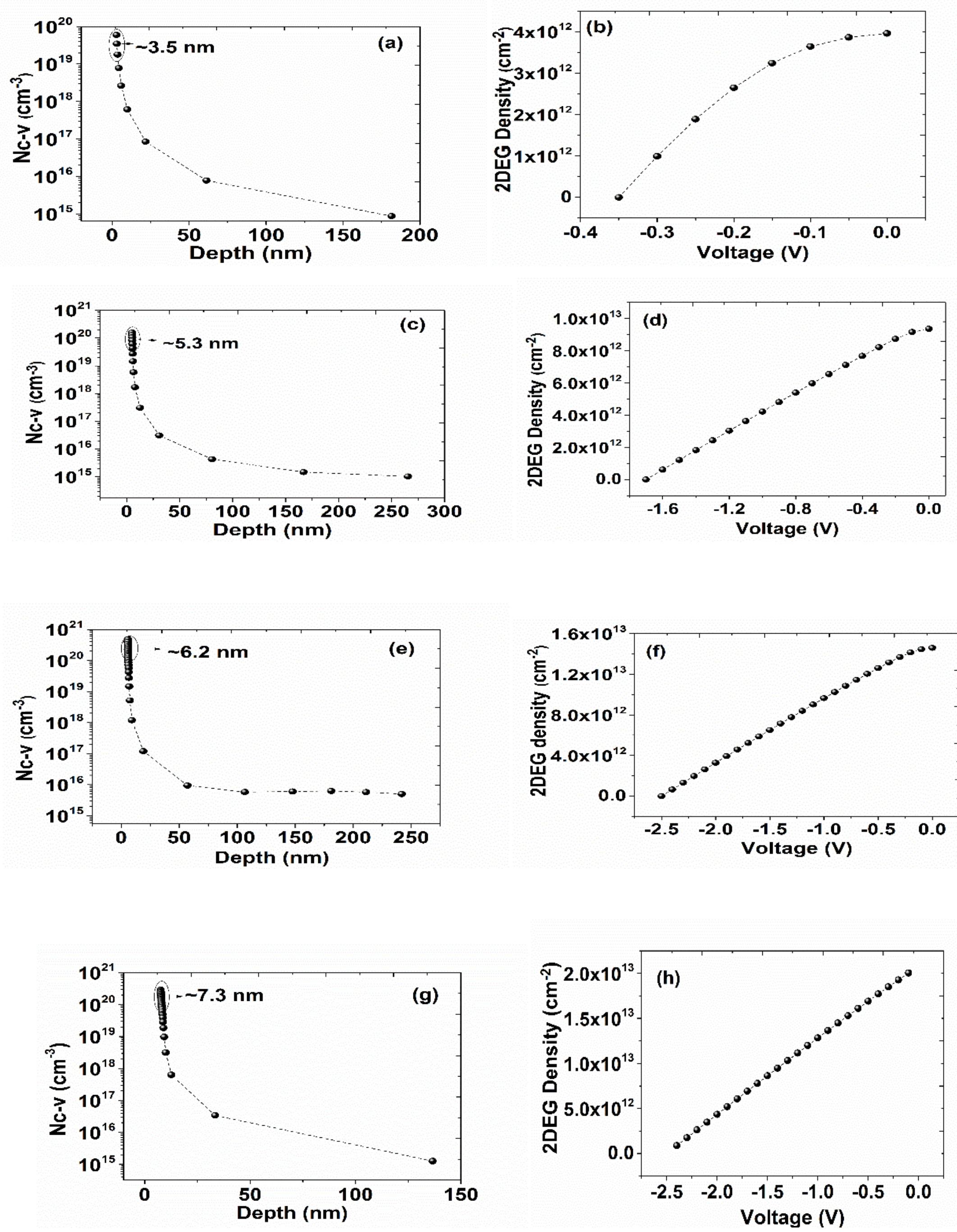


Fig. 4.7 (left column) Carrier concentration vs depth profile and (right column) integrated electron density, deduced from C-V curves for (a-b) 2.2, (c-d) 3, (e-f) 3.7 and (g-h) 4.5 nm AlN barrier.

Figure 4.7 shows the typical carrier concentration profiles for all the structures. A high carrier concentration is observed at the AlN/GaN interface and a low background carrier density is observed at the bottom of the GaN buffer layer, demonstrating a sharp carrier confinement. An estimation of the 2DEG density as a function of applied voltage was obtained by integrating the concentration vs. depth profile with respect to the applied voltage, as shown in Fig. 4.9. The 2DEG density changes linearly with the applied voltage and the values are in close agreement with Hall-effect measurements.

4.6 DC characterization of AlN/GaN/AlN HEMT transistors

The previously described 2DEG results (N_S, mobility, pinch-off) were consistent with the dc I-V measurements of the fabricated HEMT devices. For statistical revelance, more than 200 devices have been characterized from each sample. Figure 4.8 shows the I-V characteristics of representative transistors. The structure with t_b = 3.0 nm exhibited a maximum drain-source saturation current (I_{dssmax}) of 1.1 A/mm with V_{gs} of +3 V. The I_{dssmax} was the same for t_b=3.7 nm, while a slightly lower value of ~1.0 A/mm was obtained for t_b=4.5 nm. The I_{dss} at V_{gs}= 0 V (I_{dss0}), versus the AlN barrier thickness is shown in Fig. 4.9 and exhibits the same dependence on t_b as that observed for N_S in Fig. 4.5(a). The on resistance (R_{on}) of the devices, extracted at gate-source voltage V_{gs}=0 V from the linear region of DC I–V curves, was in the range 3.9 – 4.8 Ohm·mm for t_b between 3.0 – 4.5 nm (Fig. 4.9). However, the 2.2 nm ultrathin AlN layer exhibits a much higher R_{on} exceeding 11 Ohm·mm due to very low carrier density and the resulted high sheet resistance values.

The measured transconductance-voltage (G_m-V_{gs}) characteristics of the devices are shown in Fig. 4.10. The intrinsic G_{mi} ($G_{mi} = G_m/1-G_mR_s$) was also extracted by correcting for the effects of parasitic resistance R_s, where $R_s = R_c + R_{s(a)}$; R_c is the contact resistance of the source electrode and $R_{s(a)}$=R_{sh}*(L_{gs})/W is the source access resistance due to the biased gate-to-source channel region (Fig. 4.11(a)). The maximum extrinsic g_m was 330 mS/mm for the 3 nm AlN barrier and reduced for higher t_b, approaching the value of 250 mS/mm for 4.5 nm. From the figures, it is obvious that the optimal AlN thickness for maximizing both drain current and transconductance occurs at the 3 nm AlN barrier thickness where 2DEG mobility is also maximized.

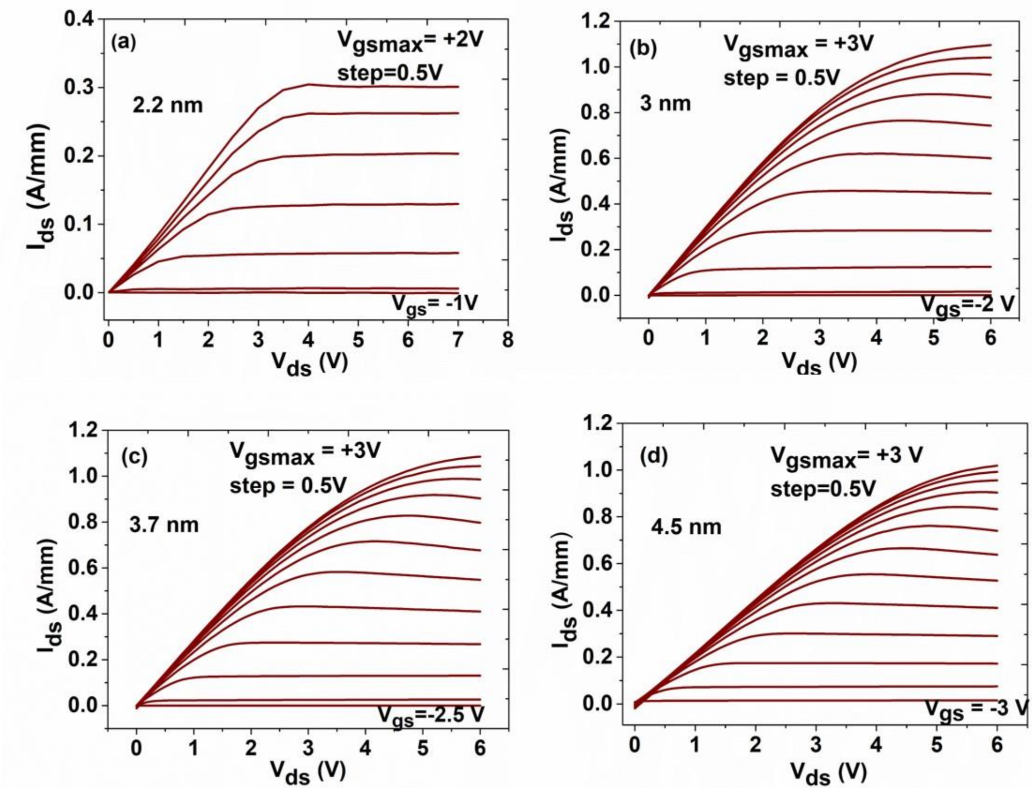


Fig. 4.8 Drain-source current characteristics for varied AlN barrier thicknesses.

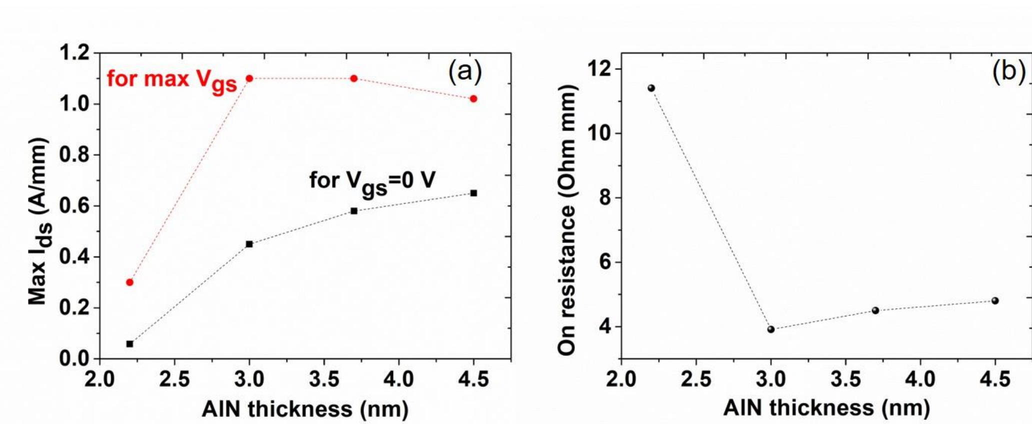


Fig. 4.9 (a) Drain-source saturation current measured at the maximum V_{gs} and V_{gs}= 0 V, and (b) on-resistance, R_{on}, as a function of AlN thickness, as evaluated from the slope of the HEMT I_{ds}–V_{ds} curve at V_{gs}=0 V.

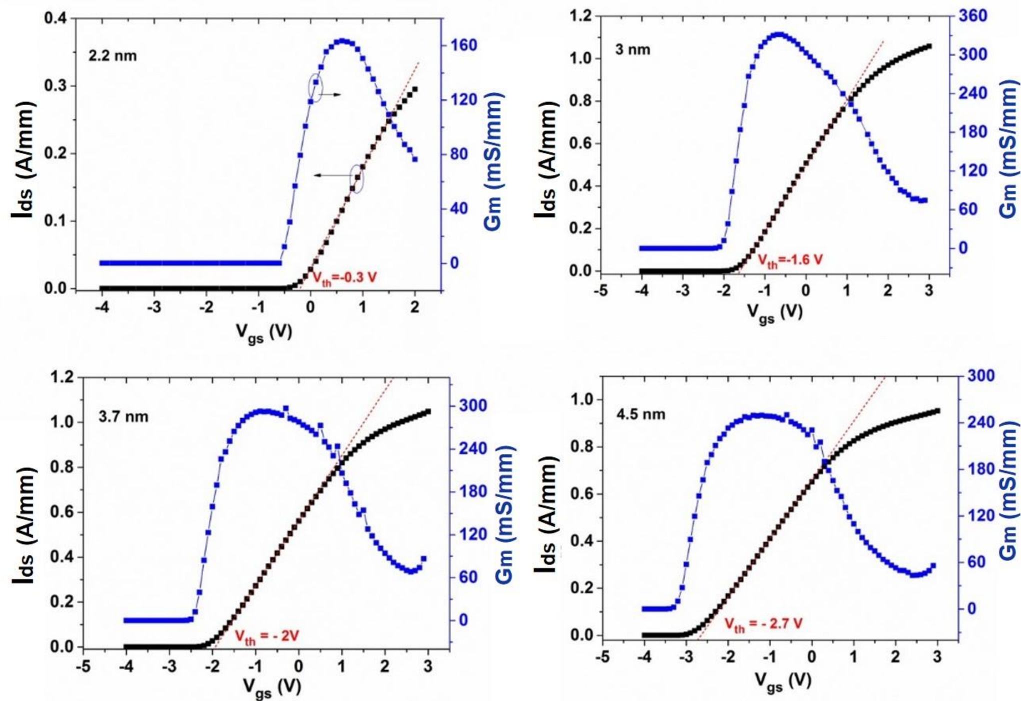


Fig. 4.10 I_{ds}-V_{gs} and G_m-V_{gs} plots for various AlN barrier thicknesses measured at the saturation regime (V_{ds}=5 V).

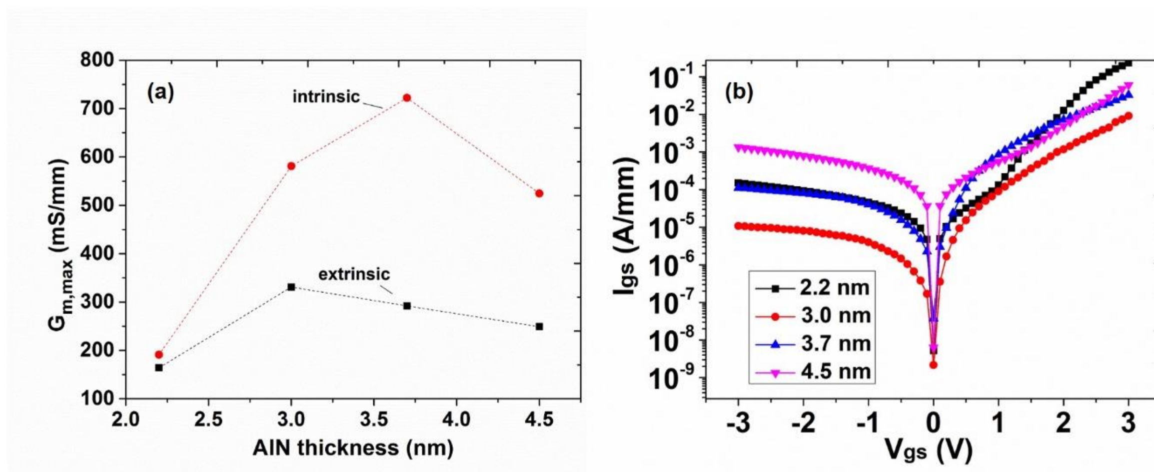


Fig. 4.11 (a) Maximum G_m versus AlN thickness and (b) gate leakage currents for various devices.

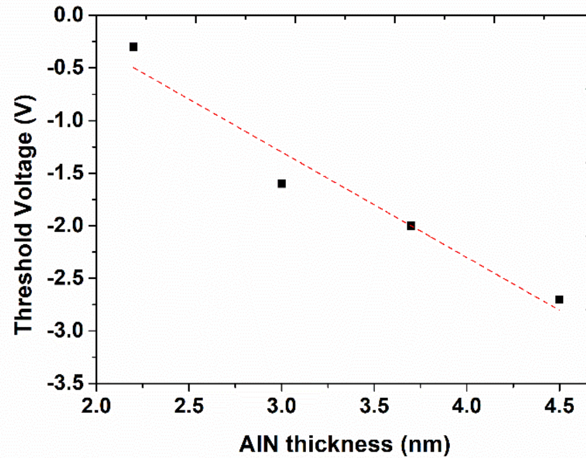


Fig. 4.12 Threshold voltage dependence on AlN barrier thickness, as extracted from the transfer (I_{ds}-V_{gs}) curves.

In addition to this, this sample exhibited the lowest gate leakage currents under pinch-off conditions (~10^{-5} A/mm at V_{gs}=-3 V), as shown in Fig. 4.11(b). It is interesting to note that I_{gs} was ~2 orders of magnitude higher for the thicker 4.5 nm AlN barrier, although the total gate-to channel thickness is increasing, causing a ~32% reduction in G_m compared to 3 nm AlN. This could be related to a different defect density in the grown buffer layers. However, it may also result from the onset of lattice relaxation at the 4.5 nm AlN barrier structure, which is close to the 5 nm critical thickness reported by Adikimenakis et. al [37]), and the introduction of microcracks for relaxation of the stress of the AlN layer. The presence of microcracks or other defects could result in the creation of current paths through the barrier that increase the gate leakage [36].

From the transfer characteristics of Fig. 4.10, the transistor threshold voltage V_{th} was also extracted, defined as the gate-bias intercept of the linear extrapolation of the drain current from the point of the peak transconductance. The reduction of AlN barrier thickness increases the HEMT device V_{th}, from -2.7 V for t_b=4.5 nm to -0.3 V for t_b=2.2 nm (Fig. 4.12). The extracted values were in close agreement with V_{th} extracted from C-V measurements on Schottky contacts; in the latter case, V_{th} was defined as the bias voltage where the linear extrapolations of the capacitance curves of the accumulation and depletion regions intersect (see Fig. 4.6).

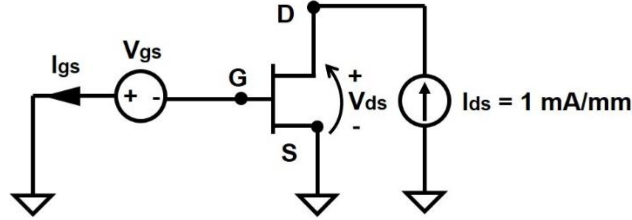


Fig. 4.13 Schematic setup of the drain current injection technique (ref. [44,45]).

The transistors were also submitted to off-state electric breakdown measurements. AlN/GaN HEMTs generally show [38-43] a limited applied V_{ds} range and sustain low V_{br} compared with the inherent material properties. Although gate insulators for gate leakage current suppression were used in many works to avoid high tunneling currents, the reported devices showed low off-state V_{br} due to gate insulator failure resulting premature off-state breakdown [38-43]. Chabak et al [38] reported a maximum V_{ds} of 20 V for a fixed I_{ds} = 50 mA/mm and drain-source distance L_{ds} = 2.7 μm for HEMTs with a plasma-oxidized gate insulator, whereas Meyer et al [39] measured an off-state V_{br} of 35 V for I_{ds}=1 mA/mm and L_{sd} = 3 μm for HfO_2/AlN/GaN HEMTs. Corrion et al [40] reported an enhancement-mode AlN/GaN/AlGaN double heterostructure FET with L_{sd} = 1 μm and V_{br} of 57 V, while Taking et al [41] demonstrated a similar value of 58 V for an AlN/GaN MOS-HEMT with L_{sd} = 3.5 μm.

Many different measurement and extraction techniques and a variety of criteria have been cited in the literature to elicit V_{br} values. Several authors define V_{br} as the drain voltage of the turned-off device where a sharp rise in I_{ds} occurs on the output I-V characteristics. It does not necessarily imply that breakdown occurs in the channel; it could equally occur between drain and gate. Also, in that case, great care must be taken to limit the current and prevent device destruction. In this work, the drain-current injection technique was used [44,45] for the measurement of off-state V_{br} (Fig. 4.13), which gives insight into the physics of breakdown and provide safe operation of the device. To characterize breakdown, the transistor is biased with grounded source and a fixed predefined drain current, commonly but not always 1 mA/mm, the gate-source voltage is ramped down from a zero bias to below threshold, and V_{ds} and I_{gs} are monitored.

Figure 4.14 shows the off-state V_{br} characteristics of the double heterostructure AlN/GaN/AlN HEMT devices. When V_{gs} starts to sweep down from zero voltage and the transistor is on-state, V_{ds} is close to zero because the channel is conducting and only a minor drain bias is needed on the drain to obtain the very small I_{ds}=1 mA/mm. As V_{gs} is further lowered toward pinch-off, an increase in V_{ds} is observed which is necessary to keep the fixed I_{ds} flowing; the I_{gs} increases also (in magnitude) due to the reverse bias and starts becoming significant. The peak of the V_{ds} marks the drain-source breakdown voltage V_{br}. Moreover, at the point of maximum V_{ds} (V_{br}) the I_{gs} becomes equal to I_{ds} for all the devices, i.e. $I_{gs}=-I_{ds}=-1$mA/mm, indicating a drain current coming out of the gate (gate breakdown). Defect-assisted tunneling [46], thermionic emission at the Schottky gate [46] and defect-related leakage paths [47,48] are possible relevant gate-related breakdown current components which may significantly contribute to leakage through the AlN barrier and may be responsible for the device degradation.

Interestingly, it is observed that the highest V_{br} of 70 V was measured for the 3 nm thick AlN, while the lowest V_{br} value of 16 V was measured for the 4.5 nm thick AlN barrier HEMT for a fixed I_{ds}=1 mA/mm. This difference is related with the ~2 orders of magnitude higher gate leakage current observed in HEMTs with the thicker 4.5 nm AlN barrier.

Figure 4.15 exhibits the off-state breakdown characteristics for a (reference) single AlN/GaN HEMT structure fabricated by growing a 1 nm GaN cap/3 nm AlN top barrier/500 nm GaN buffer layer on a commercially available 2 μm GaN/Al_2O_3 substrate. For the single AlN/GaN, V_{br} was 26 V at I_{ds} =1mA/mm which was increased to 36 V when the injected fixed drain current I_{ds} increased to 10 mA/mm. This value is lower when compared with the V_{br} value of 70 V measured from the double heterostructure AlN/GaN/AlN HEMT with the same 3 nm AlN barrier thickness.

In addition to this, it can be observed that the breakdown mechanisms may differ between structures with different heteroepitaxial design. In the single AlN/GaN HEMT, the subthreshold gate current I_{gs} was very small compared with I_{ds}, even at the maximum V_{ds} (i.e. V_{br}) which implies a channel/buffer breakdown mechanism [44,49]. GaN buffer layers grown by PAMBE are typically conductive with a concentration in the 10^{15}–10^{16} cm^{-3} range, as mentioned in par. 4.1,

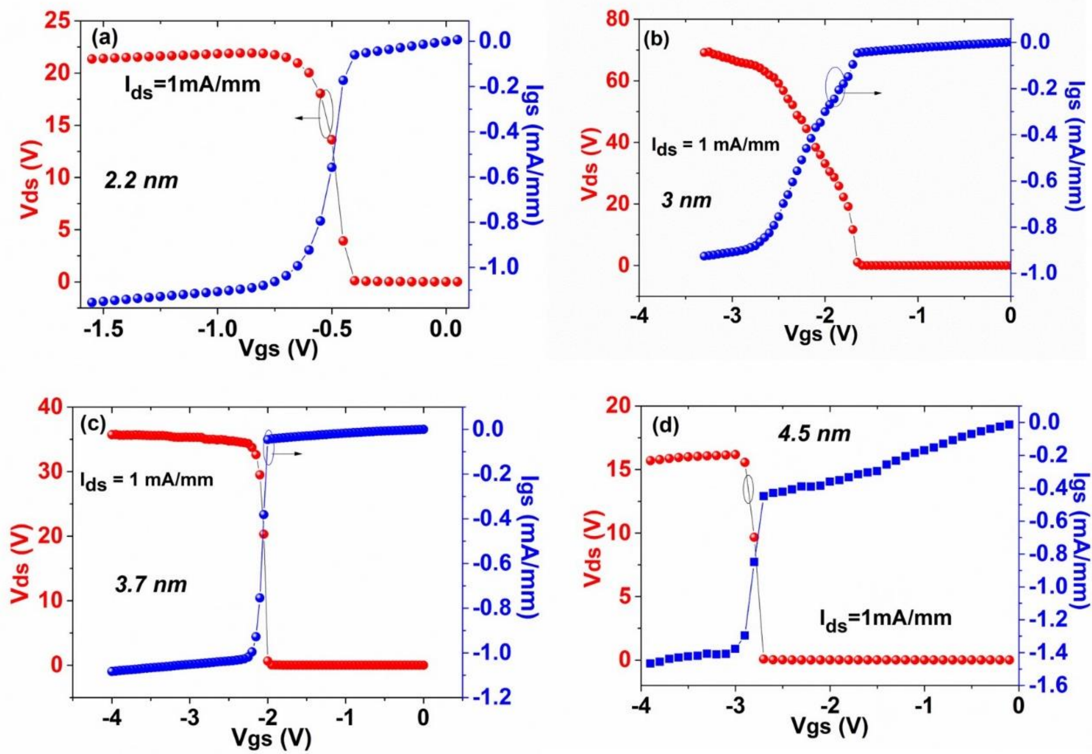


Fig. 4.14 Off-state breakdown characteristics for the double AlN/GaN/AlN HEMT heterostructure devices. The gate-drain distance is L_{gd}=2 µm and a fixed I_{ds}=1 mA/mm was used.

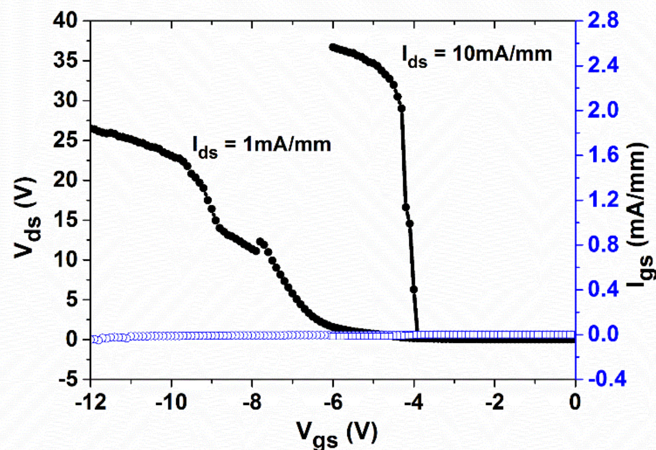


Fig. 4.15 (left) Off-state breakdown characteristics for a single 3 nm AlN/GaN HEMT heterostructure with 2.5 µm GaN buffer layer. The gate-drain distance is L_{gd}=2 µm and two fixed I_{ds} values were predefined (1 mA/mm and 10 mA/mm).

whilst a high electron concentration may also appear at the GaN epilayer/GaN substrate interface due to substrate surface contamination. In a double heterostructure AlN/GaN/AlN HEMT, the bottom interface of the GaN layer with the 200 nm thick AlN buffer-nucleation layer results in an improved confinement that restraints the electron spillover from the quantum well, by raising the conduction band in the 300 nm thin GaN buffer (Fig. 4.1), and limiting the access of electrons to the highly defective epilayer/substrate interface, which could decrease V_{br}.

4.7 Pulsed characterization of AlN/GaN/AlN HEMTs and of trapping effects

Nowadays, although the technology of GaN-based devices is quite mature, the identity of trapping mechanisms in ultrathin AlN/GaN HEMTs is not well understood. Traps are responsible for a recoverable I_{ds} decrease (or collapse) in the I-V characteristics of transistors determined by the accumulation of electrons at defective states when an external voltage pulse is applied [50]. Electrons can be trapped under the gate and/or throughout the access regions, either at the surface [1,50] or within the epitaxial layers [1,50]. Gate leakage current has been considered to be the source of electrons needed to charge the defective states [1]. Since this current increases at negative V_{gs}, the magnitude of current collapse is expected to increase at V_{gs} close to pinch-off of the channel. If charge trapping occurs under the gate, then the threshold (or pinch-off) voltage of the transistor should change correspondingly [1], given by $\Delta V_{th} = q\ \Delta N_s / C_{AlN}$, where C_{AlN} is the capacitance of the AlN layer and ΔN_s is the change in 2DEG density. This is the gate-lag effect [50] (Fig. 4.16). If charge trapping occurs in the access regions (most importantly in the gate-drain region), either at the surface or within the epitaxial layers, this would have an additional effect: the series resistances (R_s, R_d) will be increased causing also the increase of the on-resistance, R_{on}, and decrease in the drain current and transconductance of devices (Fig. 4.17), since [1,50,51]:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = V_{ds} \frac{\partial (R_{on})^{-1}}{\partial V_{gs}}$$

This is due to a virtual gate effect [52] which is described by a measurement known as drain lag [50] (Fig. 4.17). According to the model developed by Ladbrooke [51], the resistance of the source-gate and gate-drain access regions is related with the surface depletion depth which depends upon the occupied surface-state density. The occupied-state density depends on the available density of states at the surface and the mechanism by which electrons are transported to (and from) those

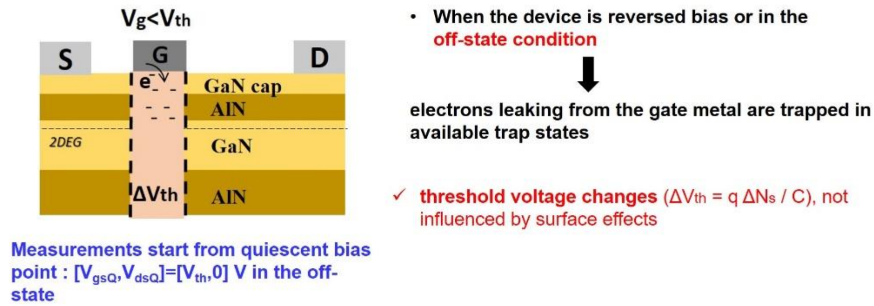


Fig. 4.16 Schematic interpretation of the measurement under gate lag conditions [50].

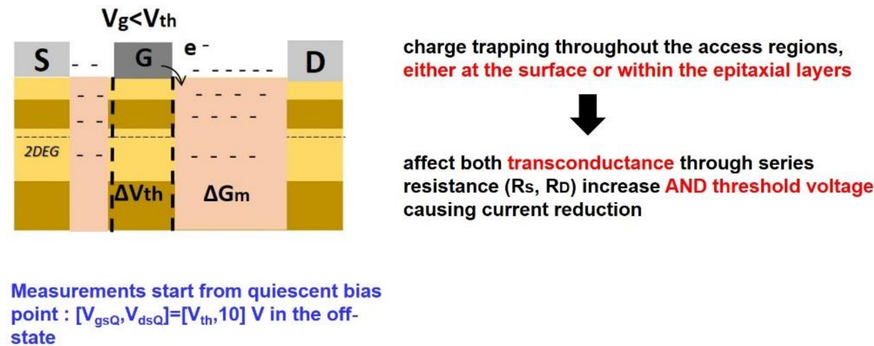


Fig. 4.17 Schematic interpretation of the physical trap charging processes under drain lag measurement [50,51]. When the device is biased in the off-state condition, significant gate electron injection takes place, concentrated, due to the positive V_{ds} applied, at the gate-drain region.

---

states [51]. In an Al(Ga)N/GaN heterostructure, a net positive charge exists on the surface to compensate the negative sheet charge due to electrons in the channel. Neutralizing this surface positive sheet charge by capturing electrons in trap states, is analogous to negatively charging up an imaginary metal gate (referred as virtual gate) on the surface, and hence depleting the channel electrons underneath and giving rise to a second barrier to electron flow along the channel [52]. This is depicted in Fig. 4.18 (a) where the device is biased under pinch-off conditions (the channel is depleted through V_{gs}) and a drain-source bias is applied. Because of the large applied fields in this condition, the surface of the transistor becomes charged in the gate-drain region where the most intense electric field occurs.

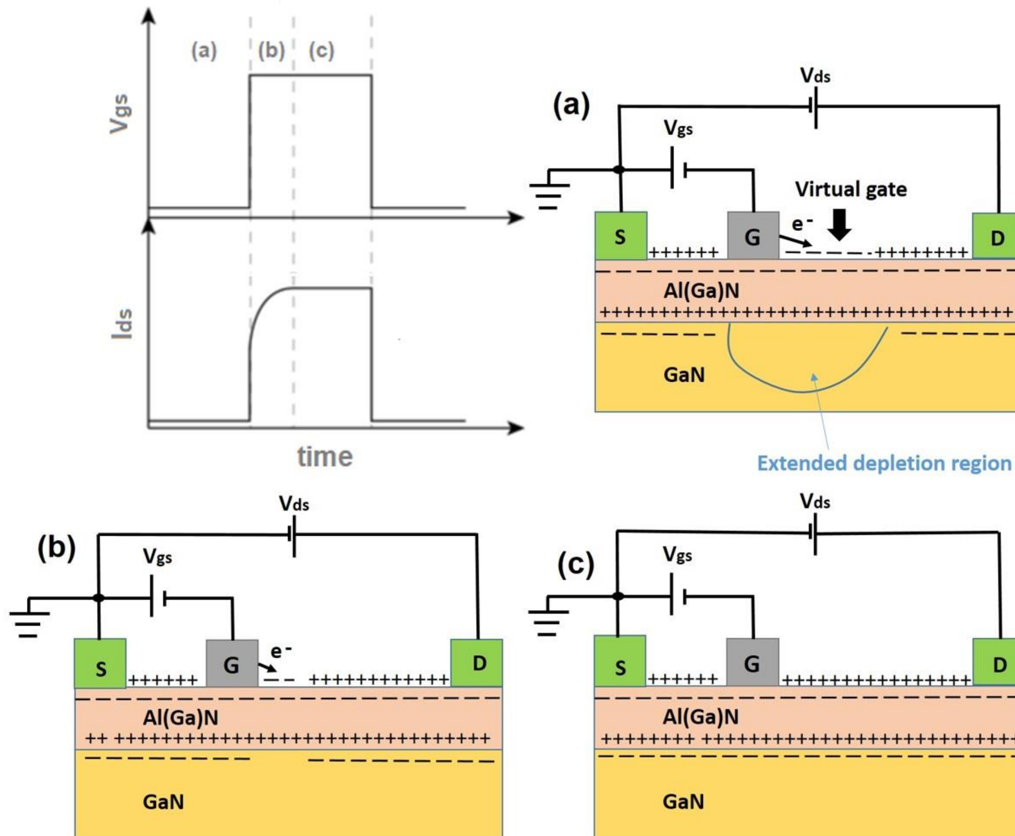


Fig. 4.18 Schematic diagram of the virtual gate effect showing the steps from pinch-off to fully open channel conditions. (a) under a highly negative V_{gs} that pinched-off the channel, (b) application of $V_{gs} > V_{th}$ that resulted to open (but partially depleted) channel and (c) application of $V_{gs} > V_{th}$ for sufficient amount of time, when current reaches its maximum I_{dsmax} value. The time plot of the surface charge and channel depletion is also shown.

Once V_{gs} opens the channel i.e the metal gate is forward biased (Fig. 4.18(b)), electrons trapped in the surface states are removed. However, I_{ds} cannot respond immediately because it takes a discrete amount of time to discharge the access region trap states and the surface region between the gate and drain remains partially charged. Finally, I_{ds} reaches its maximum value after a sufficient amount of time where the traps are discharged (Fig. 4.18 (c)).

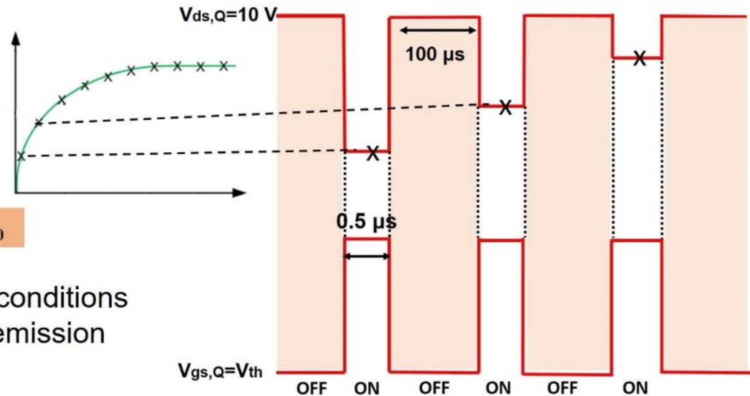


Fig. 4.19 A double pulse with an initial quiescent bias point [V_{gsQ}, V_{dsQ}] is applied to investigate the influence of trapping phenomena on I_{ds}-V_{ds} and I_{ds}-V_{gs} dynamic characteristics.

In this work, pulsed I–V measurements were conducted for the evaluation of trapping effects, with 500 ns pulse duration, which is shorter than the time constant of most traps observed in AlGaN structures [53], and 100 µs period of the square wave signal. Thermal and trapping effects can be minimized under pulsed I-V measurements with the usage of the "cold" quiescent bias point [V_{gs},V_{ds}]=[0,0] V. A negative gate bias V_{gs} at/or beyond the pinch-off bias condition, with V_{ds}=0 V ([V_{gsQ},V_{dsQ}]=[V_{th},0] V) or a high drain–source voltage V_{ds}=10 V ([V_{gsQ},V_{dsQ}] = [V_{th}, 10] V), were used as initial quiescent bias points to evaluate trapping of electrons in the regions immediately under the gate (gate lag) or in the gate–drain access region (drain lag), respectively [54] (Fig. 4.19). The quiescent bias point of V_{dsQ} = 10 V was selected according to the common practice in the specialized literature, such as ref. [50]. The three types of pulsed I_{ds}–V_{ds} characteristics for HEMTs with different AlN barrier thicknesses are shown in Fig. 4.20. The maximum observed saturation current was I_{dsmax}=1.4 A/mm for a 3.7 nm AlN barrier at V_{gs}=+3 V, while devices with the thinnest AlN barrier of 2.2 nm exhibited currents with I_{dsmax}=0.3 A/mm at the highest possible V_{gs}=+2 V (without observing excess gate leakage). The current collapse, observed when cold-pulsed and gate/drain lag I-V characteristics are compared (Fig. 4.20), occurs because the 500 ns pulse width is shorter that the emission time constants of the active traps and electrons captured by traps do not have enough time to be fully emitted.

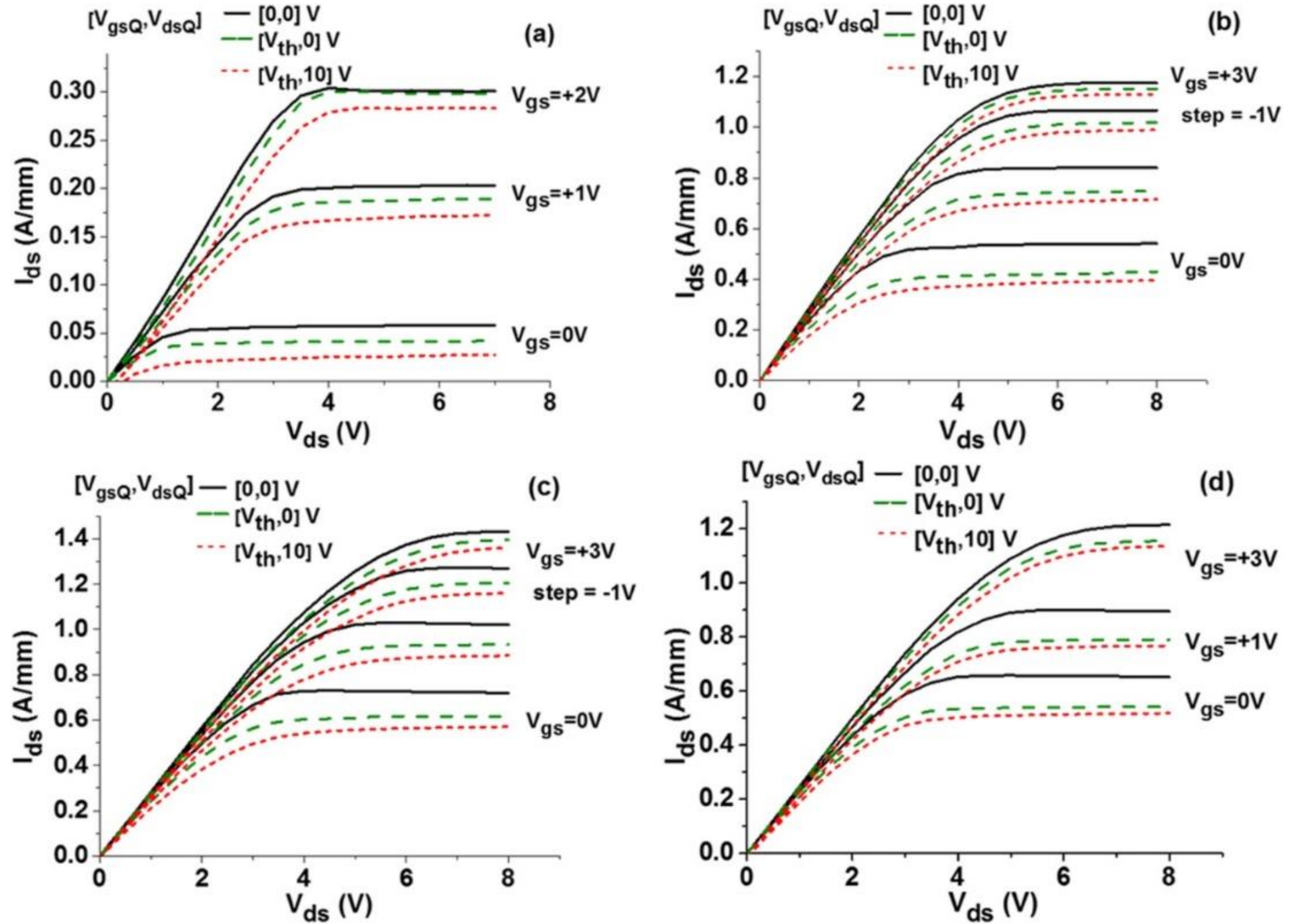


Fig. 4.20 Pulsed I_{ds}–V_{ds} characteristics of HEMT devices for (a) 2.2 nm, (b) 3.0 nm (c) 3.7 nm and (d) 4.5 nm AlN top barrier thickness.

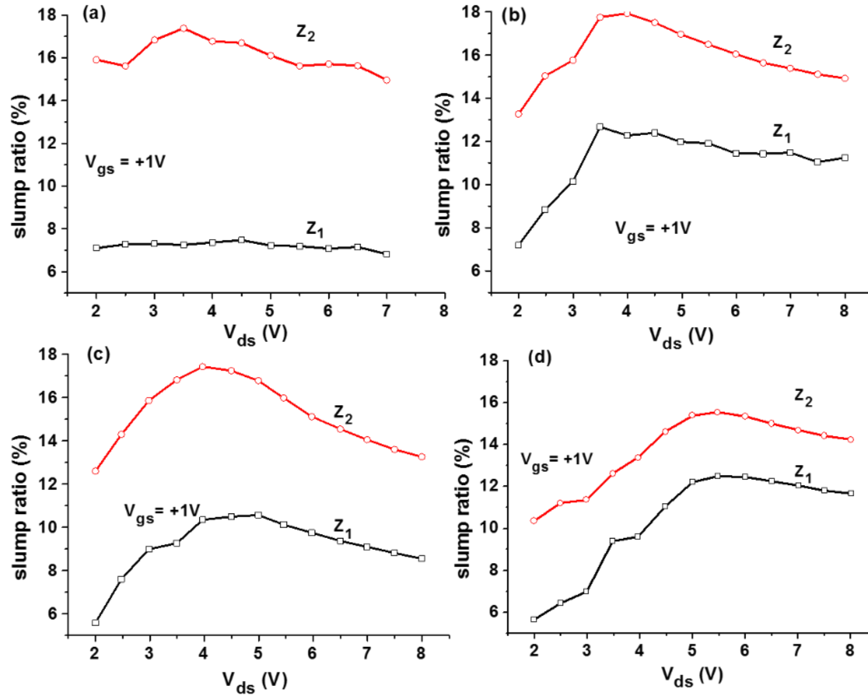


Fig. 4.21 Slump ratios Z_1 and Z_2 versus V_{ds} for HEMTs with AlN top barrier thickness (a) 2.2 nm, (b) 3.0 nm (c) 3.7 nm and (d) 4.5 nm. The Z_1 and Z_2 values were calculated at $V_{gs} = +1V$. Rectangles represent Z_1 and circles represent Z_2 values.

For a quantitative evaluation between the different HEMT devices, the so called [55,56] slump ratios Z_1 and Z_2, defined for gate and drain pulsed from $[V_{gsQ}, V_{dsQ}]$ to a final V_{gs}=+1 V and to V_{ds} varied between 0–8 V, were calculated. The values Z_1, Z_2 are:

$$Z_1 = (I_{ds,VgsQ,VdsQ} - I_{ds,00}) / I_{ds,00} ,$$
$$\text{for } ([V_{gsQ},V_{dsQ}] = [V_{th},0]V), \quad (1)$$
$$Z_2 = (I_{ds,VgsQ,VdsQ} - I_{ds,00}) / I_{ds,00} ,$$
$$\text{for } ([V_{gsQ},V_{dsQ}] = [V_{th},10]V) \quad (2)$$

where $I_{ds,00}$ is the cold pulsed current. Figure 4.21 exhibits the Z_1 and Z_2 slump ratio variations with the drain-source voltage, at $V_{gs} = +1$ V, for all the devices. For $t_b = 2.2$ nm, it is observed that Z_1 was ~7% for V_{ds} between 2 and 7 V, and that Z_2 is more pronounced exhibiting a value of 15-17%.

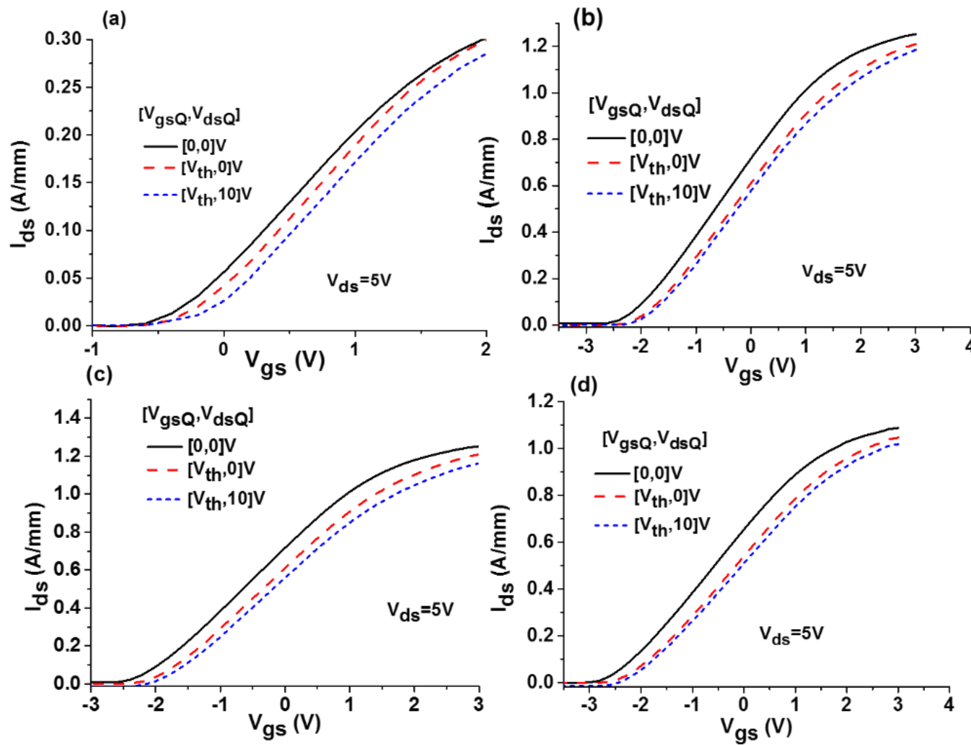


Fig. 4.22 Pulsed transfer I_{ds}-V_{gs} characteristics of HEMT devices for (a) 2.2 nm, (b) 3 nm (c) 3.7 nm and (d) 4.5 nm AlN top barrier thickness.

On the other hand, for t_b = 3.0, 3.7 and 4.5 nm, an increase of lag effects can be noticed during the transition from the linear (low V_{ds}) to the saturation region of the I_{ds}-V_{ds} characteristics. The minimum values (6-7% and 10-13% for Z_1 and Z_2, respectively) were obtained from the linear part of the I-V characteristics, which determines the R_{on} of the devices, while the maximum values (10-12% and 15-18% for Z_1 and Z_2 respectively) were observed in the onset of the saturation region.
Pulsed transfer characteristics (I_{ds}-V_{gs}) obtained at V_{ds} = 5 V are reported in Fig. 4.22 for the HEMT devices with AlN t_b = 2.2, 3.0, 3.7 and 4.5 nm, respectively. The threshold voltages (V_{th}) were determined from the V_{gs} intercept of the linear extrapolation of I_{ds} from the point of peak transconductance. In all cases, a small positive threshold voltage shift was observed for applied quiescent bias of [V_{th}, 0] V (gate lag). The V_{th} shift was 0.4 V for the devices with t_b = 3.0, 3.7 and 4.5 nm, while it became of approximately 0.2 V for t_b = 2.2 nm. Moreover, the currents did not exhibit any essential change under drain lag measurement conditions, when a high drain voltage

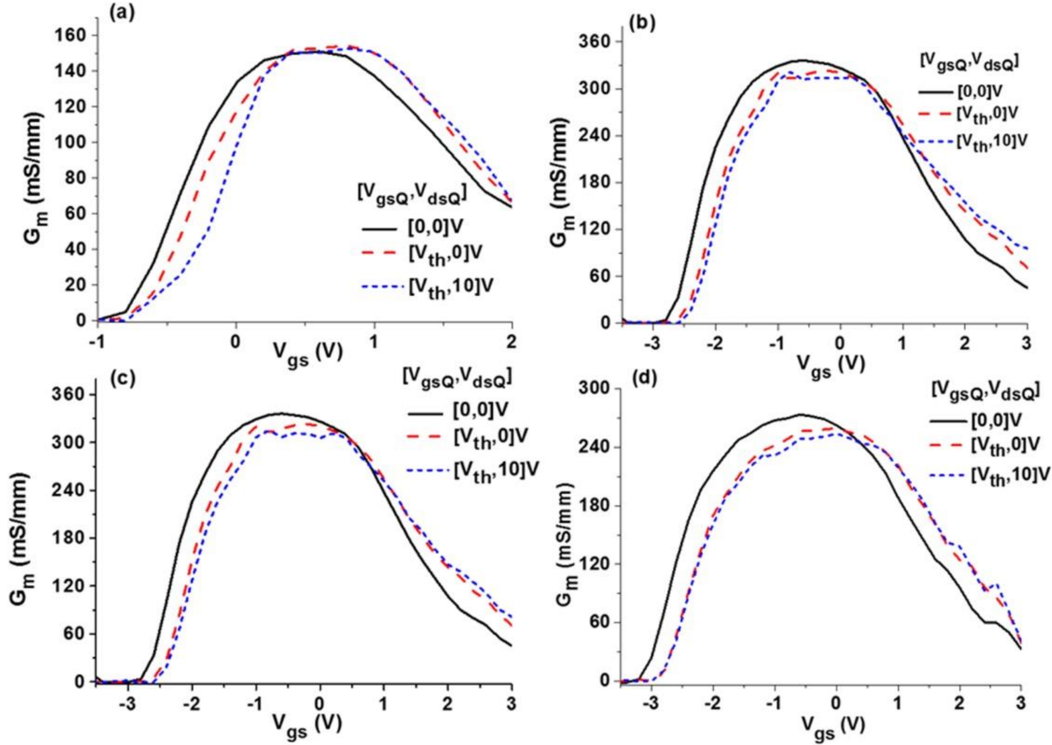


Fig. 4.23 Pulsed G_m-V_{gs} characteristics of HEMT devices for (a) 2.2 nm, (b) 3 nm (c) 3.7 nm and (d) 4.5 nm AlN top barrier thickness at V_{ds} = 5V.

---

was combined with the negative gate voltage V_{gs}=V_{th} in the quiescent bias point ([V_{gsQ}, V_{dsQ}] = [V_{th},10] V) (Fig. 4.22).

The transconductance, G_m, versus V_{gs} characteristics, extracted from the pulsed I_{ds}-V_{gs} measurements, are shown in Fig. 4.23. The maximum G_m is slightly affected by the quiescent bias point, with the highest reduction being ~8% for the device with 4.5 nm AlN barrier. The observed reduction of I_{dsmax} under gate or drain lag measurement conditions is due to the influence of traps with emission time constant higher than 500 ns. A conclusion about the location of traps in the devices may be inferred by the observed current variations [50,54,55]. In our experiments, the initial application of a negative V_{gs} voltage for off-state condition (V_{gsQ} = V_{th}) and zero V_{ds} voltage, i.e. quiescent bias point ([V_{gsQ}, V_{dsQ}] = [V_{th}, 0] V), induced a V_{th} shift without any significant decrease in the slope of the transfer curves and the maximum G_m. These results remained unaltered by the application of V_{dsQ} = 10 V with V_{gsQ} = V_{th}. Only the HEMT device with 2.2 nm AlN barrier exhibited a slight increase of V_{th} shift, without any change in the maximum G_m.

Meneghesso et al [50] has reported a comparative study of HEMT devices passivated, non-passivated and passivated but having defects under the gate, to determine the correlation of the gate lag and drain lag effects with the different locations of trapping levels in the device. According to that report [50], the trapping of electrons in trap levels at the surface between gate and drain becomes evident in the drain lag measurements, which are carried out with high V_{dsQ} (10 V was used) under closed channel conditions and results to reduction of G_m. If electron trapping occurs under the gate, then the drain lag measurements would not differ essentially from the gate-lag (V_{dsQ} = 0 V) measurements and result only to V_{th} shift, without reduction of G_m. The non-passivated surface of our HEMT devices does not allow to securely exclude any involvement of surface traps in the observed gate and drain lag effects. However, it should be noted that the observed negligible differences between gate lag and drain lag measurements, the negligible reduction of G_m and the noticeable V_{th} shift are consistent with dominant electron trapping under the gate and negligible effect of trapping in the gate-drain surface region.

The observation of V_{th} shift has been also associated [50] to sufficient gate leakage to charge the traps during the reverse quiescent bias pulse. The leakage of the gates in the current study was not negligible and could allow trapping of electrons in defects underneath the Schottky contact, in the AlN or GaN layers. However, the observed V_{th} shift in this work is very weak, especially for the most shallow 2DEG structure with t_b = 2.2 nm although an increased concentration of threading dislocations is expected in these thin heteroepitaxial structures, with a total thickness of ~0.5 μm, and this could result to a higher trap content in the layers. This indicates an unexpected low trapping effect in the layers underneath the gate, in spite of their small thickness above the highly lattice-mismatched AlN/sapphire interface. Medjdoub et al [16] have shown that the improved electron confinement that resulted from insertion of a 1.5 μm thick $Al_{0.08}Ga_{0.92}N$ layer underneath the GaN channel reduced significantly the current collapse of HEMT devices. The current work indicates that an AlN back barrier could have a very efficient effect even for the very thin heterostructures of ~0.5 μm total thickness. AlN is providing the maximum barrier to the overlaying GaN channel and, even more, can be grown by PAMBE with insulating characteristics without any doping, something not easy for GaN.

The absence of strong electron trapping at the non-passivated gate-drain surface region should also indicate that the GaN capped AlN/GaN/AlN heterostructure is a rather tolerant heterostructure

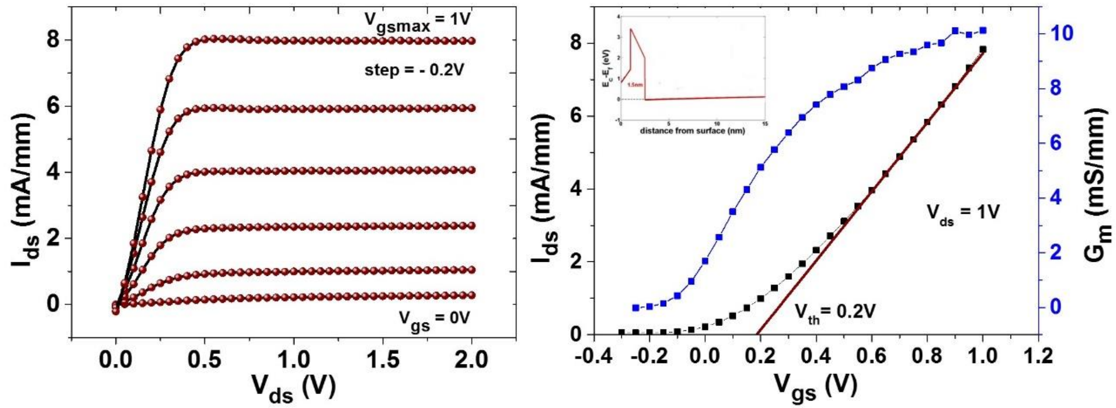


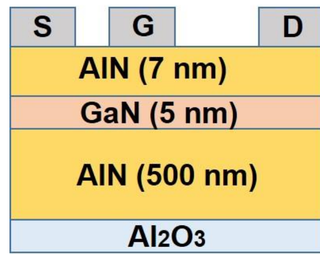
Fig. 4.24 (left) I_{ds}-V_{ds} curve and (right) transfer and G_m-V_{gs} characteristic, obtained at V_{ds}=1 V, for the structure 1.5 nm AlN/300 nm GaN/200 nm AlN/Al_2O_3 . Inset shows the equilibrium E_c band diagram.

---

design and material system. The 1 nm GaN cap protects the AlN surface from oxidation and stabilizes the charge at the surface which may improve the stability of the 2DEG. In addition, it is anticipated that a thin AlN barrier may facilitate the fast exchange of electronic charge between surface states and the 2DEG channel, as the bias conditions change [49].

4.8 Normally-off approach of AlN/GaN heterostructures

While significant improvement has been achieved toward developing normally-on devices, normally-off devices are also highly desirable for two key applications: power switching and digital logic circuits. As shown earlier, the threshold voltage shift can be accomplished by reducing the AlN top barrier thickness and therefore the 2DEG density. Figure 4.24 shows the I_{ds}-V_{ds} characteristic of a HEMT with a 1.5 nm ultrathin AlN barrier. As the E_c diagram shows in the inset, there is no 2DEG quantum well formation due to the charge depletion effect of the surface potential. The normally-off channel is turned on by positive V_{gs} and the device can operate up to +1 V before excessive gate leakage appears. A maximum I_{ds} current of 8 mA/mm and a peak G_m of 10 mS/mm was measured while V_{th} obtained from the transfer characteristic is about +0.2 V.



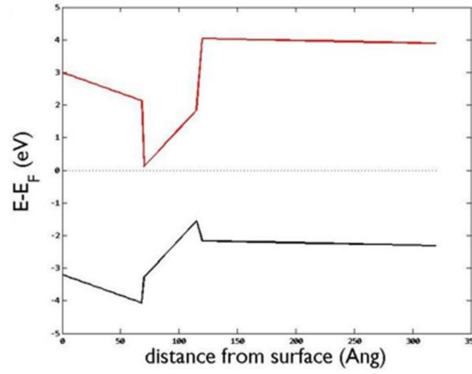


Fig. 4.25 The schematic cross section of the fabricated normally-off AlN/GaN/AlN transistor and the corresponding energy band diagram.

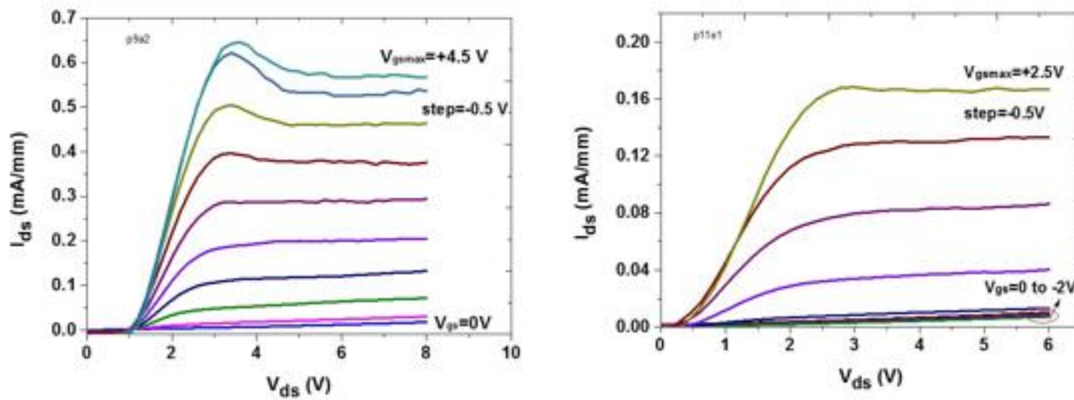


Fig. 4.26 DC I-V curves for L_g~1 µm transistors from the structure [7 nm AlN/5 nm GaN/500 nm AlN] grown on Al_2O_3 (0001) substrate. Maximum I_{ds} currents ranged between 0.16 and ~0.60 mA/mm for all the measured transistors.

Another approach to achieve normally-off operation could be the use of a heterostructure of GaN quantum well sandwiched between an AlN barrier and an AlN buffer (Fig. 4.25). The studied structure was 7 nm AlN/ 5 nm GaN/ 500 nm AlN buffer/ Al_2O_3 and the calculated equilibrium energy band diagram is shown in Fig. 4.25. As shown in the diagram, similarly to the previous structure, E_c falls above the Fermi level and there should be no 2DEG formation at the AlN/GaN

interface. The fabricated devices (with L_g~1 μm and W~50 μm) exhibited maximum I_{ds} currents ranging between 0.16-0.60 mA/mm (Fig. 4.26).

It should be noted that these structures are not suitable for high power applications because they suffer from very high on-resistances due to the absence of 2DEG across the entire source-drain region. However, this structure could be optimized by increasing the electron concentration under the ohmic metal contacts and the channel access regions by implanted dopants or patterning and selective growth of highly conductive material. The normally-off structures may also offer promise well beyond the established power-related applications and could be useful for ultra low-power or digital circuitry applications.

For high power operation, low-on resistance, high drive current and high extrinsic transconductance are needed. Therefore, to realize high-performance normally-off HEMTs, in addition to the mandatory normally-off channel under the gate which is controlled by the gate electrode, it is equally important the access regions (e.g. gate-source and gate-drain regions that are not controlled by the gate bias) to be highly conductive, i.e. in normally-on mode with high 2DEG density and resultant low access resistances. To overcome this problem, several approaches have been reported that start from an epitaxial structure with additional layers, which are modified selectively, with processes such as gate recess and F-treatment [57]. However, the concept of gate recess, which is the most common approach to obtain normally-off devices, is very difficult (or even impossible) to be accomplished successfully in ultrathin AlN/GaN HEMTs.

Simple oxygen plasma treatment in structures comprising of 4 nm AlN/GaN HEMTs was tested for gate-recessing, expecting that a part of the AlN layer is converted into Al oxide layer during this treatment. It was found that this process is difficult to control and causes serious plasma-induced damage. Moreover, the optimization of the plasma recipe is not easy for such a thin AlN barrier and the etch details of the plasma or the true depth of the etch cannot be determined accurately. For example, for plasma treatment time <30 sec, characteristic values obtained from Hall measurements before O_2 plasma treatment were: R_{sh}=264 Ohm, μ=680 cm^2/Vs, Ns=3.47 x 10^{13} cm^{-2}. After O_2 treatment the obtained values were: R_{sh}=3.87 x 10^3 Ohm, μ=185 cm^2/Vs, Ns=8.70 x 10^{12} cm^{-2}.

4.9 AlN/GaN/AlN HEMTs with in-situ deposited SiN_x

Control of surface states on III–N materials is a well-known difficult issue. Several insulators have been used as passivation layers to solve this problem. However, the most widely utilized one is silicon nitride (SiN_x). SiN_x passivation was first introduced in the early 1990s to overcome trapping effects in GaAs FETs [58]. In 2000, Green et al. from Cornell University were the first who demonstrated SiN_x/AlGaN/GaN HEMTs with improved pulsed I-V characteristics and microwave power performance [59]. Generally, it is assumed that the SiN_x deposition prevents surface trapping and the formation of the virtual gate on the device surface in the gate drain access region (preventing the injection of electrons from the gate) [52,59]. However, undesirable side-effects of SiN_x deposition, such as increased gate leakage may still remain depending on the deposition method and the experimental conditions [60-65]. The deposition of SiN_x inside a metalorganic chemical vapor deposition (MOCVD) reactor, which is used for III-Nitride growth, has been demonstrated as an efficient method for passivating the surface of HEMT devices [66-70]. This kind of passivation is thought to be an effective way to avoid problems related with surface exposure to atmosphere and native oxide formation. Recently, it has been showed that the in situ SiN_x dielectric grown by MOCVD has great potential also for the ultrathin barrier AlN/GaN HEMT heterostructures [67-69]. However, the in situ SiN_x deposition on AlN/GaN HEMT structures, at the end of their growth in a PAMBE reactor, has not been explored yet. PAMBE is a suitable growth technique for III-Nitride HEMTs with ultrathin layers and may also provide hydrogen-free SiN_x layers [71].

A thin AlN/GaN/AlN HEMT heterostructure with 5 nm SiN_x cap layer was grown entirely inside the MBE growth chamber and its material and device properties were compared to a similar structure without the SiN_x cap layer. The 5 nm thick SiN_x layer was grown in situ on top of the GaN cap, with a deposition rate of 0.1 nm/min at a substrate temperature of 250 ^{o}C, under nitrogen-rich conditions, using a silicon sublimation source and the N_2 plasma source. HEMT devices were fabricated by Ni/Au metallization for formation of MIS or Schottky barrier gates on the structures with or without the SiN_x cap, respectively (Fig. 4.27). BCl_3/Cl_2 plasma etching was used for mesa isolation. The Ohmic contacts were formed by Ti/Al/Ni/Au metallization and were annealed at 750 ^{o}C. Before the MIS-HEMT source and drain contact metallization, the SiN_x insulator had been

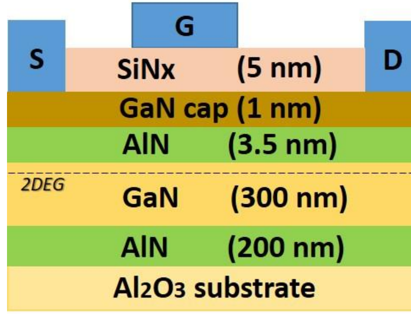


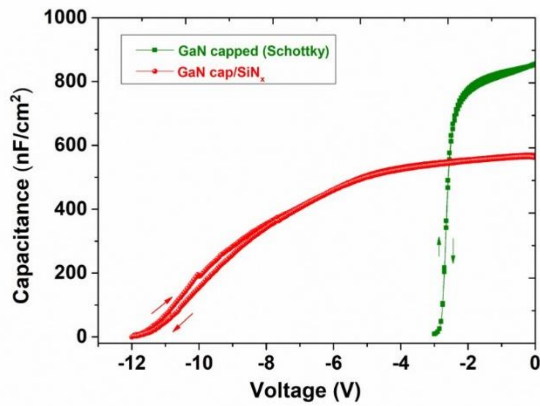
Fig. 4.27 Cross section of the MIS-gate HEMT devices processed from the heterostructure with in situ SiN_x cap layer. A similar heterostructure without the SiN_x layer was used for processing of Schottky-gate HEMTs.

---

removed selectively by SF_6 plasma etch. Discrete MIS capacitor (MISCAP) devices of Ni/SiN_x/GaN/AlN/GaN were also processed, with circular diameter d=100 μm.

C–V characteristics for the SiN_x MIS and Schottky barrier contacts measured at 1 MHz sweeping from negative to positive bias direction are plotted in Fig. 4.28. The plateau (total) capacitance C_{tot} in the MISCAP devices is a series connection of the AlN barrier capacitance C_{AlN} and the SiN_x dielectric capacitance C_{SiNx}, given by $C_{tot} = C_{SiNx} C_{AlN} / C_{SiNx} + C_{AlN}$. The SiN_x thickness may be estimated by using the above equation, where C_{AlN}=836 nF/cm^2 is the zero bias capacitance of the unpassivated HEMT and C_{tot}=580 nF/cm^2 is the zero bias capacitance of the MIS-HEMT. Thus, the SiN_x capacitance can be calculated by using $C_{SiNx}=C_{tot}C_{AlN}/C_{tot} - C_{AlN}$. This results in C_{SiNx}= 1980 nF/cm^2; by talking into account that $C_{SiNx}=\varepsilon_0 * \varepsilon_{SiNx}/d_{SiNx}$, where ε_0=8.85 x 10^{-12} F/m is the vacuum perimitivity and ε_{SiNx}= 7.5 is the dielectric constant of amorphous Si_3N_4, the estimated SiN_x thickness is 3.5 nm. This value is less than the 5 nm SiN_x nominal thickness, possibly due to the uncertainty in the MBE SiN_x dielectric constant.

It can be also observed that the depletion portion of the MISCAP device is stretched out in the voltage direction due to the existence of interface trap states (say at the SiN_x/GaN interface) that can (dis)charge based on Fermi level position and proximity to a mobile charge supply (e.g. the 2DEG channel) [36,72]; these trap states can follow the slowly varying dc bias causing the distortion of the C–V curve [72] (see chapter 3, par. 3.2.3.2). On the other hand, high quality C-V curve is observed in the case of Schottky barrier device, as evidenced by the steep slope in the depletion region.



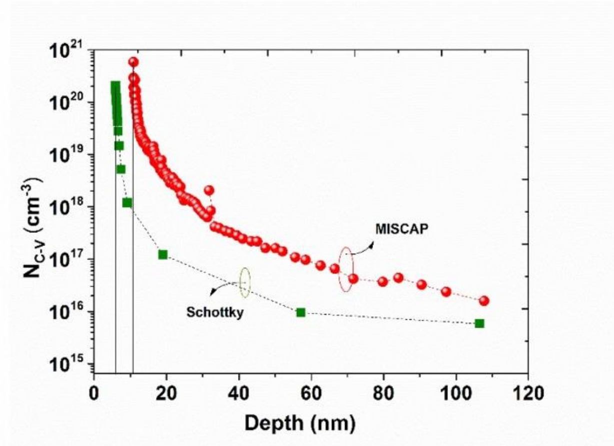


Fig. 4.28 (left) C-V curves and (right) the apparent carrier concentration profiles from a Schottky diode of the unpassivated AlN/GaN HEMT and a MISCAP device of the SiN_x passivated AlN/GaN/AlN HEMT devices measured at 1 MHz. The diameter of the Schottky and MIS contact dot was 100 μm.

Figure 4.28 exhibits also the apparent carrier concentration profiles, as obtained from C-V measurements on the MISCAP device and the Schottky diode, using $N_{cv}=(C^3/q\varepsilon_s)(dC/dV)^{-1}$. In both cases, a high carrier concentration can be observed close to the AlN/GaN interface, confirming the high polarization discontinuity between the 3.5 nm AlN and the GaN buffer. The electron densities calculated by integrating the carrier profile were ~1.6 x 10^{13} for the Schottky diode and ~4.0 x 10^{13} cm^{-2} for the MISCAP device, which are in close agreement with N_s obtained from Hall-effect data (1.9 x 10^{13} and 3.8 x 10^{13} cm^{-2}, respectively). The increased N_s value for the sample with in-situ SiN_x cap is consistent with previous studies [73-76]. It suggests the presence of an additional positive charge at the SiN_x/GaN interface, which could be attributed to some kind of interface states. It has been speculated that Si atoms at the SiN_x/GaN interface might act as donor dopants [76]. The positive sheet charge at the SiN_x/GaN cap interface neutralizes negative polarization charges of the GaN cap surface, increasing the 2DEG density at the AlN/GaN heterojunction. Though the exact origin of the charges at the interface has not been clarified yet, this is essentially identical to modulation doping and has been reported similarly to occur for other insulators like Al_2O_3 [77]. The observed increase of N_s may be related with the change of the energy level of the GaN surface donor with the SiN_x deposition (surface barrier height) [1,64,76].

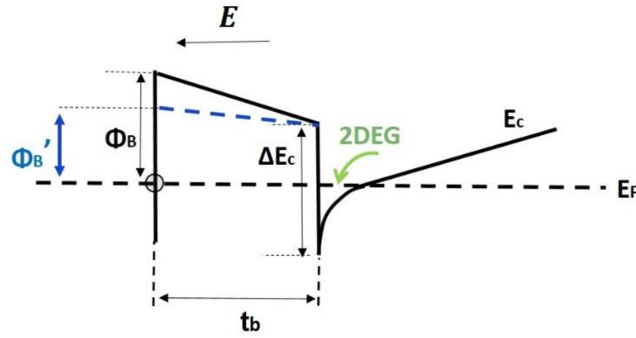


Fig. 4.29 Schematic diagram showing the possible effect of SiN_x deposition on the surface pinning level (ref. 1) for an AlN/GaN heterostructure.

A 2DEG density increase should correspond to a decreased electric field in the barrier, which implies that the surface pinning level is now smaller (Fig. 4.29) [1].

To our knowledge, such an extremely high N_s increase with SiN_x deposition has not been reported and there are no literature data for the ultrathin AlN barrier (compared to AlGaN) HEMT structures. Higashiwaki et al. [74] studied SiN/AlGaN/GaN HFETs with thin and high Al composition barrier layers and suggested that for thin barrier devices the effect of the electric field from the surface states, which are considered as fixed negative charges, is stronger than for thick ones due to the shorter distance between the surface and the channel interface [74]. Similarly, the high N_s increase in our AlN/GaN structures is related with the use of the 3.5 nm thin AlN barrier and the proximity of the heterointerface to the negatively charged surface.

Figure 4.30(a) shows the dc I_{ds}-V_{ds} characteristics of the SiN_x MIS-gate AlN/GaN/AlN HEMT with L_g~1 μm. The device shows an I_{ds} current of 1.15 A/mm at V_{ds} = 6 V and V_{gs} = 0 V. In the same figure, the I_{ds}-V_{ds} curve of the Schottky-gate HEMT exhibits I_{ds} = 0.43 A/mm, at V_{gs} = 0 V. The significantly higher current of the MIS-HEMT is consistent with the large increase in N_s observed by Hall and C-V measurements. A further I_{ds} increase at forward V_{gs} bias could not be achieved for the MIS-gate AlN/GaN/AlN HEMT, probably due to the presence of high interface state densities, as evidenced from the C-V stretch-out of the MISCAP device (Fig. 4.28). It is speculated that the high density of the interface states at the SiN_x/GaN interface is responsible for innefficient Fermi level response and quasi-pinning under the gate when $V_{gs} > 0$.

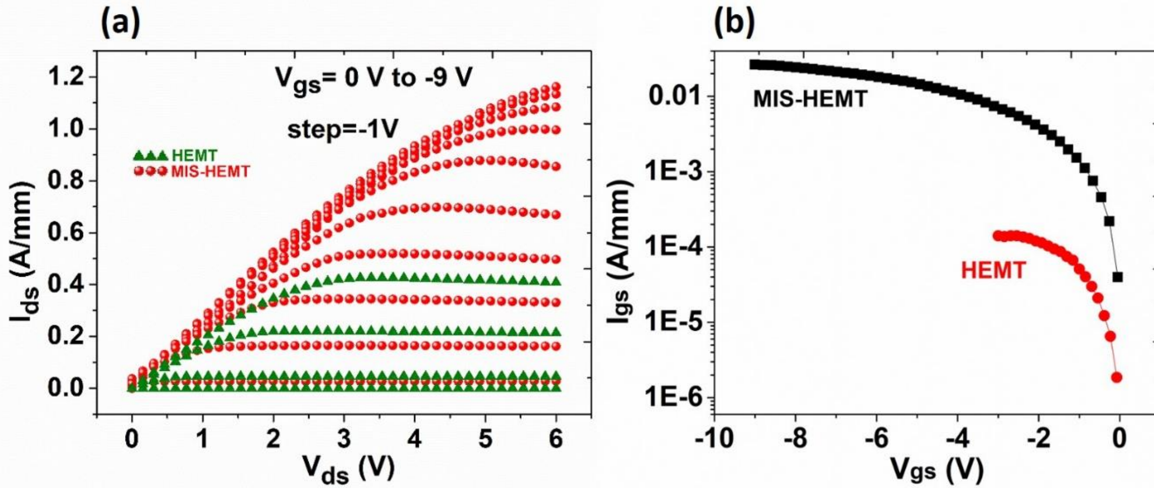


Fig. 4.30 (a) DC output I_{ds}-V_{ds} characteristics and (b) two-terminal gate leakage curves for a MIS-gate HEMT, fabricated by the PAMBE grown SiN_x/AlN/GaN/AlN heterostructure, and for a Schottky-gate HEMT of a similar structure without SiN_x. Device dimensions: L_g=1 μm, W=50 μm.

V_{gs} cannot modulate N_s sufficiently and consequently I_{ds} no longer increases. This "choked channel" mechanism has been also reported for HfO_2/AlN/GaN HEMTs by Deen [36]. Moreover, the MIS-HEMT exhibited a high leakage current originating from the gate. I_{gs} was ~2 orders of magnitude higher for the MIS-HEMT when compared with the Schottky-gate HEMT (Fig. 4.30(b)). The increase of leakage after SiN_x deposition in a HEMT device has been observed by many authors [60-65], and is closely related with the different passivation processes and the surface preparation method [61]. Z. H. Lu et al. [64] showed that PECVD deposited SiN on AlGaN/GaN HEMTs may increase the gate leakage current up to five orders compared to a device without passivation [64]. It has been proposed that electron hopping conduction through trap states along the SiN_x surface or the SiN_x/GaN interface could be involved and contribute to the gate leakage problem [60-63,64,65].

Pulsed gate and drain lag results of the MIS-gate AlN/GaN HEMTs showed that such a thin SiN_x layer does not passivate the nitride surface from the standpoint of current collapse, resulting in a >70% reduction of I_{ds} in the majority of devices, while the lowest measured slump ratio for drain lag condition was ~45 % (Fig. 4.31). Thus, an increase in 2DEG density as a result of a deposited

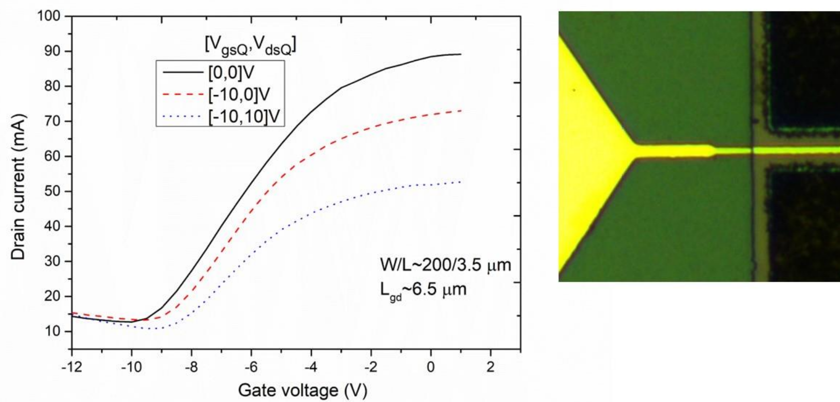


Fig. 4.31 Pulsed I_{ds}-V_{gs} measurements under gate and drain lag conditions for a SiN_x MIS-gate HEMT device with L_g~3.5 µm, and optical image of a fabricated transistor.

---

dielectric is not indicative of a passivated surface because a succesful HEMT surface passivation requires the minimization of the deviation of the dynamic I-V characteristics of a transistor from the dc I-V characteristics [36]. If the SiN_x/GaN interface or the bulk of the SiN_x contains charge trapping sites, then electrons leaking from the gate metal under a high electric field can get trapped. This trapped negative charge can result in a negatively charged virtual gate to develop in a similar way to that on an unpassivated surface [52]. Moreover, the high current collapse is correlated with the observed high gate leakage. The SiN_x capping increased the leakage current, which means that the number of carriers delivered from the gate to traps located at the SiN_x/GaN interface and/or the SiN_x bulk was increased, in comparison to traps on an uncapped GaN surface. A higher gate leakage will increase the charging of the trap states at the GaN surface during the reverse-bias pulse. [50,78].

The above results suggest the need for a systematic investigation of the structural and electronic properties of the MBE deposited SiN_x insulator and the SiN_x/GaN interface in order to optimize the SiN_x/GaN deposition and interface.

As a first step towards understanding and optimizing the SiN_x/GaN structures, three SiN_x/GaN samples were realized by depositing 10 nm thick SiN_x layer on top of 1 µm GaN buffer at three different substrate temperatures: 250° C, 500° C and 700 ^{o}C. A Ti/Al/Ni/Au multilayer structure

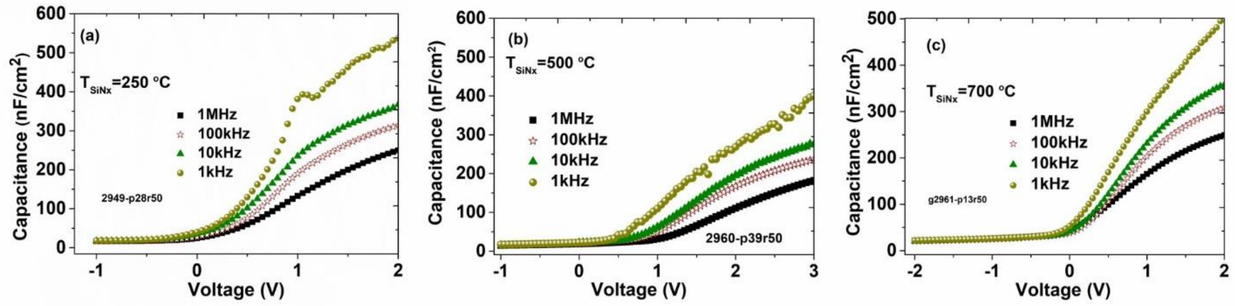


Fig. 4.32 Frequency dependence of the C-V characteristics for Ni/SiN_x/GaN MISCAPs where SiN_x dielectric was deposited at (a-b) 250 °C, (c-d) 500 °C and (e-f) 700 °C.

---

was deposited on the GaN for ohmic contact formation after selective SiN_x etching by SF_6, followed by annealing at 750 °C. A circular Ni/Au metallization with a diameter of 100 μm was deposited on the SiN_x surface to form an MIS contact. High non-uniformities were observed among the 40 MISCAPs studied from each sample. An investigation of C-V characteristics is needed to understand the MIS structures [79-81].

Figure 4.32 shows the frequency dependence (1, 10, 100 kHz and 1 MHz) of the C-V characteristics of the MISCAP devices. A large frequency dispersion and an increase of capacitance with decreasing frequency, from 1 MHz to 1 KHz, is observed for all the MISCAPs reflecting a poor SiN_x/GaN interface quality. This is related with a larger interface state capacitance contribution at lower frequencies (theory explained analytically in chapter 3, par. 3.2.3.2), and is a strong indication of high interface trap densities. Similar behavior has been reported by Gaffey et al. [81] for nonoptimized MIS capacitors using $SiO_2/Si_3N_4/SiO_2$ insulators deposited on GaN by jet vapor deposition, and by Hori et al. [82] for atomic layer deposited Al_2O_3 on AlGaN/GaN structures grown by MOCVD.

By studying the flat band voltage ($V_{FB} = \Phi_{MS} - Q_{f,eff} / C_{SiNx}$) as described in chapter 2, the effective dielectric-fixed charge densities, $Q_{f,eff}$, of the MISCAPs were also calculated (Table I). V_{FB} was determined from the $1/C^2$ versus V plot, measured at f=1MHz, as shown in Fig. 4.33. The donor concentration N_d in GaN was also obtained from data fitting to the partial range of the C-V characteristics in which $1/C^2$-V is linear ($1/C^2 \propto -2V/q\varepsilon_s N_d$).

SiN_x growth T (°C)	N_d (cm^{-3})	Φ_{MS} (V)	V_{FB} (V)	$Q_{f,eff}$ (x 10^{12} cm^{-2})
250	3.2 x 10^{15}	+1.63	+0.19	+2.8
500	7.6 x 10^{15}	+1.66	+0.35	+1.7
700	1.2 x 10^{16}	+1.67	-0.20	+3.4

Table I. Summary of parameters extracted for the SIN_x/GaN MISCAPs, as described in chapter 2. The doping concentration N_d was obtained from the slopes of the $1/C^2$ – V curves. Φ_{MS} calculated from Eq. (2.33) by using X_{GaN} = 3.3 eV.

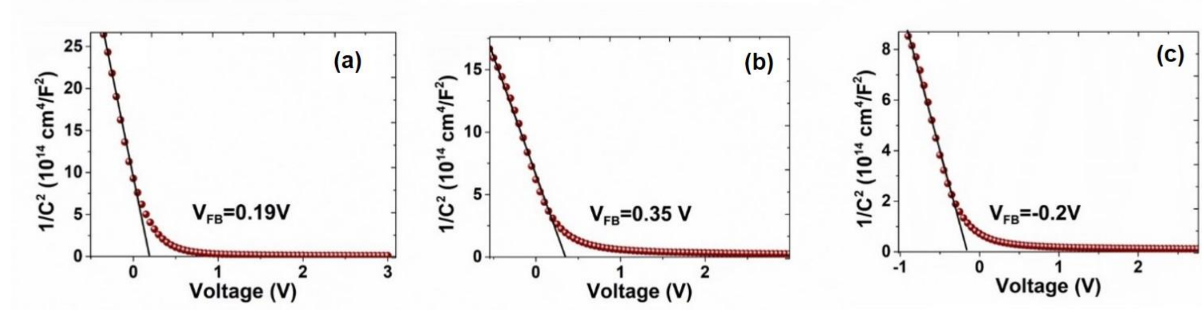


Fig. 4.33 Plot of $1/C^2$ versus V data for the SIN_x/GaN MISCAPs. The SiN_x dielectric was deposited at (a) 250, (b) 500 and (c) 700 °C.

The C-V results are correlated with the leakage of devices. Figure 4.34 exhibits the I-V curves for the MISCAP devices. All the MISCAPs exhibited similar leakage behavior where Schottky-like characteristics observed rather than MIS-like behavior. Although in the reverse bias direction the MISCAPs can sustain a low current of ~10^{-5} A/cm^2 at -5 V, in the forward direction where electrons are injected from the GaN into the SiN_x, a steep increase, without any current barrier, is observed. A small ΔE_c between SiN_x and GaN may also have a significant contribution to a leaky behavior for device operation under forward bias [83-85]. Robertson and Falabretti predicted by calculations ΔE_c to be generally low (1.2 eV) [86], when compared with other common insulators like Al_2O_3 or SiO_2 (Fig. 4.35). Experimentally, ΔE_c was determined to be lower (0.5 eV) than the theoretical value, for Si_3N_4 films deposited onto GaN by CVD deposition [87,88].

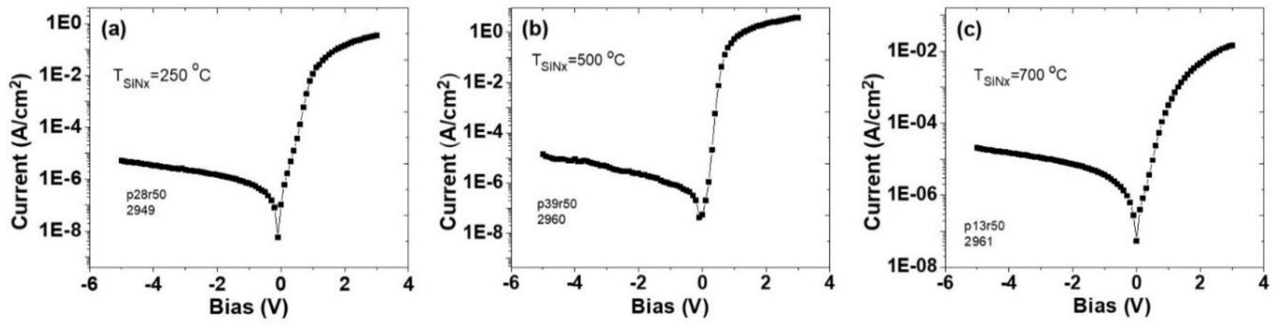


Fig. 4.34 I-V curves of Ni/SiN_x/GaN MISCAP devices for SiN_x deposition temperature of (a) 250 °C, (b) 500 °C and (c) 700 °C.

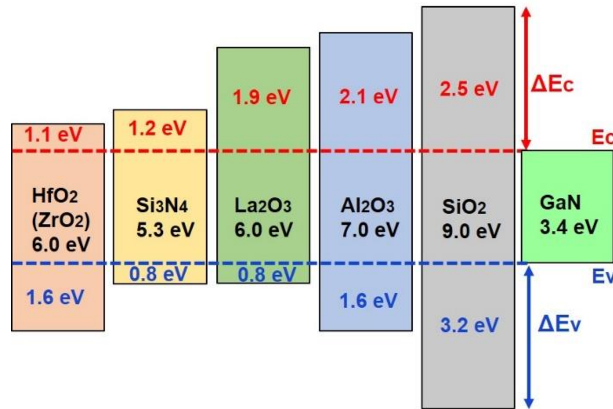


Fig. 4.35 Band alignements at insulators/GaN interfaces calculated by Robertson and Falabretti [89].

Thus, SiN_x may not be the best choice material to be adopted as a gate dielectric in ultrathin HEMT structures, because its bandgap (~5 eV) is not large enough to form a sufficient barrier with GaN, which in turn leads to high leakage currents [83]. Therefore, only limited work has been reported using in situ SiN_x by MOCVD [67] or SiN_x deposited by PECVD [87] on an AlN/GaN structure with successful suppression of gate leakage current. The MBE SiN_x dielectric studied in this work remains a subject of further study and more investigation is needed to understand and achieve the successful passivation of AlN/GaN HEMTs and possibly the formation of high quality MIS gate contacts.

4.8 Conclusions

AlN/GaN HEMT structures with thin GaN/AlN buffer layer have been extensively studied and the effects of the back AlN barrier on 2DEG properties have been evaluated. HEMT structures consisting of 300 nm GaN/ 200 nm AlN buffer layer on sapphire were grown by PAMBE and exhibited a remarkable agreement with the theoretical calculations. The results suggest that the double GaN capped AlN/GaN/AlN heterostructures may offer intrinsic advantages for the breakdown and current stability characteristics of high current HEMTs. When an in situ MBE SiN_x cap was introduced in a double AlN/GaN/AlN structure, the electron density was increased significantly causing an increase in HEMT device I_{ds} current. However, the MBE SiN_x was not suitable as a passivation layer and gate dielectric for the AlN/GaN HEMTs due to high gate leakage and significant current collapse. An approach towards the realization of normally-off transistors with very low I_{ds} currents was also presented based on a very thin (1.5 nm) AlN barrier and by using a double heterostructure with a 5 nm GaN quantum well sandwiched between a 7 nm AlN barrier and an AlN buffer.

4.9 Chapter 4 references

[1] R. Vetury. Polarization induced 2DEG in AlGaN/GaN HEMTs: On the origin, DC and transient characterization. Ph.D. dissertation, University of California, Santa Barbara, 2000.

[2] S. Kato, Y. Satoh, H. Sasaki, I. Masayuki and S. Yoshida S. C-doped GaN buffer layers with high breakdown voltages for high-power operation AlGaN/GaN HFETs on 4-in Si substrates by MOVPE. J. Cryst. Growth 298, 831, 2007.

[3] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Würfl and G. Tränkle. AlGaN/GaN/GaN:C Back-barrier HFETs with breakdown voltage of over 1 kV and low $R_{ON}\times A$. 2010 IEEE Trans. Electron Devices 57, 3050, 2010.

[4] S. Heikman, S. Keller, S. P. DenBaars and U. K. Mishra. Growth of Fe doped semi-insulating GaN by metalorganic chemical vapor deposition. Appl. Phys. Lett. 81, 439, 2002.

[5] H. S. Kang, C. H. Won, Y. J. Kim, D.S. Kim, Y. J. Yoon, I. M. Kang, Y. S. Lee and J. H. Lee. Suppression of current collapse in AlGaN/GaN MISHFET with carbon- doped GaN/undoped GaN multi-layered buffer structure. Phys. Status Solidi A 212, 1116, 2015.

[6] Z. Y. Fan, J. Li, M. L. Nakarmi, J. Y. Lin, and H. X. Jiang. AlGaN/GaN/AlN quantum-well field-effect transistors with highly resistive AlN epilayers. Appl. Phys. Lett. 88, 073513, 2006.

[7] C. Q. Chen, J. P. Zhang, V. Adivarahan, A. Koudymov, H. Fatima, G. Simin, J. Yang, and M. Asif Khan. AlGaN/GaN/AlGaN double heterostructure for high-power III-N field-effect transistors. Appl. Phys. Lett. 82, 4593, 2003.

[8] F. Medjdoub, M. Zegaoui, B. Grimbert, N. Rolland and P.-A. Rolland. Effects of AlGaN Back Barrier on AlN/GaN-on-Silicon High-Electron-Mobility Transistors. Appl. Phys. Express 4 124101, 2011.

[9] X. Kong, K. Wei, G. Liu, X. Liu, C. Wang, and X. Wang. Improved performance of highly scaled AlGaN/GaN high-electron-mobility transistors using an AlN back barrier. Applied Physics Express 6, 051201, 2013.

[10] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl and G. Tränkle. Punchthrough-voltage enhancement of AlGaN/GaN HEMTs using AlGaN double-heterojunction confinement. IEEE Trans. Electron Devices 55, 3354, 2008.

[11] A. L. Corrion, K. Shinohara, D. Regan, I. Milosavljevic, P. Hashimoto, P. J. Willadsen, A. Schmitz, S. J. Kim, C. M. Butler, D. Brown, S. D. Burnham, and M. Micovic. High-speed AlN/GaN MOS-HFETs with scaled ALD Al_2O_3 gate insulators. IEEE Electron Device Lett. 32, 1062, 2011.

[12] G. Li, R. Wang, J. Guo, J. Verma, Z. Hu, Y. Yue, F. Faria, Y. Cao, M. Kelly, T. Kosel, H. Xing, and D. Jena. Ultrathin body GaN-on-insulator quantum well FETs with regrown ohmic contacts. IEEE Electron Device Lett. 35, 661, 2012.

[13] X. Hu, J. Deng, N. Pala, R. Gaska, M. S. Shur, C. Q. Chen, J. Yang, G. Simin, M. A. Khan, J. C. Rojo and L. J. Schowalter. AlGaN/GaN heterostructure field-effect transistors on single-crystal bulk AlN. Appl. Phys. Lett. 82, 1299, 2003.

[14] G. Meneghesso, A. Zazandrea, A. Stocco, I. Rossetto, C. De Santi, F. Rampazzo, M. Meneghini and E. Zanoni. GaN-HEMTs devices with single- and double- heterostructure for power switching applications. in Proc. IEEE Int. Rel. Phys. Symp. (IRPS), Apr. 2013, pp. 3C.1.1–3C.1.7.

[15] H. Hahn, C. Funck, S. Geipel, H. Kalisch, and A. Vescan. The III-nitride double heterostructure revisited: Benefits for threshold voltage engineering of MIS devices. IEEE Trans. Electron Devices 63, 606, 2016.

[16] F. Medjdoub, D Ducatteau, M. Zegaoui, B. Grimbert, N. Rolland, and P.A. Rolland. Trapping effects dependence on electron confinement in ultrashort GaN-on-Si high-electron-mobility transistors. Appl. Phys. Express 5, 034103, 2012.

[17] G. Li, B. Song, S. Ganguly, M. Zhu, R. Wang, X. Yan, J. Verma, V. Protasenko, H. G. Xing, and D. Jena. Two-dimensional electron gases in strained quantum wells for AlN/GaN/AlN double heterostructure field-effect transistors on AlN. Appl. Phys. Lett. 104, 193506, 2014.

[18] A. Bairamis, Ch. Zervos, A. Adikimenakis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis & A. Georgakilas. Electron density and currents of AlN/GaN high electron mobility transistors with thin GaN/AlN buffer layer. Appl. Phys. Lett. 105, 113508, 2014.

[19] A. Hinoki, S. Kamiya, T. Tsuchiya, T. Yamada, J. Kikawa, T. Araki, A. Suzuki, and Y. Nanishi. Correlation between the leakage current and the thickness of GaN-layer of AlGaN/GaN-HFET. Phys. stat. sol. (c) 4, 2728, 2007.

[20] H. M. Ng, D. Doppalapudi, T. D. Moustakas, N. G. Weimann and L. F. Eastman. The role of dislocation scattering in n-type GaN films. Appl. Phys. Lett. 73, 821, 1998.

[21] Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, P. Kozodoy, S. P. Denbaars, and U. K. Mishra. Very high breakdown voltage and large transconductance realized on GaN heterojunction field effect transistors. Appl. Phys. Lett. 69, 1438, 1996.

[22] P. Herfurth, Y. Men, R. Rosch, J. F. Carlin, N. Grandjean, and E. Kohn. GaN on sapphire mesa technology. Phys. Status Solidi C 9, 945, 2012.

[23] P. Herfurth, D. Maier, L. Lugani, J. F. Carlin, R. Rosch, Y. Men, N. Grandjean, and E. Kohn. Ultrathin body InAlN/GaN HEMTs for high-temperature (600° C) electronics. IEEE Electron Device Lett. 34, 496, 2013.

[24] L. Lugani, J. F. Carlin, M. A. Py, D. Martin, F. Rossi, G. Salviati, P. Herfurth, E. Kohn, J. Blasing, A. Krost, and N. Grandjean. Ultrathin InAlN/GaN heterostructures on sapphire for high on/off current ratio high electron mobility transistors. J. Appl. Phys. 113, 214503, 2013.

[25] A. Georgakilas, S. Mikroulis, V. Cimalla, M. Zervos, A. Kostopoulos, Ph. Komninou, Th. Kehagias, and Th. Karakostas. Effects of the sapphire nitridation on the polarity and structural properties of GaN layers grown by plasma-assisted MBE. Phys. Status Solidi A 188, 567, 2001.

[26] S. Mikroulis, A. Georgakilas, A. Kostopoulos, V. Cimalla, E. Dimakis, and Ph. Komninou. Control of the polarity of molecular-beam-epitaxy-grown GaN thin films by the surface nitridation of Al_2O_3 (0001) substrates. Appl. Phys. Lett. 80, 2886, 2002.

[27] E. Bellet-Amalric, C. Adelmann, E. Sarigiannidou, J. L. Rouviere, G. Feuillet, E. Monroy, and B. Daudin. Plastic strain relaxation of nitride heterostructures. J. Appl. Phys. 95, 1127, 2004.

[28] I.-H. Tan, G. L. Snider, L. D. Chang, and E. L. Hu. A self-consistent solution of Schrödinger–Poisson equations using a nonuniform mesh. J. Appl. Phys. 68, 4071, 1990.

[29] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman. Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures. J. Phys.: Condens. Matter 14, 3399, 2002.

[30] C. G. Van de Walle and J. Neugebauer. Universal alignment of hydrogen levels in semiconductors, insulators and solutions. Nature 423, 626, 2003.

[31] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra. Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures. J. Appl. Phys. 93, 10114, 2003.

[32] Y. Cao and D. Jena. High-mobility window for two-dimensional electron gases at ultrathin AlN/GaN heterojunctions. Appl. Phys. Lett. 90, 182112, 2007.

[33] Y. Cao. Study of AlN/GaN HEMTs: MBE Growth, Transport Properties, and Device Issues. Ph.D. Dissertation, University of Notre Dame, 2010.

[34] Yu Cao, H. Xing, and D. Jena. Polarization-mediated remote surface roughness scattering in ultrathin barrier GaN high-electron mobility transistors. Appl. Phys. Lett. 97, 222116, 2010.

[35] D. A. Deen, D.F. Storm, D.S. Katzer, D.J. Meyer, S.C. Binari. Dependence of ohmic contact resistance on barrier thickness of AlN/GaN HEMT structures. Solid-State Electron. 54, 613, 2010.

[36] D. A. Deen. Advanced design of ultra-thin barrier AlN/GaN HEMTs; A study of device design, modeling, and analysis. Ph.D. Dissertation, University of Notre Dame, 2011.

[37] A. Adikimenakis, K. E. Aretouli, E. Iliopoulos, A. Kostopoulos, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas, High electron mobility transistors based on the AlN/GaN heterojunction. Microelectron. Eng. 86, 1071, 2009.

[38] K. D. Chabak, D. E. Walker, M. R. Johnson, A. Crespo, A. M. Dabiran, D. J. Smith, A. M. Wowchak, S. K. Tetlak, M. Kossler, J. K. Gillespie, R. C. Fitch, and M. Trejo. High-performance AlN/GaN HEMTs on sapphire substrate with an oxidized gate insulator. IEEE Electron Device Lett. 32, 1677, 2011.

[39] D. J. Meyer, D. A. Deen, D. F. Storm, M. G. Ancona, D. S. Katzer, R. Bass, J. A. Roussos, B. P. Downey, S. C. Binari, T. Gouges, T. Paskova, E. A. Preble, and K. R. Evans. High electron velocity submicrometer AlN/GaN MOS-HEMTs on freestanding GaN substrates. IEEE Electron Device Lett. 34, 199, 2013.

[40] L. Corrion, K. Shinohara, D. Regan, I. Milosavljevic, P. Hashimoto, P. J. Willadsen, A. Schmitz, D. C. Wheeler, C. M. Butler, D. Brown, S. D. Burnham, and M. Micovic. Enhancement-mode AlN/GaN/AlGaN DHFET with 700-mS/mm g_m and 112-GHz f_t. IEEE Electron Device Lett. 31, 1116, 2010.

[41] S. Taking, D. MacFarlane and E. Wasige. AlN/GaN MOS-HEMTs with thermally grown Al_2O_3 passivation. IEEE Trans. Electron Devices 58, 1418, 2011.

[42] G. Guodong, D. Shaobo, L. Yuanjie, H. Tingting, X. Peng, Y. Jiayun, F. Zhihong. Low ohmic contact AlN/GaN HEMTs grown by MOCVD. Journal of Semiconductors 34, 114004, 2013.

[43] D. A. Deen, D. F. Storm, R. Bass, D. J. Meyer, D. S. Katzer, S. C. Binari, J. W. Lacis, and T. Gougousi. Atomic layer deposited Ta_2O_5 gate insulation for enhancing breakdown voltage of AlN/GaN high electron mobility transistors, Appl. Phys. Lett. 98, 023506, 2011.

[44] S. R. Bahl and J. A. del Alamo. A new drain-current injection technique for the measurement of off-state breakdown voltage in FETs. IEEE Trans. Electron Devices 40, 1558, 1993.

[45] R. Menozzi. Off-state breakdown of GaAs PHEMTs: Review and new data. IEEE Trans. Electron Devices 4, 54, 2004.

[46] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta and N. DasGupta. Gate leakage mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and modeling. 2013 IEEE Trans. Electron Devices 60, 3157, 2013.

[47] G. Meneghesso, M. Meneghini and E. Zanoni. Breakdown mechanisms in AlGaN/GaN HEMTs: An overview. Jpn. J. Appl. Phys. 53, 100211, 2014.

[48] D. Marcon, G. Meneghesso, T.-L. Wu, S. Stoffels, M. Meneghini, E. Zanoni and S. Decoutere. Reliability analysis of permanent degradations on AlGaN/GaN HEMTs. IEEE Trans. Electron Devices 60, 3132, 2013.

[49] Ch. Zervos, A. Adikimenakis, A. Bairamis, A. Kostopoulos, M. Kayambaki, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas. Analysis of current instabilities of thin AlN/GaN/AlN double heterostructure high electron mobility transistors. Semicond. Sci. Technol. 31, 065002, 2016.

[50] G. Meneghesso, M. Meneghini, D. Bisi, I. Possetto, A. Cester, U K Mishra and E. Zanoni. Trapping phenomena in AlGaN/GaN HEMTs: a study based on pulsed and transient measurements. Semicond. Sci. Technol. 28, 074021, 2013.

[51] P.H. Ladbrooke, S.R. Blight. Low-field low-frequency dispersion of transconductance in GaAs MESFETs with implications for other rate-dependent anomalies. IEEE Trans. Electron Devices, 35, 257, 1988.

[52] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. IEEE Trans. Electron Devices 48, 560, 2001.

[53] F. Medjdoub. Ultrathin barrier GaN-on-Silicon devices for millimeter wave applications. Microelectronics Reliability, 54, 1, 2014.

[54] M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. VanHove, Tian-Li Wu, S. Decoutere, G. Meneghesso, E. Zanoni. Trapping and reliability assessment in D-Mode GaN-based MIS-HEMTs for power applications. IEEE Trans. Power Electronics 29, 2199, 2014.

[55] M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, U. K. Mishra, Y. Pei, and E. Zanoni. Investigation of trapping and hot-electron effects in GaN HEMTs by means of a combined electrooptical method. IEEE Trans. Electron Devices 58, 2996, 2011.

[56] A. Malmros, P. Gamarra, M.-A. di Forte-Poisson, H. Hjelmgren, C. Lacam, M. Thorsell, M. Tordjman, R. Aubry, and N. Rorsman. Evaluation of thermal versus plasma-assisted ALD Al_2O_3 as passivation for InAlN/AlN/GaN HEMTs. IEEE Electron Device Lett. 36, 235, 2015.

[57] H. Hahn, B. Reuters, H. Kalisch and A. Vescan. AlN barrier HFETs with AlGaN channels to shift the threshold voltage to higher positive values: a proposal. Semicond. Sci. Technol. 28, 074017, 2013.

[58] A. Platzker, A. Palevsky, S. Nash, W. Struble, and Y. Tajima. Characterization of GaAs devices by a versatile pulsed I-V measurement system. IEEE MTT-S Int. Microwave Symp. Dig. 3, 1137–1140, 1990.

[59] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman. The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's IEEE Electron Device Lett. 21, 268, 2000.

[60] A. V. Vertiatchikh and L. F. Eastman. Effect of the surface and barrier defects on the AlGaN/GaN HEMT low-frequency noise performance. IEEE Electron Device Lett. 24, 535, 2003.

[61] W. S. Tan, P. A Houston, P. J. Parbrook, G. Hill and R. J. Airey. Comparison of different surface passivation dielectrics in AlGaN/GaN heterostructure field effect transistors. J. Phys. D: Appl. Phys. 35, 595, 2002.

[62] F. Karouta, M. C. Krämera, J. J. Kwaspen, A. Grzegorczyk, P. Hageman, B. Hoex, W.M.M. Kessels, J. Klootwijk, E. Timmering, and M.K. Smit. Influence of the structural and compositional properties of PECVD Silicon Nitride layers on the passivation of AlGaN/GaN HEMTs. ECS Transactions, 16, 181-191, 2008.

[63] B. J. Ansell, I. Harrison, and C. T. Foxon. The effect of surface passivation and illumination on the device properties of AlGaN/GaN HFETs. Phys. stat. sol. (a) 188, 279, 2001.

[64] G. I. Ng, H. Zhou, S. Arulkumaran, Y. K. T. Maung. Reduced surface leakage current and trapping effects in AlGaN/GaN high electron mobility transistors on silicon with SiN/Al_2O_3 passivation. Appl. Phys. Lett. 98, 113506, 2011.

[65] G. Zhu, H. Wang, Y. Wang, X. Feng, and A. Song. Performance enhancement of AlGaN/AlN/GaN high electron mobility transistors by thermally evaporated SiO passivation. Appl. Phys. Lett. 109, 113503, 2016.

[66] J. Ma, X. Lu, H. Jiang, C. Liu, and K. M. Lau. In situ growth of SiN_x as gate dielectric and surface passivation for AlN/GaN heterostructures by metalorganic chemical vapor deposition. Applied Physics Express 7, 091002, 2014.

[67] X. Lu, J. Ma, H. Jiang, C. Liu, P. Xu, and K. M. Lau. Fabrication and Characterization of Gate-Last Self-Aligned AlN/GaN MISHEMTs with in situ SiN_x gate dielectric. IEEE Trans. Electron Devices, 62, 1862, 2015.

[68] X. Lu, J. Ma, H. Jiang, and K. M. Lau. Characterization of in situ SiN_x thin film grown on AlN/GaN heterostructure by metal- organic chemical vapor deposition. Appl. Phys. Lett. 104, 032903, 2014.

[69] F. Medjdoub, M. Zegaoui, A. Linge, B. Grimbert, R. Silvestri, M. Meneghini, G. Meneghesso, E. Zanoni. High PAE high reliability AlN/GaN double heterostructure. Solid-State Electronics 113, 49, 2015.

[70] J. Derluyn, S. Boeykens, K. Cheng, R. Vandersmissen, J. Das, W. Ruythooren, S. Degroote, M. R. Leys, M. Germain, and G. Borghs. Improvement of AlGaN/GaN high electron mobility transistor structures by in situ deposition of a Si_3N_4 surface layer. J. Appl. Phys., 98, 54501, 2005.

[71] B.P. Downey, D.J. Meyer, D.S. Katzer, T.M. Marron, M. Pan c, X. Gao. Effect of SiN_x gate insulator thickness on electrical properties of $SiN_x/In_{0.17}Al_{0.83}N$/AlN/GaN MIS–HEMTs. Solid-State Electronics 106, 12, 2015.

[72] M. Miczek, C. Mizue, T. Hashizume and B. Adamowicz. Effects of interface states and temperature on the C-V behavior of metal/insulator/AlGaN/GaN heterostructure capacitors. J. Appl. Phys 103, 104510, 2008.

[73] M. Higashiwaki, T. Mimura and T. Matsui. AlN/GaN insulated-gate HFETs using Cat-CVD SiN. IEEE Electron Device Lett. 27, 719, 2006.

[74] M. Higashiwaki, N. Hirose, and T. Matsui. Cat-CVD SiN-passivated AlGaN-GaN HFETs with thin and high Al composition barrier layers. IEEE Electron Device Lett. 26, 139, 2005.

[75] J. R. Shealy, T. R. Prunty, E. M. Chumbes, and B. K. Ridley. Growth and passivation of AlGaN/GaN heterostructures. J. Cryst. Growth, 250, 7, 2003.

[76] N. Onojimaa, M. Higashiwaki, J. Suda, T. Kimoto, T. Mimura and T. Matsu. Reduction in potential barrier height of AlGaN/GaN heterostructures by SiN passivation. J. Appl. Phys 101, 043703, 2007.

[77] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena. Presence and origin of interface charges at atomic-layer deposited Al_2O_3/III-nitride heterojunctions. Appl. Phys. Lett. 99, 193504, 2011.

[78] B. Song, M. Zhu, Z. Hu, M. Qi, K. Nomoto, X. Yan, Y. Cao, D. Jena and H. G. Xing. Ultralow-leakage AlGaN/GaN high electron mobility transistors on Si with non-alloyed regrown ohmic contacts. IEEE Electron Device Lett. 37, 16, 2016.

[79] C. Bae, C. Krug, G. Lucovsky, A. Chakraborty and U. Mishra. Surface passivation of n -GaN by nitrided-thin-Ga_2O_3/SiO_2 and Si_3N_4 film. J. Appl. Phys. 96, 2674, 2004.

[80] C. Bae, C. Krug, and G. Lucovskya. Electron trapping in metal-insulator-semiconductor structures on n–GaN with SiO_2 and Si_3N_4 dielectrics. J. Vac. Sci. Technol. A 22, 2379, 2004.

[81] B. Gaffey, L. J. Guido, X.W. Wang, and T. P. Ma. High-quality oxide/nitride/oxide gate insulator for GaN MIS structures. IEEE Trans. Electron Devices 48, 458, 2001.

[82] Y. Hori, Z. Yatabe and T. Hashizume. Characterization of interface states in Al_2O_3/AlGaN/GaN structures for improved performance of high-electron-mobility transistors. J. Appl. Phys. 114, 244503, 2013.

[83] Z. Yatabe, J. T. Asubar and T. Hashizume. Insulated gate and surface passivation structures for GaN-based power transistors. J. Phys. D: Appl. Phys. 49, 393001, 2016.

[84] K. M. Chang, C.C. Cheng, C.C. Lang. Electrical properties of SiN/GaN MIS diodes formed by ECR-CVD. Solid-State Electronics 46, 1399, 2002.

[85] R. Nakasaki, T. Hashizume and H. Hasegawa. Insulator-GaN interface structures formed by plasma-assisted chemical vapor deposition. Physica E 7, 953, 2000.

[86] J. Robertson and B. Falabretti. Band offsets of high-k gate oxides on III–V semiconductors. J. Appl. Phys. 100, 014111, 2006.

[87] T. Zimmermann, Y. Cao, D. Jena, H. G. Xing, and P. Saunier. 4-nm AlN barrier all binary HFET with SiN_x gate dielectric. Int. J. High Speed Electronics Systems, 19, 153, 2009.

CHAPTER 5

InN-based devices

5.1 Introduction to InN

InN has been recognized as a channel material for future ultra-high speed transistors that would boost performance over GaN-based devices and pave the way for terahertz frequency electronics [1,2]. InN is a III-V semiconductor predicted to exhibit unique transport properties due to a small electron effective mass, a very high mobility, and a high electron peak velocity [3-6]. However, a number of impediments related to material issues has prevented the development of any kind of device applications, despite the improvements of the epitaxial growth of InN by PAMBE [7-9]. As grown InN layers, present n-type conductivity, with unintentional free electron concentrations that could be as high as 10^{21} cm^{-3} [10]. Nowadays, the reason for the unintentionally conductivity of InN still remains unclear. Some researchers have found a relation between electron concentration and impurity concentrations, such as oxygen and hydrogen [11,12], while other studies have reported that dislocations act as donors and can contribute also, to some point, to the layer conductivity [13,14].

In addition, it has been reported that a surface accumulation layer exists due to the pinning of Fermi level at about 0.8 eV above the E_c minimum due to intrinsic surface states [10]. It has been reported that the surface state density of the accumulation layer has a range between 2 and 6 x 10^{13} cm^{-2} and its thickness ranges between 5-10 nm [15]. To avoid the electron accumulation, a thin GaN capping on InN was suggested by Kuzmik et al. [16]. An additional problem is the large lattice mismatch between InN and either GaN (~11%) or AlN (~14%) buffer layers [7]. For example, when InN is grown on GaN, InN has a larger in-plane lattice constant than GaN, and thus will present an in-plane compressive strain (plane of growth) and a tensile strain in the [0001] direction [17]. Hence, the piezoelectric component of polarization points opposite to the spontaneous polarization direction (Fig. 5.1). The spontaneous polarization of InN is very close to that of GaN, and the polarization sheet charge at the heterointerface is almost totally piezoelectric [17]. However, the large lattice mismatch between InN and GaN with a critical thickness of ~2 monolayers [18] does not allow for thin InN pseudomorphic layers to be grown on GaN and benefit from the induced large piezo-electric charge, which would be very advantageous for HEMT device

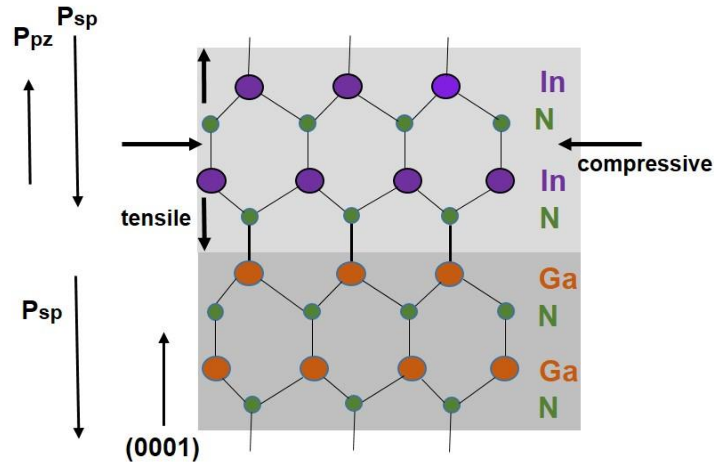


Fig. 5.1 Crystal structure and polarization fields in the InN/GaN structure where GaN is relaxed, and InN is assumed coherently strained (reproduced from C. Wood, D. Jena [ref. 17]).

---

applications; in reality almost immediately misfit dislocations are introduced which lead to strain relaxation. Hence, the development of InN channel transistors is still hampered due to the absence of a suitable lattice matched substrate and the difficulty to fabricate a gate contact that could control the electron charge inside the InN channel. The possibility that will be examined in the following studies is the formation and the properties of MIS gates and InN MISFET transistors. To optimize the purity of the SiN_x/InN interface and exclude extrinsic effects, the SiN_x layer was deposited in situ in the PAMBE system on the previously grown InN layer. This excludes the exposure of the InN surface to atmosphere and its oxidation before the SiN_x/InN heterojunction formation.

5.2 SiN_x/InN/GaN structures with 2 nm ultrathin InN layer

Two SiN_x/InN-on-GaN/Al_2O_3 (0001) samples were grown in the PAMBE system. Commercially available high resistivity (Fe-doped) Ga-face GaN (0001) epilayers grown by MOVPE on Al_2O_3 (0001), were used as substrates. A 2 nm thin InN layer was grown directly on the substrate, under stoichiometric growth conditions (indium/nitrogen flux ratio=1) that are known to result to a two-dimensional InN growth mode and full coverage of the GaN (0001) substrate [8]. Finally, a SiN_x layer was grown on top, under nitrogen-rich conditions with a deposition rate of 0.1 /min, using a silicon sublimation source. The substrate temperature during SiN_x deposition was 150 ^oC, in order to avoid possible decomposition of the InN layer. Two samples with different SiN_x thicknesses (5

and 10 nm) were grown. RHEED observations during growth revealed a streaky pattern for both the cleaned GaN (0001) substrate surface and the surface of the grown InN (0001) layer, suggesting atomically smooth surfaces in both cases. During the growth of the SiN_x layer, the RHEED pattern became fuzzy, suggesting an amorphous SiN_x layer growth at 150 ^oC.

The average R_{sh}, N_s, and μ were determined at room temperature by conductivity and Hall-effect measurements with a magnetic field of 0.4 T, on van der Pauw patterns defined by optical lithography. For both SiN_x thicknesses, R_{sh} was in the range of 1–2x10^3 Ohm/sq. For 5 nm SiN_x thickness, the N_s and μ values were 5.8x10^{13}cm^{-2} and 15 cm^2/V s, while for 10 nm SiN_x were 6.8x10^{13}cm^{-2} and 24 cm^2/V s, respectively. These apparent concentrations are much higher compared to the values determined by C-V measurements (presented later) and suggest inaccuracy of the Hall-effect measurements, probably as a result of the high series resistances and inhomogeneities in the ultrathin InN heterostructures. In any case, very low mobilities are expected due to InN strain relaxation by introduction of misfit dislocations at the InN/GaN interface.

Discrete MISCAP devices with circular shape of diameter d=100 μm (Fig. 5.2(a)), as well as MISFET devices with gate length L_g~1 μm and gate width W~50 μm, were fabricated with the same processing steps. The source-gate and the gate-drain spacing of the MISFETs were L_{sg}~1 μm and L_{gd}~2 μm, respectively. Device isolation was performed using BCl_3/Ar reactive ion etching. Ti/Al/Ni/Au (30/170/40/50 nm) ohmic metal stacks were deposited by e-beam evaporation on the InN surface after the selective removal of the SiN_x by SF_6 plasma etch. The ohmic metals were not annealed due to the known Fermi level pinning and electron accumulation on the InN surface. The mean R_c, measured by the transmission line model (Fig. 5.2(b)), was R_c=0.47 – 0.56 Ohm mm. Finally, Ni/Au (30/100 nm) metallization on the SiN_x surface was used for the metal of MISCAPs and the gate of MISFETs. Figure 5.2 shows a schematic cross-section and a SEM image for the fabricated Ni/SiN_x/InN MISCAPs. All the MISCAPs exhibited insulating characteristics with low leakage current at both positive and negative bias regions (Fig. 5.3). For the MISCAP with 5 nm SiN_x dielectric, the applied bias ranged between -2.5 V and +2.5 V. The current was increasing with the applied voltage for both polarities, and it became 6.6 x 10^{-2} and -5.7 x 10^{-2} A/cm^2 for 2.5 V and -2.5 V bias, respectively. The MISCAPs with 10 nm SiN_x could withstand significantly higher voltage with the ~2 orders of magnitude further reduction in the current, indicating that the thicker dielectric is more effective in leakage suppression as compared with 5

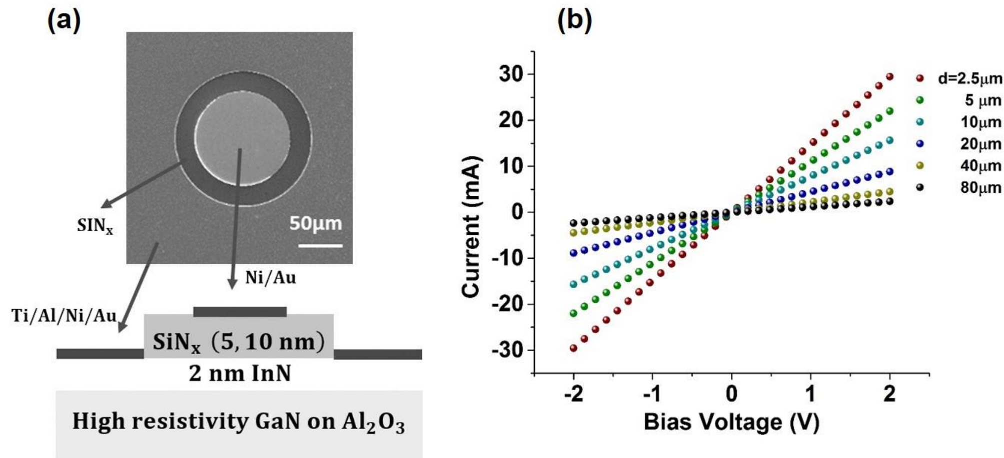


Fig. 5.2 (a) Schematic cross section and SEM image of a 100 µm diameter Ni/SiN_x/InN discrete MISCAP device, (b) example of I-V measurements of a TLM pattern with d=2.5-80 µm pad distances for an InN test structure.

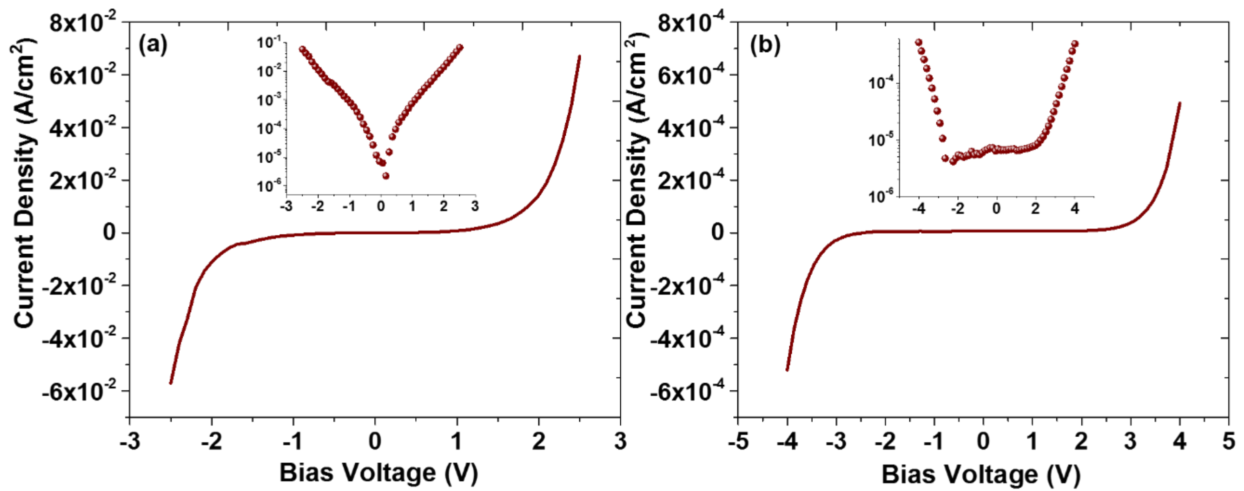


Fig. 5.3 I-V characteristics of a 100 µm diameter Ni/SiN_x/InN MISCAP device for (a) 5 nm and (b) 10 nm SiN_x dielectric. The insets show the I-V characteristics in semi-logarithmic scale.

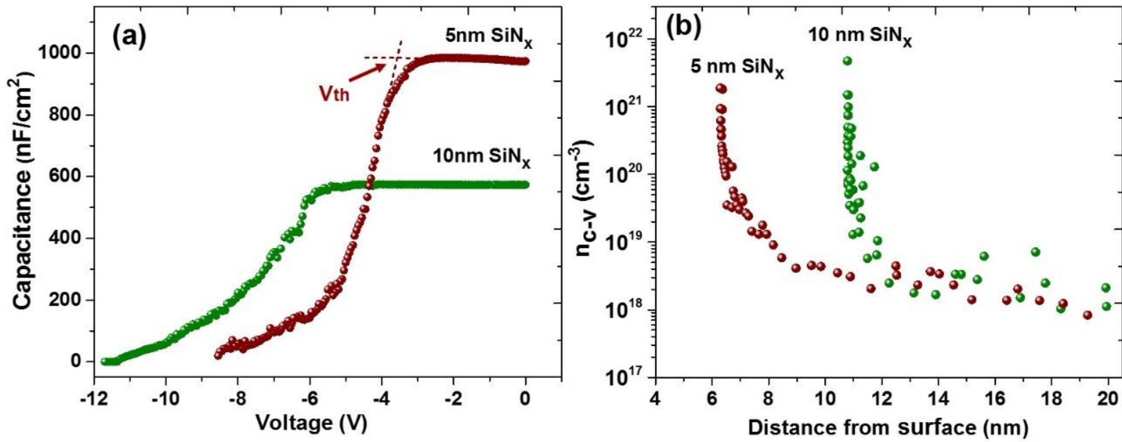


Fig. 5.4 (a) C-V plots of the Ni/SiN_x/InN MISCAP devices with 5 and 10 nm SiN_x thicknesses, measured at room temperature with frequency 1 MHz; (b) charge distributions with distance from the SiN_x surface, as estimated from the C-V measurements.

---

nm SiN_x thickness. The applied bias range was from -4 V to +4 V. A low leakage current of ~5x10^{-6} A/cm^2 remained constant for bias up to ±2 V whilst it started increasing above ~2 V, being 4.9x10^{-4} and -5.2x10^{-4} A/cm^2 for +4 and -4 V bias, respectively (Fig. 5.3).

Figure 5.4 (a) shows the C-V characteristics at room temperature of the MISCAPs, measured by sweeping from positive to negative bias, with a 0.05 V step, with a sinusoidal voltage variation of 10 mV amplitude and frequency f=1 MHz. The plateau capacitance was ~980 and 575 nF/cm^2 for 5 and 10 nm SiN_x, respectively, and corresponds to the electron accumulation condition and the sheet density of electrons confined in the 2 nm InN layer. The efficient modulation of the electron concentration in the 2 nm InN layer is evidenced by the transition from accumulation to depletion, at highly reverse bias voltages. Threshold voltage (V_{th}) values of - 3.7 and -6.0 V were estimated for the 5 and 10 nm SiN_x MISCAPs, respectively, from the intersect of linear extrapolations of the capacitance curves of the accumulation and depletion regions (Fig. 5.4(a)). A negative threshold shift of 2.3 V is observed for the MISCAP with 10 nm SiN_x, as compared with 5 nm SiN_x. This shift with increase of the dielectric thickness has been reported by several groups [19-21]. Ganguly et al. [19] studied the Ni/Al_2O_3/AlN/GaN MIS system and showed that the decrease of V_{th} decrease with increasing dielectric thickness can be explained by the presence

of a positive charge at the Al_2O_3/AlN interface, which compensates the negative polarization charge on the AlN surface. Similar findings were also reported recently [21] for $SiN_x/In_{0.17}Al_{0.83}N$/AlN/GaN structures, consisting of a SiN_x layer deposited by PAMBE on a MOVPE grown InAlN/AlN/GaN HEMT structure. Thus, the threshold decrease with SiN_x thickness in the current work could be also attributed to the presence of positive charge at the SiN_x/InN interface. This is further studied in the next paragraph, with the assistance of charge control calculations. Fig. 5.4(b) exhibits the carrier density profile $n_{c\text{-}v}(z)$ with the distance from the surface, as extracted from the C-V measurements of Fig. 5.4(a), using $n_{c\text{-}v}=(C^3/q\varepsilon_s)\,(dC/dV)^{-1}$. A sharp confinement of a high electron concentration inside the 2 nm InN layer is observed. The integration of $n_{c\text{-}v}$ from V_{th} up to 0 V yields N_s of ~2.1×10^{13} cm^{-2} for both SiN_x thicknesses.

For a better understanding of the effect of SiN_x on the N_s and V_{th} values, it was interesting to compare the experimental results with the carrier distribution and the equilibrium energy band diagrams calculated using a self-consistent Schrodinger-Poisson solver (SCSP) for the Ni/SiN_x/InN/GaN structure. Conduction band discontinuities and polarization-related parameters incorporated in the calculations were set according to the literature [22-25] Specifically, $\Delta E_{C(InN/GaN)} = -2.4$ eV [24] is the conduction band offset of InN compared to GaN and $\Delta E_{C(SiN/InN)} = 3.1$ eV [23] is the conduction band offset of SiN compared to InN. Only spontaneous polarization was taken into account in the simulations, i.e., InN is treated as fully relaxed on the GaN-on sapphire substrate [7]. Spontaneous polarization values of -0.029 C/m^2 and -0.032 C/m^2 were used for GaN and InN, respectively [22] For the boundary conditions, we used $q\Phi_B=3.0$ eV as the Ni/SiN_x surface barrier height, according to $q\Phi_B=q\Phi_M-X$, with SiN_x electron affinity $X=2.1$ eV [23] and work function of Ni metal $q\Phi_M = 5.1$ eV. Neutrality was considered as the boundary condition at the bottom surface of the GaN buffer. The donor concentration inside the InN layer was set at $N_d=10^{18}$ cm^{-3}, to be in agreement with experimental Hall-effect measurements on thicker InN films. In addition to the polarization charges, a fixed positive interface charge Q_{if} was introduced at the SiN_x/InN interface. This is indicatively shown in the energy band diagram of Fig. 5.5(a), for the Ni/SiN_x/InN/GaN structure with 5 nm SiN_x thickness.

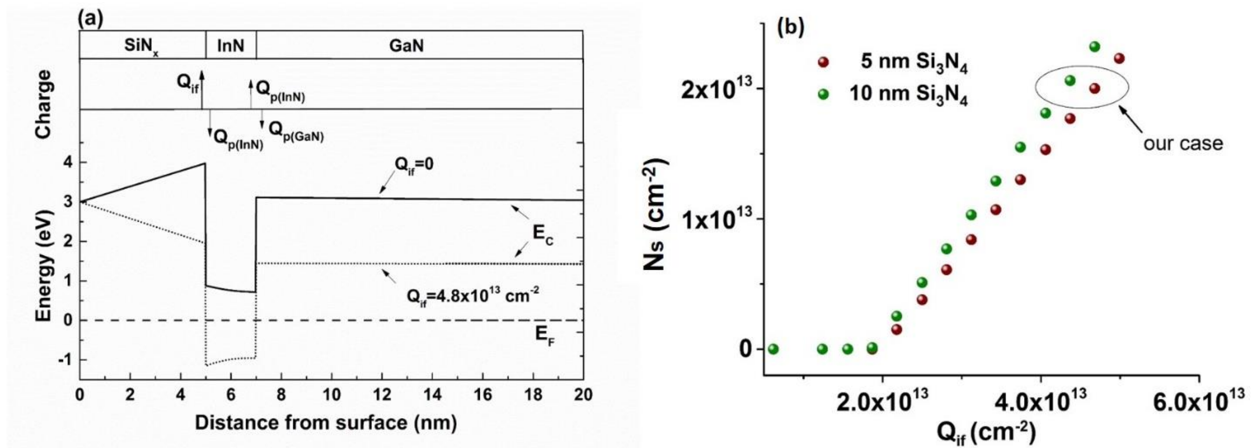


Fig. 5.5 (a) Charge distribution and conduction band diagram for the Ni/ SiN_x/InN/GaN structure with 5 nm SiN_x thickness, for the cases of Q_{if}=0 and Q_{if}=4.8x10^{13}cm^{-2}. (b) The electron concentration N_s in InN versus the fixed charge Q_{if} at the Si_3N_4/InN interface.

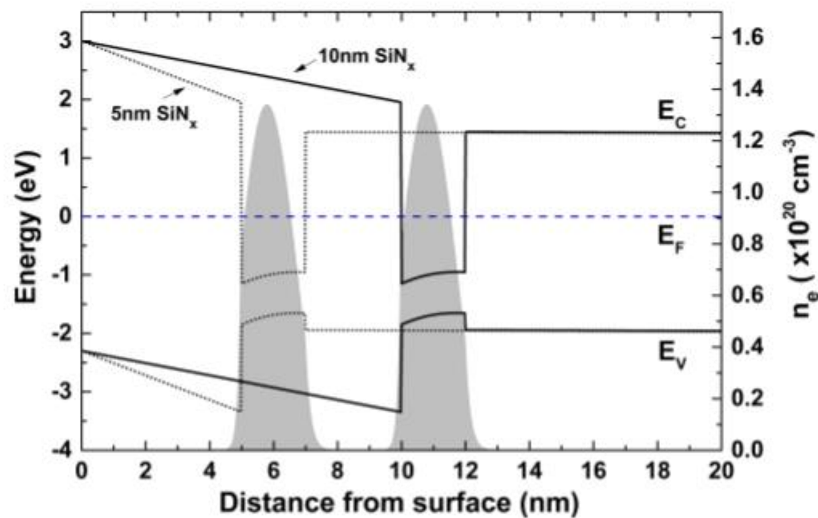


Fig. 5.6 Band diagrams and electron concentration profiles for the Ni/SiN_x/InN/GaN structures with 5 and 10 nm SiN_x thicknesses, where Q_{if} values are considered.

As it was mentioned previously, the presence of a positive Q_{if} at the SiN_x/InN interface is suggested by the observed shift of V_T to more negative value with doubling the SiN_x thickness. Then it was investigated which value of Q_{if} could reproduce the experimental N_s value, as calculated from C-V measurements. Assuming Q_{if}=0, the SCSP calculations show that the structures should be completely depleted of electrons in the 2 nm InN. However, by including a positive sheet charge at the SiN_x/InN interface of $Q_{if} \approx 4.8 x 10^{13}$ cm^{-2} for 5 nm SiN_x and $\approx 4.4 x 10^{13}$ cm^{-2} for 10 nm SiN_x, the SCSP calculations predict N_s values in the relaxed InN layer in agreement with the experimental ones.

Figure 5.5(b) shows the calculated electron concentration N_s in InN versus the fixed charge Q_{if} at the Si_3N_4/InN interface. A depleted InN is observed for $Q_{if} < 2 \cdot 10^{13} cm^{-2}$, whereas N_s starts increasing above $Q_{if} = 2 x 10^{13} cm^{-2}$. It should be also noticed that even if a high residual strain of ~30 % is assumed, the calculations suggest only a slight increase (~4%) of the Q_{if} value to reproduce the experimental values of N_s.

Figure 5.6 shows the band profiles and the electron distribution for 5 and 10 nm SiN_x thicknesses, for the considered Q_{if} values. The peak of the electron concentration is located at a distance of 5.9 and 10.8 nm from the surface of the 5 and 10 nm SiN_x layer, respectively, which matches well with the values extracted from C-V data. Figure 5.7 shows the theoretical and the experimental C-V plots for 5 and 10 nm SiN_x thickness, where Q_{if} was set as a fitting parameter to match the V_{th} from the experimental results. The effect of interface states, which are ignored in the SCSP calculations, is obvious below V_{th} leading to stretch out along the voltage axis.

The capability of the MIS capacitors to control the electron concentration in the InN layer allowed the successful fabrication and operation of MISFET InN transistors. The output characteristics of the transistors are shown in Fig. 5.8. Drain- source voltage was limited to 2.5–3 V due to device breakdown that was observed at these values. This has been associated with the small band gap of InN (~0.65 eV) that may result in an early channel breakdown [26]. For the used V_{ds} range, a variation of the drain-source current was observable only for highly negative gate-source voltages. The InN MISFETs with 5 nm SiN_x thickness exhibited maximum I_{ds} of 57 mA/mm at V_{gs} = - 4 V, and the channel was pinched-off at V_{gs} = - 9.5 V. The MISFET with 10 nm SiN_x thickness exhibited maximum I_{ds} of 63 mA/mm at V_{gs} = - 4 V, which changed very slightly with V_{gs} between -4 and -7 V. A stronger effect on I_{ds} was observed for V_{gs}>-7 V, and the channel

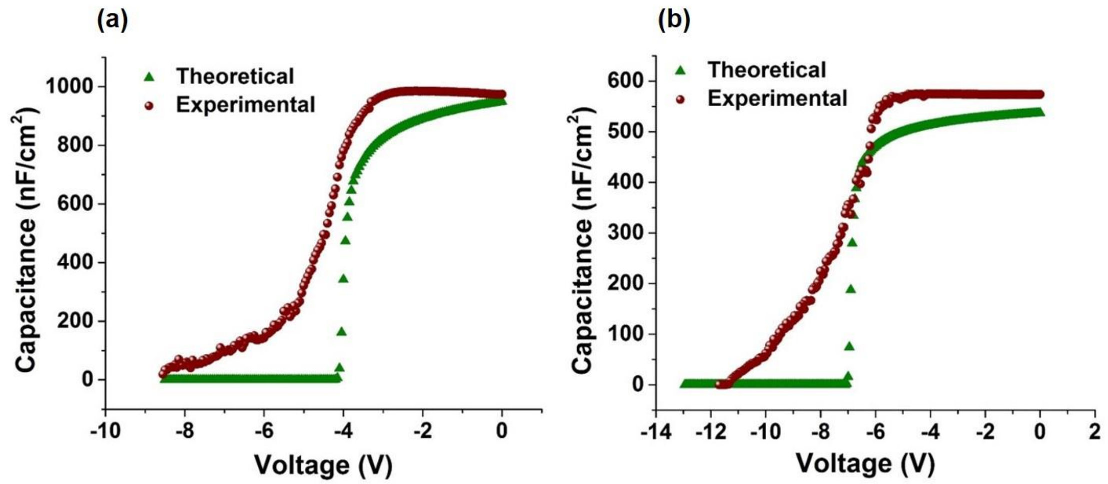


Fig. 5.7 Comparison of experimental and theoretical C-V curves for (a) 5 and (b) 10 nm SiN_x thickness.

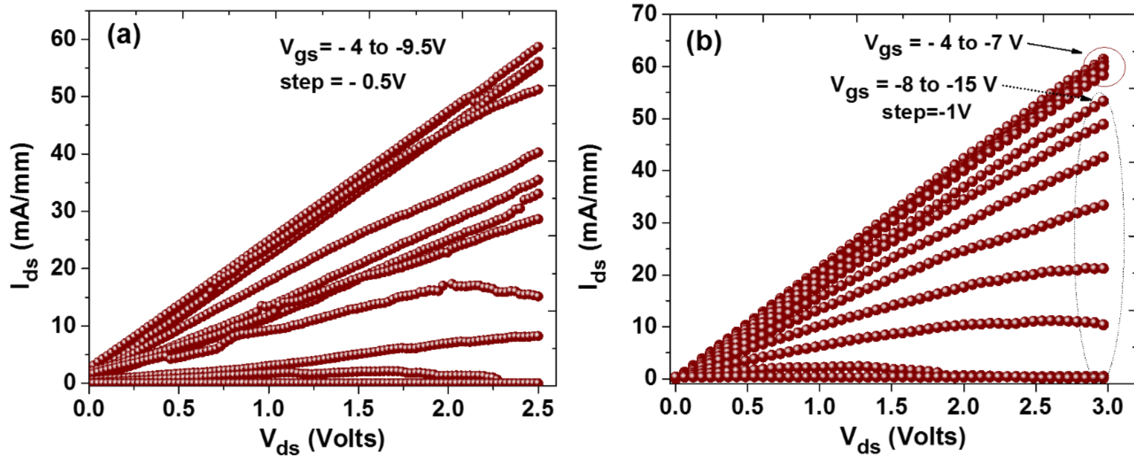


Fig. 5.8 I_{ds}–V_{ds} characteristics for SiN_x/InN/GaN MISFET devices, for (a) 5 nm and (b) 10 nm SiN_x thicknesses. The gate length and width were 1 and 50 µm, respectively.

---

was pinched-off at V_{gs} = - 15 V. The gate leakage currents under pinch-off conditions were in the range 1–3x10^{-3} A/mm. The MISFET channels pinched-off at significantly higher V_{gs} compared to the V_{th} values extracted from C-V measurements on MISCAPs. The cause for this difference may be parallel conduction paths in the channel with varying efficiency of gate control and charge instabilities in the devices due to electron trapping. High parasitic source resistances ($R_s=R_c+(L_{sg}/W)R_{sh}$, where L_{sg} is the source-gate distance) caused by low electron mobilities may be responsible for the observed small drain-source currents, as it has been found in the past for other non-optimized HEMT systems [27].

5.3 SiN_x/InN/GaN structures with 4/7/10 nm thin InN layer

Three SiN_x/InN/GaN/Al_2O_3 (0001) heterostructures were grown in the PAMBE system differing only in the InN layer thickness (4, 7, and 10 nm), while all the other growth parameters were kept constant. Commercially available high resistivity (Fe-doped) Ga-face GaN (0001) epilayers, grown by MOVPE on Al_2O_3 (0001), were used as substrates. A 100 nm GaN layer was grown at 700 ^oC in order to improve the surface smoothness and GaN crystal purity. The background electron concentration, according to earlier calibration by Hall-effect measurements on 0.5–1.0 μm thick GaN buffer layers, was about ~10^{16} cm^{-3}. Next, the temperature was reduced to 350 ^oC and an InN layer was grown, under stoichiometric growth conditions. A 7 nm thick SiN_x layer was grown on top at 250 ^oC, under nitrogen-rich conditions in order to avoid possible decomposition of the InN layer. MISCAP devices and MISFETs were fabricated with the same processing steps using the same process flow with previous SiN_x/InN devices. The fabrication of devices started with mesa isolation; (Ti/Al/Ni/Au) ohmic contact formation after the selective removal of SiN_x in the ohmic region resulted in mean contact resistances, measured by the transmission line model, ranged between 0.7 and 1.1 Ohm mm. Finally, (Ni/Au) metallization on the SiN_x surface was used for the metal of MISCAPs and the gate of MISFETs (Fig. 5.9(a)).

FTIR spectroscopy was used for evaluating the chemical bonding configuration of the SiN_x films. The transverse-optical (TO) mode position of the Si-N stretching vibration of the 7 nm MBE grown SiN_x layers was observed at a wavenumber of 857 cm^{-1}, as shown in Fig. 5.9(b). The observed shift of 17 cm^{-1} above the 840 cm^{-1} value of stoichiometric Si_3N_4 may be an evidence of nitrogen-rich MBE SiN_x layers [28]. AFM revealed very smooth surfaces for all samples, characteristic for two-dimensional growth mode of the layers (Fig. 5.10). The apparent surface defects consisted of

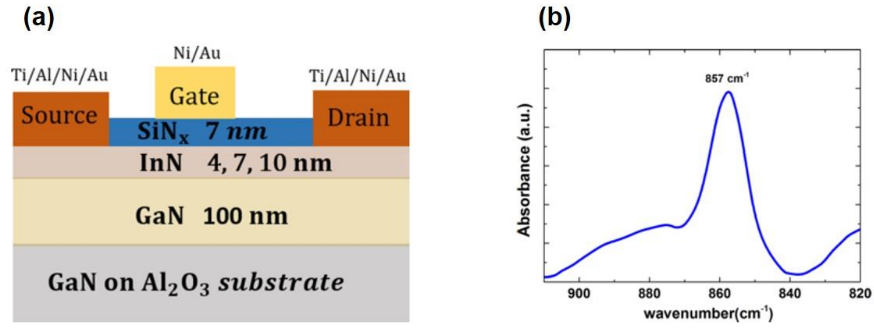


Fig. 5.9 (a) Schematic cross section of the fabricated InN channel MISFET devices, (b) FTIR absorbance spectrum measured on the 7 nm SiN_x/7 nm InN/100 nm GaN/Al_2O_3 (0001) sample.

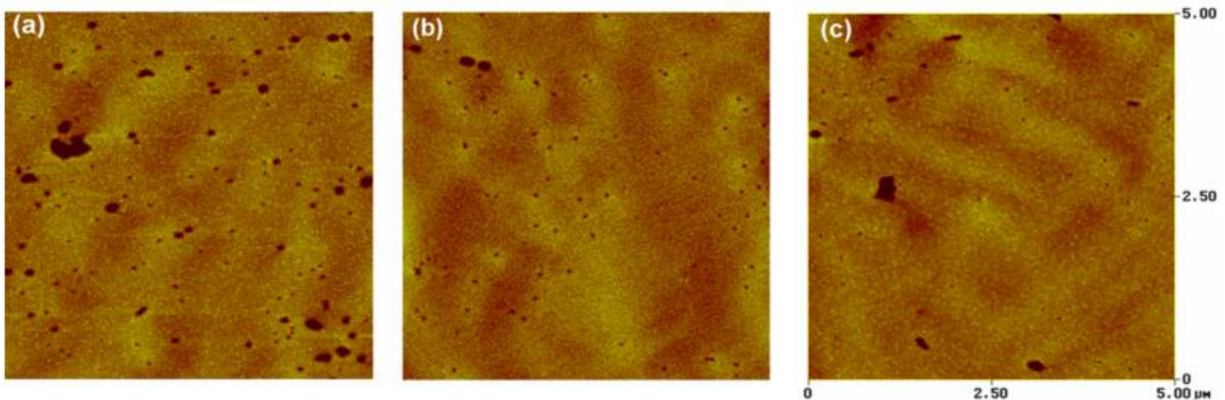


Fig. 5.10 AFM micrographs of 5x5 μm^2 showing the surface of SiN_x/InN/GaN heterostructures, grown by PAMBE on (0001) sapphire substrate, for (a) 4, (b) 7, and (c) 10 nm InN thickness. Excluding the pits originating from the GaN templates, the RMS roughness was (a) 1.2, (b) 0.6, and (c) 0.7 nm, respectively.

deep pits, randomly distributed over the surfaces, with the highest density observed in the 4 nm thick InN structure. These pits are morphological defects existing in the MOVPE GaN templates and are not related with the PAMBE growth of the epilayers. Nevertheless, the areas free of pits are smooth enough for the fabrication of electronic devices, with RMS roughness of 1.2, 0.6, and

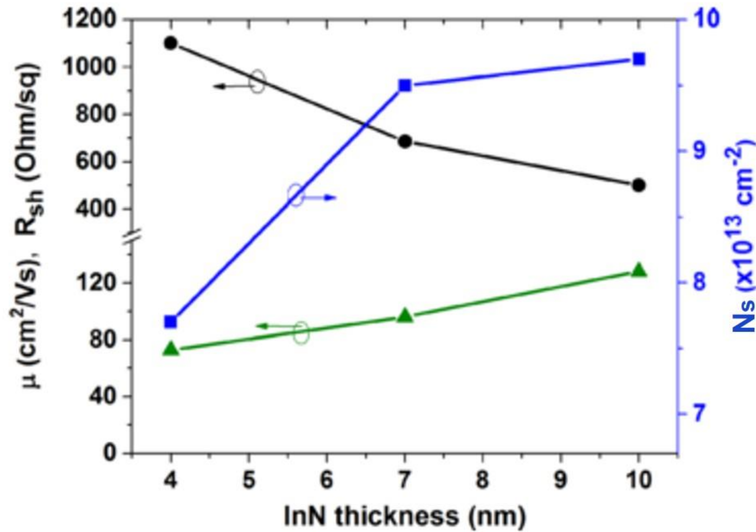


Fig. 5.11 Room temperature Hall-effect measurements showing the dependence of sheet resistance, mobility and sheet carrier density, of 7 nm SiN_x/InN/GaN heterostructures, on the InN thickness.

0.7 nm for 4, 7, and 10 nm InN thickness, respectively, over the 5 x 5 μm^2 scanned areas. Conductivity and Hall-effect measurements were performed at room temperature on van der Pauw patterns defined by optical lithography. Figure 5.11 shows the dependence of R_{sh}, μ, and N_s as a function of InN thickness. For the few nanometer InN thickness range examined here, the mobility and sheet electron density were observed to increase with InN thickness up to values of 128 cm^2/Vs and 9.7 x $10^{13}/cm^2$ for the structure with 10 nm thick InN layer, while the sheet resistance was found to decrease reaching a minimum value of 501 Ohm/sq.

Figure 5.12 exhibits the room temperature I-V measurements of the fabricated Ni/SiN_x/InN MISCAP devices. The reverse leakage current was 3.1, 5.5, and 4.5x10^{-4} A/cm^2 at -3 V for devices with 4, 7, and 10 nm InN thickness, respectively, while a low level of ~10^{-6} A/cm^2 from -2 to +2 V was sustained for 4 and 7 nm thick InN before the onset of the leakage.

To get more insight on the leakage current of the MISCAPs, the electrical conduction of SiN_x was studied, following Sze [29] and other authors [30-33], by analyzing the charge conduction mechanisms, discussed in chapter 2 (par. 2.3.5).

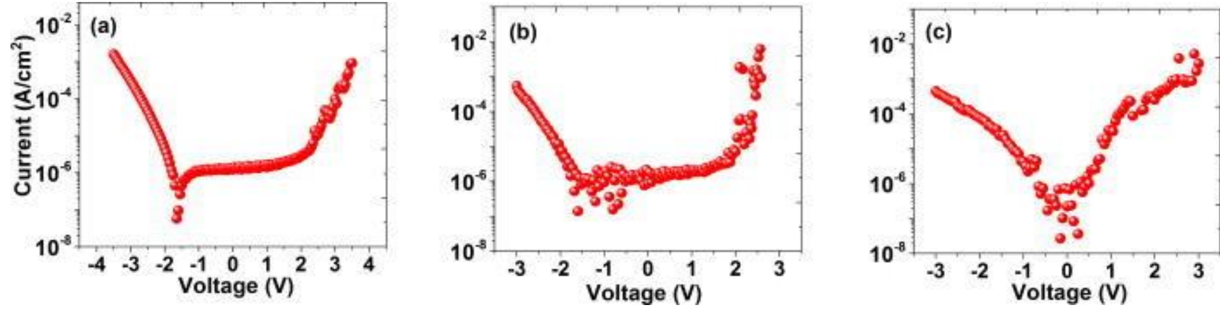


Fig. 5.12 I-V characteristics of Ni/SiN_x/InN MISCAP devices for (a) 4 nm and (b) 7 nm and (c) 10nm InN thickness.

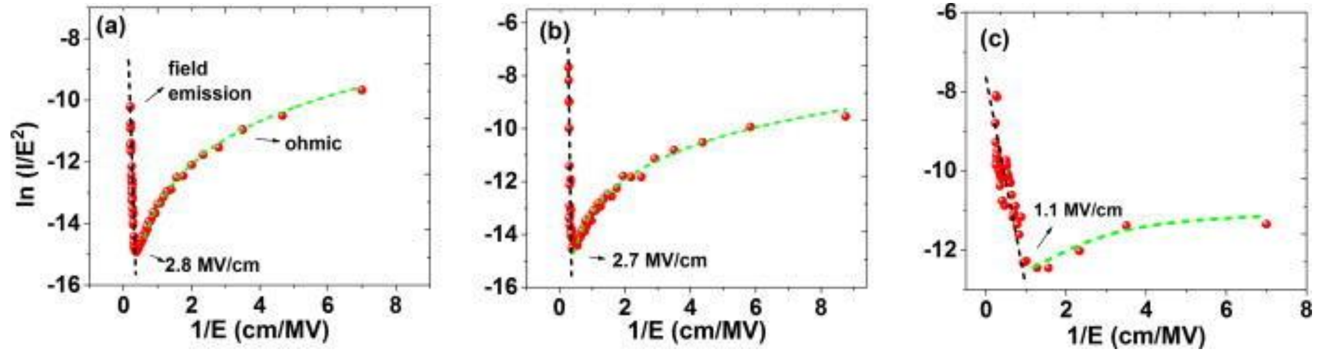


Fig. 5.13 Field emission plots [ln(I/E^2)-1/E] of Ni/SiN_x/InN MISCAP devices for (a) 4 nm, (b) 7 nm, and (c) 10 nm InN thickness.

By analyzing the ln(I/E^2) versus 1/E plot (E is the electric field in SiN_x given by E≈V/d and d is the SiN_x thickness), a logarithmic dependence was revealed at low fields (Fig. 5.13). This is an evidence of ohmic (hopping) conduction (see also Eq. 2.41 for ohmic conduction, from which it can be deduced that $\ln(I/E^2) \propto \ln(1/E) - q\varphi/kT$, where φ is the activation energy). Direct tunneling can also occur at low fields if the insulator is very thin (<4 nm); however, the SiN_x layer is 7 nm thick, and thus, this probability is low. On the other hand, a straight line with a negative slope was observed at high fields, which is an indication of field emission tunneling (see also Eq. 2.40 for field emission, from which it can be deduced that $\ln(I/E^2) \propto -[8\pi(2m^*\Phi_B^3)^{1/2}](1/E)$). The two different regions, hopping and field emission, are depicted clearly in Fig. 5.13 for the 4 and 7 nm thick InN structures for positive applied bias.

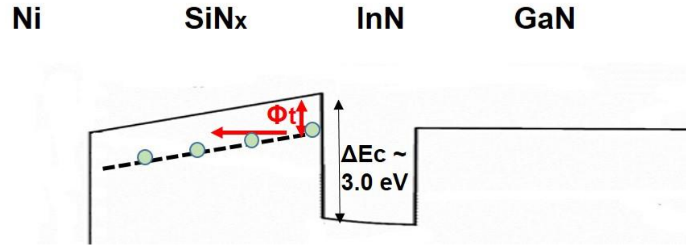
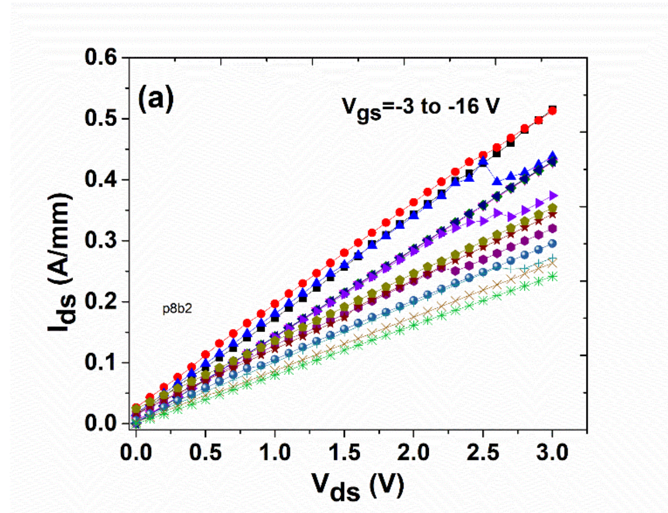
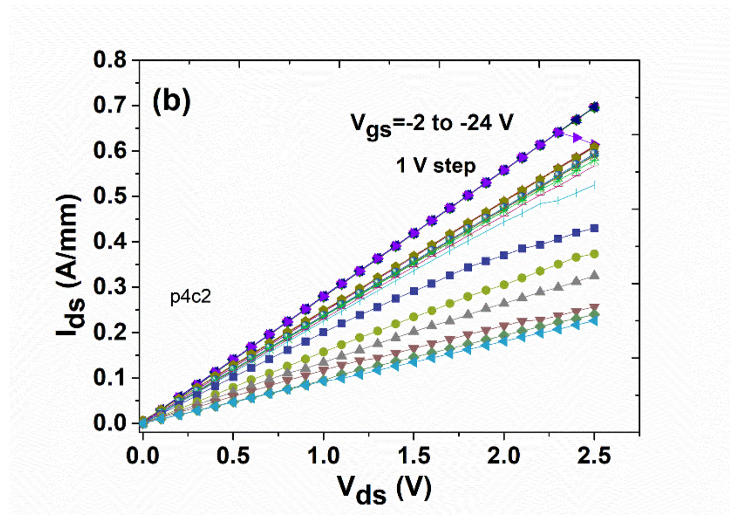


Fig. 5.14 Schematic conduction band diagram of the SiN_x/InN/GaN structure showing the field emission tunneling of electrons from trap states located in the SiN_x, at a trap barrier height Φ_t.

A characteristic inflection point indicates the crossover from hopping to field emission at an electric field of 2.7–2.8 MV/cm. By assuming [34] $m^*=0.30\ m_0$ (m_0 is the electron rest mass) for SiN_x, a barrier height Φ_B (ΔE_c) in the range of 1.1–1.3 eV was extracted from the linear fit of the slope in the high field region, for all the devices with 4 and 7 nm InN thickness. However, this Φ_B value is ~two times lower than the reported theoretical conduction band discontinuity between InN and Si_3N_4, ΔE_c (3.1 eV, [35]). This can be explained by assuming a non-negligible number of traps in the SiN_x. In that case, field emission tunneling of electrons from trap centers in SiN_x may occur, and the extracted Φ_B may represent a trap barrier height Φ_t = 1.1-1.3 eV below the SiN_x conduction band minimum, as depicted in Fig 5.14. Recently, Tapajna et al. observed a similar behavior in Al_2O_3/AlGaN/GaN MOS-HEMTs [36]. On the other hand, devices with 10 nm thick InN did not exhibited sufficiently good linear fits, and thus, no reliable extracted data could be obtained from these structures. However, the onset electric field (1.1 MV/cm) for the field emission region was lower compared with 4 and 7 nm thick InN devices. This may be due to a higher trap density, which requires a lower electric field to initiate the field emission mechanism in the 10 nm thick InN structures.

In order to evaluate the effectiveness of the MISCAPs to modulate the electron concentration in the InN layer, direct current output characteristics were measured for the fabricated MISFETs (Fig. 5.15). It was found that I_{ds} cannot be fully shut-off and V_{gs} can partially modulate I_{ds}, for V_{gs} values between -2 V and -24 V. The maximum current density was found to increase with InN thickness, reaching the value of 1.4 A/mm for the best 10 nm thick InN channel HEMTs, where a maximum V_{ds} of 4 V could be sustained before breakdown occurs. The I_{gs} for all the structures was < 10 mA/mm, implying that the current I_{ds} that cannot be modulated (equals to ~0.2-0.3 A/mm in most





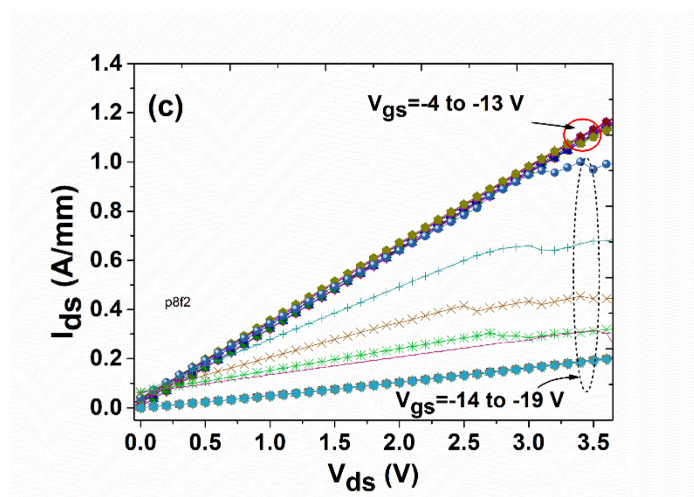


Fig. 5.14 Drain–source characteristics for L_g~1μm MISFETs with (a) 4, (b) 7, and (c) 10 nm InN

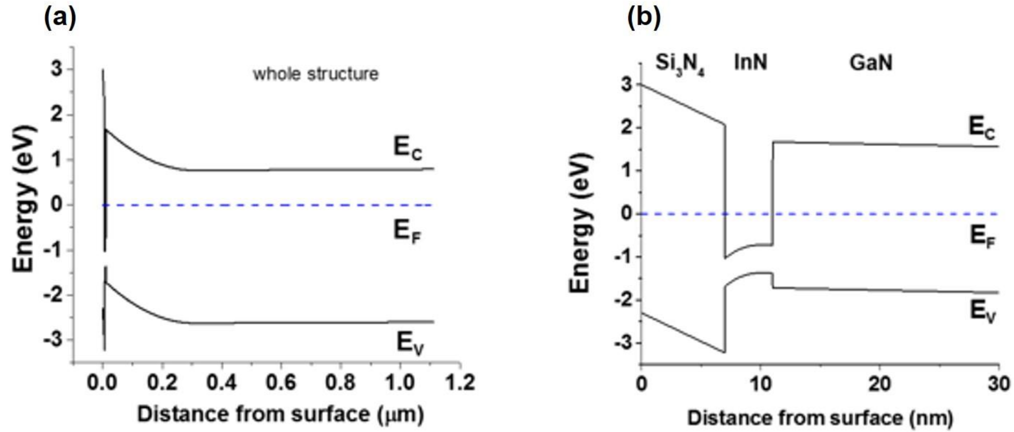


Fig. 5.15 (a) Energy band diagram for the 7 nm SiN_x/4 nm InN/100 nm GaN/1 μm Fe-doped GaN structure , and (b) magnification of the left band diagram for the first 30 nm.

---

devices) is related with channel-buffer leakage. A conductive GaN buffer layer could be a possible source of leakage current in the MISFETs. GaN buffer layers grown in the same PAMBE system exhibited an electron concentration of about 10^{16} cm^{-3}. However, according to self-consistent Schrödinger–Poisson calculations in our structures, a 100 nm thin GaN buffer layer with $10^{16}cm^{-3}$ donor concentration will be depleted due to large conduction band offset ΔE_c between InN and GaN [37] and the bottom interface with the insulating Fe-doped GaN (Fig. 5.15). Thus, the 100 nm, GaN epilayer is not expected to contribute in the leakage current.

In some cases of GaN overgrowth on GaN templates, a residual concentration of unintentional impurities (O, Si, C) might be present at the GaN epilayer/GaN template interface [38]. However, even if a $10^{19}cm^{-3}$ donor concentration is assumed in a 5 nm interfacial area at the GaN epilayer/GaN template interface, the resulting electron density at this interface is low (~$2x10^{12}$ cm^{-2}) compared to the values (10^{13} cm^{-2} range) determined by Hall-effect measurements. Thus, we do not anticipate any conductivity of the GaN epilayer to play a dominant role on the devices pinch-off behavior. The overall experimental results suggest high electron concentrations in the InN layers. Several groups contend that the high density of dislocations formed due to the large lattice mismatch between InN and GaN (>10%) increase conductivity in the InN layers by acting as donors, which contribute electrons to the layers [13,14,39] and thus making difficult to modulate

the channel current by the gate bias and achieve device pinch-off operation. The anticipated high dislocation density in the thin InN layers degrades also the electron transport in the InN channel.

5.4 Summary

We studied the formation of InN MIS capacitors and MISFETs by in-situ deposition of SiN_x dielectric on ultrathin 2 nm InN layers grown on GaN-on sapphire substrates by PAMBE. The MIS capacitors exhibited insulating characteristics and fully depleted the electron concentration in the InN channel, as it was evidenced by C-V and I-V measurements on discrete MIS capacitors and MISFET devices. The comparison of the V_T and N_s experimental results with SCSP calculations suggests the presence of a positive charge at the SiN_x/InN interface of 4.4 – 4.8x10^{13}cm^{-2}, assuming full InN strain relaxation. The MISFET channels could be pinched-off but the maximum currents were limited by low mobility and catastrophic breakdown at low V_{ds} voltages. SiN_x/InN/GaN structures with larger InN thicknesses (4, 7, and 10 nm) were also investigated. MIS capacitor devices were demonstrated and evaluated as potential gates in MISFETs. The maximum drain–source current was increased by increasing the InN thickness and it was 1.2 A/mm for the 10 nm thick InN, although the channel could not fully pinch-off. According to the I-V analysis of the MIS capacitors, the electrical conduction of SiN_x is dominated by hopping between localized states under low electric fields and field emission tunneling at high fields, with an extracted trap barrier height in the range of 1.1–1.3 eV for all the structures.

5.6 Chapter 5 references

[1] J. Kuzmik and A. Georgakilas. Proposal of high-electron mobility transistors with strained InN channel. IEEE Trans. Electron Devices 58, 720, 2011.

[2] V. M. Polyakov and F. Schwierz. Low-field electron mobility in wurtzite InN. Appl. Phys. Lett. 88, 032101, 2006.

[3] B. R. Nag. Electron mobility in InN. J. Cryst. Growth 269, 35, 2004.

[4] V. M. Polyakov and F. Schwierz. Low-field electron mobility in wurtzite InN. Appl. Phys. Lett. 88, 032101, 2006.

[5] K. T. Tsen, C. Poweleit, D. Ferry, H. Lu, and W. J. Schaff. Observation of large electron drift velocities in InN by ultrafast Raman spectroscopy. Appl. Phys. Lett. 86, 222103, 2005.

[6] S. K. O'Leary, B. E. Foutz, M. S. Shur, and L. F. Eastman. Potential performance of indium-nitride-based devices. Appl. Phys. Lett. 88, 152113, 2006.

[7] Heteroepitaxial growth of In-face InN on GaN (0001) by plasma-assisted molecular beam epitaxy. E. Dimakis, E. Illiopoulos, K. Tsagaraki, Th. Kehagias, Ph. Komninou, and A. Georgakilas, J. Appl. Phys. 97, 113520, 2005.

[8] E. Dimakis, E. Iliopoulos, K. Tsagaraki, and A. Georgakilas. Physical model of InN growth on Ga-face GaN (0001) by molecular-beam epitaxy Appl. Phys. Lett. 86, 133104, 2005.

[9] H. Naoi, F. Matsuda, T. Araki, A. Suzuki, and Y. Nanishi. The effect of substrate polarity on the growth of InN by RF-MBE. J. Cryst. Growth 269, 155, 2004.

[10] N. Khan, A. Sedhain, J. Li, J. Y. Lin, and H. X. Jiang. High mobility InN epilayers grown on AlN epilayer templates. Appl. Phys. Lett. 92, 172101, 2008.

[11] N. Miller, E. E. Haller, G. Koblmuller, C. Gallinat, J. S. Speck, W. J. Schaff, M. E. Hawkridge, K. M. Yu, and J. W. Ager. Effect of charged dislocation scattering on electrical and electrothermal transport in n-type InN. Physical Review B 84, 075315, 2011.

[12] C. G. Van de Walle, J. L. Lyons, and A. Janotti. Controlling the conductivity of InN. Phys. Status Solidi A 207, 1024, 2010.

[13] P. D. C. King, T. D. Veal, and C. F. McConville. Unintentional conductivity of indium nitride: transport modelling and microscopic origins J. Phys. Condens. Matter 21, 174201, 2009.

[14] X. Wang, S.-B. Che, Y. Ishitani, and A. Yoshikawa. Threading dislocations in In-polar InN films and their effects on surface morphology and electrical properties. Appl. Phys. Lett. 90, 151901, 2007.

[15] T. A. Komissarova, V. N. Jmerik, S. V. Ivanov, O. Drachenko, X. Wang, and A. Yoshikawa. Identification of the main contributions to the conductivity of epitaxial InN. Physical Review B 84, 035205, 2011.

[16] J. Kuzmık, S. Hascık, M. Kucera, R. Kudela, E. Dobrocka, A. Adikimenakis, M. Micusık, M. Gregor, A. Plecenik, and A. Georgakilas. Elimination of surface band bending on N-polar InN with thin GaN capping. Appl. Phys. Lett. 107, 191605, 2015.

[17] C. Wood, D. Jena. Polarization effects in semiconductors. Springer, New York, 2008.

[18] J. Kioseoglou, Ph. Komninou, J. Chen, G. Nouet, E. Kalesaki, and Th. Karakostas. Structural and electronic properties of elastically strained InN/GaN quantum well multilayer heterostructures. Phys. Status Solidi C 11, 289, 2014.

[19] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena. Presence and origin of interface charges at atomic-layer deposited Al2O3/III-nitride heterojunctions. Appl. Phys. Lett. 99, 193504, 2011.

[20] M. Tapajna and J. Kuzmık. A comprehensive analytical model for threshold voltage calculation in GaN based metal-oxide-semiconductor high-electron-mobility transistors. Appl. Phys. Lett. 100, 113509, 2012.

[21] B.P. Downey, D.J. Meyer, D.S. Katzer, T.M. Marron, M. Pan, X. Gao. Effect of SiN_x gate insulator thickness on electrical properties of $SiN_x/In_{0.17}Al_{0.83}N$/AlN/GaN MIS–HEMTs. Solid-State Electron. 106, 12, 2015.

[22] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, and L. F. Eastman. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures. J. Appl. Phys. 85, 3222, 1999.

[23] J. Robertson and B. Falabretti. Band offsets of high-K gate oxides on III–V semiconductors. J. Appl. Phys. 100, 014111, 2006.

[24] C. G. Van de Walle and J. Neugebauer. Universal alignment of hydrogen levels in semiconductors, insulators and solutions. Nature 423, 626, 2003.

[25] J Kuzmık. InAlN/(In)GaN high electron mobility transistors: some aspects of the quantum well heterostructure proposal. Semicond. Sci. Technol. 17, 540, 2002.

[26] Y. S. Lin, S. H. Koa, C. Y. Chan, S. H. Hsu, H. M. Lee, and S. Gwo. High current density InN/AlN heterojunction field-effect transistor with a gate dielectric layer Appl. Phys. Lett. 90, 142111, 2007.

[27] J. Kuzmik, A. Kostopoulos, G. Konstantinidis, J.-F. Carlin, A. Georgakilas, and D. Pogany. InAlN/GaN HEMTs: A first insight into technological optimization. IEEE Trans. Electron Devices 53, 422, 2006.

[28] O. Debieu, R. P. Nalini, J. Cardin, X. Portier, J. Perriere, and F. Gourbilleau. Structural and optical characterization of pure Si-rich nitride thin films. Nanoscale Res. Lett. 8, 31, 2013.

[29] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1981); J. Appl. Phys. 38, 2951 (1967).

[30] C. A. Mead. Electron transport mechanisms in thin insulating films. Phys. Rev. 128, 2088 1962.

[31] E. J. M. Kendall. The conduction processes in silicon nitride. Can. J. Phys. 46, 2509, 1968.

[32] Y. Misawa and H. Yagi. Electrical conduction of silicon nitride films deposited by SiH_4-NH_3 reaction. Jpn. J. Appl. Phys. 15, 1045, 1976.

[33] M. Tao, D. Park, S. N. Mohammad, D. Li, A. E. Botchkerav, and H. Morkoc. Electrical conduction in silicon nitrides deposited by PECVD. Philos. Mag. B 73, 723, 1996.

[34] T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa. Surface passivation of GaN and GaN/AlGaN heterostructures by dielectric films and its application to insulated-gate heterostructure transistors. J. Vac. Sci. Technol. B 21, 1828, 2003.

[35] J. Robertson and B. Falabretti. Band offsets of high K gate oxides on high mobility semiconductors. Mater. Sci. Eng., B 135, 267, 2006.

[36] M. Tapajna, L. Valik, F. Gucmann, D. Gregusova, K. Frohlich, S. Hascık, E. Dobrocka, L. Toth, B. Pecz and J. Kuzmik. Low-temperature atomic layer deposition-grown Al_2O_3 gate dielectric for GaN/AlGaN/GaN MOS HEMTs: Impact of deposition conditions on interface state density. J. Vac. Sci. Technol. B 35, 01A107, 2017.

[37] K. A. Wang, C. Lian, N. Su, D. Jena, and J. Timler. Conduction band offset at the InN/GaN heterojunction Appl. Phys. Lett. 91, 232117, 2007.

[38] Y. Cao, T. Zimmermann, H. Xing, and D. Jena. Polarization-engineered removal of buffer leakage for GaN transistors. Appl. Phys. Lett. 96, 042102, 2010.

[39] L. F. J. Piper, T. D. Veal, C. F. McConville, H. Lu, and W. J. Schaff. Origin of the n-type conductivity of InN: The role of positively charged dislocations. Appl. Phys. Lett. 88, 252109, 2006.

CHAPTER 6

Conclusions

6.1 Summary of the results

The performance potential of HEMTs based on AlN/GaN/AlN double heterostructures with a very thin total epilayer thickness of ~0.5 µm, on a highly lattice mismatched insulating substrate, was systematically investigated. AlN/GaN HEMT structures, consisting of [300 nm GaN/ 200 nm AlN] buffer layer were grown heteroepitaxially on insulating Al_2O_3 (0001) substrates and the effects of the AlN barrier thickness in the range 1.5-4.5 nm, were evaluated. The reduction of AlN barrier thickness increased the HEMT device V_{th}, from -2.7 V for 4.5 nm to the normally off value of +0.2 V for 1.5 nm AlN barrier, while pulsed I–V measurements resulted in the maximum cold pulsed ($[V_{gsQ},V_{dsQ}]=[0,0]$ V) saturation current of 1.4 A/mm for the 3.7 nm AlN thickness for ~1 µm gate length devices. The remarkable agreement of experimental results and theoretical calculations suggested only a minor impact of extended defects, induced by the lattice-mismatched heterointerfaces.

A negligible effect of crystalline defects was also observed from the transient characteristics of the devices by gate and drain lag measurements, performed with a 500 ns pulse-width. The devices exhibited little change of the transconductance (the highest reduction was ~8% for the device with 4.5 nm AlN barrier) and a small positive threshold voltage shift (0.2-0.4 V) due to small trapping under the gate.

The off-state breakdown voltage of 70 V, for gate-drain spacing of ~2 µm, was approximately double the value measured for a single AlN/GaN HEMT structure grown on a thick GaN buffer layer, reflecting the reduction of leakage current flowing through the buffer when the thin AlN/GaN/AlN double heterostructure is used.

In situ MBE SiN_x cap was employed as a passivation layer and gate dielectric in thin AlN/GaN/AlN HEMT heterostructures, and resulted in a significant increase of the 2DEG density. However, the fabricated devices exhibited significant current collapse and high leakage currents implying the presence of high defective states. Further investigation by C-V measurements proved

that very high interface trap densities exist at the SiN_x/GaN interface and/or in the SiN_x bulk, suggesting that further optimization of the SiN_x/GaN interface quality is needed.

In the second part of this research work, critical aspects of InN channel field-effect transistors were investigated. We studied the formation of InN MIS capacitors and MISFETs by in-situ deposition of SiN_x dielectric on ultrathin 2 nm InN layers grown on GaN-on sapphire substrates and the operation of InN MISFETs was demonstrated. This evaluation was further extended and the effect of InN channel thickness, in the range of 4-10 nm was studied. The maximum drain–source current was increased by increasing the InN thickness although the channel could not fully pinch-off. According to the I-V analysis of the MIS capacitors, the electrical conduction of SiN_x was dominated by hopping between localized states under low electric fields and field emission tunneling at high fields, with an extracted trap barrier height in the range of 1.1–1.3 eV for all the structures.

6.2 Future work

The results obtained in this work pointed out the great potentials of AlN barrier HEMT and InN-channel HFET transistors.

However, there are many issues that burden AlN-barrier GaN HEMT devices from exploiting their theoretical capabilities. Ohmic contact resistances between 0.3 – 2.0 Ω mm, measured in this research project in AlN/GaN heterostructures, are quite high and the formation of low resistance ohmic contacts remains difficult. As shown in Chapter 4, contact resistance is an important factor in decreasing transconductance and device performance. Recently, researchers at the Cornell university exhibited low contact resistance of ~0.1 Ω mm to AlN/GaN heterostructures by the n^+ GaN MBE regrowth process [1]. This technique may be one of the best options for low contact resistance but increases processing complexity. Although the use of Si ion implantation for nonalloyed contacts to AlGaN/GaN HEMT has been reported [2], implantation and n^+ capping layers are approaches which have yet to be explored and may have the potential to reduce ohmic contact resistance for the AlN/GaN system.

AlN/GaN HEMTs with an AlN barrier layer, of only a few nm, suffer from large gate leakage currents and several dielectrics such as Al_2O_3 [3, 4], SiN_x [5], HfO_2 [6] and Ta_2O_5 [7] have been explored as gate insulators. However, these dielectrics are deposited ex situ, which may cause

additional growth and process-related defects on the devices [8]. Limited work has been reported using in situ SiN_x on the AlN/GaN structure as a gate dielectric and only recently, during this PhD project, a group from Hong Kong University of Science and Technology studied extensively the AlN/GaN system using in-situ SiN_x grown by MOCVD [8-11]. In this thesis, the first experiments exploring the potential of in situ SiN_x deposition on AlN/GaN HEMT structures, at the end of their growth in a PAMBE reactor, were carried out. There are many potential advantages of depositing the SiN_x gate dielectric with MBE instead of conventional PECVD, such as the reproducible control of thickness at the single nanometer scale, uniform and continuous layer formation, limited plasma damage, hydrogen-free SiN_x layers, and the deposition immediately after heterostructure growth [12-14]. NH_3 and SiH_4 or other metal–organic precursors which are commonly used in other deposition techniques including MOCVD and ALD, similarly to PECVD, may introduce hydrogen or other contaminants into the layers. [12-14].

Premature breakdown is another important issue hampering AlN/GaN HEMT power performance to reach its limits. Y. Tang et al recently exhibited deeply-scaled devices with maximum drain currents > 3 A/mm and impressive high f_t of 454 GHz and simultaneous f_{max} of 444 GHz on AlN/GaN/AlGaN HEMTs [15]. However, this achievement, which have been primarily accomplished through both vertical and lateral dimension scaling generally suffered from very low breakdown voltages of < 10 V [15,16]. Field shaping using a proper field plate design may lead to improvement of power performance by increasing off-state breakdown voltage and this possibility has not been studied yet in AlN/GaN HEMTs.

Regarding InN, although it has been predicted to exhibit unique transport properties making it the best candidate for high frequency/high speed electronic devices reaching the terahertz region, the development of InN channel transistors must deal first with great impediments. First experimental attempts on InN-channel transistors were reported either with a 26 nm thick InN grown on AlN [17] (resulting low μ~209 cm^2/Vs, I_{ds} ~530 mA/mm and no current saturation) or 2–5 nm thick InN grown on zirconia substrates exhibiting very low transistor current densities [18]. In this work, for the first time, the operation of 2 nm ultrathin InN channel transistors grown on GaN buffer layer was demonstrated with maximum I_{ds} of ~60 mA/mm, while I_{ds} ~1.2 A/mm has been reached when a 10 nm InN channel was employed; this is the highest value so far achieved

for InN-based transistors. Obviously, the progress in InN device technology is still at the initial stage and further research is required.

As far it concerns channel transport and pinch-off properties, strained InN channels grown on low lattice-mismatch InN-rich InAlN alloy buffer layers could be used to overcome the high density of dislocations [19], originating by misfit relaxation at the InN/GaN or InN/AlN interface. The capability to grow by PAMBE InAlN alloys spanning the entire composition range have been demonstrated [20] but further work is needed to optimize the growth and properties of InN-rich InAlN alloys.

This PhD research project suggests the use of ultrathin InN layers with high crystal quality, as a straightforward approach for reducing sheet electron concentration. The proper selection of the dielectric and deposition method are also essential for the development of InN channel FETs for ultra-high frequency applications.

6.3 Chapter 6 references

[1] M. Qi, G. Li, S. Ganguly, P. Zhao, X. Yan, J. Verma, B. Song, M. Zhu, K. Nomoto, H. (Grace) Xing and D. Jena. Strained GaN quantum-well FETs on single crystal bulk AlN substrates. Appl. Phys. Lett. 110, 063501, 2017.

[2] F. Recht, L. McCarthy, S. Rajan, A. Chakraborty, C. Poblenz, A. Corrion, J. S. Speck, and U. K. Mishra. Nonalloyed ohmic contacts in AlGaN/GaN HEMTs by ion implantation with reduced activation annealing temperature. IEEE Electron Device Lett. 27, 205, 2006.

[3] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. G. Xing. AlN/GaN insulated-gate HEMTs with 2.3 A/mm output current and 480 mS/mm transconductance. IEEE Electron Device Lett. 29, 661, 2008.

[4] S. Taking, D. MacFarlane, and E. Wasige. AlN/GaN MOS-HEMTs with thermally grown Al_2O_3 passivation. IEEE Electron Device Lett. 32, 1418, 2011.

[5] M. Higashiwaki, T. Mimura. AlN/GaN insulated-gate HFETs using Cat-CVD SiN. IEEE Electron Device Lett. 27, 719, 2006.

[6] D.A. Deen, S.C. Binari, D.F. Storm, D.S. Katzer, J.A. Roussos, J.C. Hackley and T. Gougousi. AlN/GaN insulated gate HEMTs with HfO_2 gate dielectric. Elec. Lett. 45, 8, 2009.

[7] D. A. Deen, D. F. Storm, R. Bass, D. J. Meyer, D. S. Katzer, S. C. Binari, J. W. Lacis, and T. Gougousi. Atomic layer deposited Ta_2O_5 gate insulation for enhancing breakdown voltage of AlN/GaN high electron mobility transistors, Appl. Phys. Lett. 98, 023506, 2011.

[8] X. Lu, J. Ma, Z. Liu, H. Jiang, T. Huang, and K. M. Lau. In situ SiN_x gate dielectric by MOCVD for low-leakage-current ultra-thin-barrier AlN/GaN MISHEMTs on Si. Phys. Status Solidi A, 775, 2014.

[9] X. Lu, J. Ma, H. Jiang, C. Liu, P. Xu, and K. M. Lau. Fabrication and characterization of gate-last self-aligned AlN/GaN MISHEMTs with in situ SiN_x gate dielectric. IEEE Trans. Electron Devices 62, 1862, 2015.

[10] X. Lu, J. Ma, H. Jiang, and K. M. Lau. Characterization of in situ SiN_x thin film grown on AlN/GaN heterostructure by metal-organic chemical vapor deposition. Appl. Phys. Lett. 104, 032903, 2014.

[11] X. Lu, J. Ma, H. Jiang, C. Liu, and K. M. Lau. Low trap states in in situ SiNx/AlN/GaN metal-insulator-semiconductor structures grown by metal-organic chemical vapor deposition. Appl. Phys. Lett. 105, 102911, 2014.

[12] B.P. Downey, D.J. Meyer, D.S. Katzer, T.M. Marron, M. Pan c, X. Gao. Effect of SiN_x gate insulator thickness on electrical properties of $SiN_x/In_{0.17}Al_{0.83}N$/AlN/GaN MIS–HEMTs. Solid-State Electron. 106, 2015, 12–17.

[13] D. S. Katzer, D. J. Meyer, D. F. Storm, J. A. Mittereder, V. M. Bermudez, S. F. Cheng, G. G. Jernigan, and S. C. Binari. Ultra-high vacuum deposition and characterization of silicon nitride thin films. J. Vac. Sci. Technol. B, 30, 02B129, 2012.

[14] B. Heying, I. Smorchkova, R. Coffie, V. Gambin, Y. Chen, W. Sutton, T. Lam, M.S. Kahr, K.S. Sikorski, and M. Wojtowicz. In situ SiN passivation of AlGaN/GaN HEMTs by molecular beam epitaxy. Electron Lett, 43, 779, 2007.

[15] Y. Tang, K. Shinohara, D. Regan, A. Corrion, D. Brown, J. Wong, A. Schmitz, H. Fung, S. Kim, and M. Micovic. Ultrahigh-speed GaN high-electron-mobility transistors with f_T/f_{max} of 454/444 GHz. IEEE Electron Device Lett. 36, 549, 2015.

[16] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos, and M. Micovic. Scaling of GaN HEMTs and schottky diodes for submillimeter-wave MMIC applications. IEEE Trans. Electron Devices 60, 2982, 2013.

[17] Y.-S. Lin, S.-H. Koa, C.-Y. Chan, S. S. H. Hsu, H.-M. Lee, and S. Gwo. High current density InN/AlN heterojunction field-effect transistor with a SiN^x gate dielectric layer Appl. Phys. Lett. 90, 142111, 2007.

[18] M. Oseki, K. Okubo, A. Kobayashi, J. Ohta, and H. Fujioka. Field-effect transistors based on cubic indium nitride Sci. Rep. 4, 3951, 2014.

[19] J. Kuzmik and A. Georgakilas. Proposal of high-electron mobility transistors with strained InN channel. IEEE Trans. Electron Devices 58, 720, 2011.

[20] E. Iliopoulos, A. Adikimenakis, C. Giesen, M. Heuken, and A. Georgakilas. Energy bandgap bowing of InAlN alloys studied by spectroscopic ellipsometry. Appl. Phys. Lett. 92, 191907, 2008.