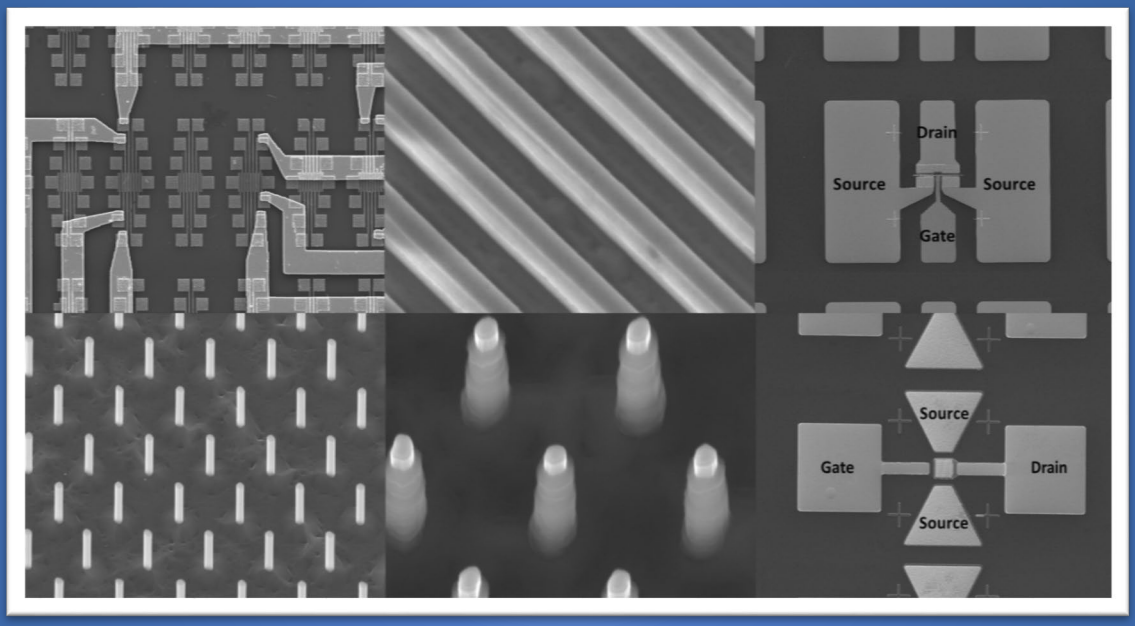
Realization and physical analysis of field-effect transistors based on GaN nanofins and vertical nanowires



Doctoral thesis

by

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Abstract

Semiconductor nanostructures, such as nanowires (NWs) and nanofins, have gained significant interest as promising elemental building blocks in nanoelectronic and nanophotonic applications. Their reduced dimensionality and high aspect ratio could enhance the miniaturization of devices and lead to high device density, decreased power consumption and high operation frequency**.** Among them, nanostructures of gallium nitride (GaN) have attracted much attention for the exploitation of the fundamental advantages of GaN material, such as wide direct band gap, high thermal conductivity and high breakdown voltage. This work has created new knowledge for material and device processing effects on the performance of next-generation GaN-based nanoelectronic devices, with focus on field-effect transistors (FETs) based on GaN nanofins (FinFETs) and vertical nanowires (V-NW FETs).

Initially, the experimental bottom-up processes for formation of GaN-based NWs and nanofins by Plasma Assisted Molecular Beam Epitaxy (PAMBE) are briefly discussed. The spontaneous growth of GaN NWs by PAMBE resulted to large deviations in shape and size of GaN NWs, critical parameters for the assembly of V-NW FETs, where an accurate control of the position and dimensions of NWs is necessary. Therefore, selective area growth (SAG) was studied for aligning GaN NWs on different substrates without using metal catalysts, which is accomplished by epitaxial growth on a substrate coated with a nanopatterned mask. Two different substrates were used for the SAG of GaN NWs. The growth of GaN NWs on Si (111) substrates patterned with a thermally grown SiO_2 mask revealed the difficulty of filling all the Si mask windows with GaN NWs, while the grown GaN NWs exhibited larger diameter than the mask window and, in some cases, inclined direction. Nanoribbons (stripes) were also patterned on the SiO_2/Si substrates, resulted to nucleation and growth of multiple GaN NWs inside each nanoribbon, instead of a compact fin material. The use of SiO_2/GaN/Si substrates for the SAG of GaN NWs was also investigated. In this case, the deposition of GaN material was enhanced by the reduction of window pitch, with the pitch of 250 nm exhibiting single NW formation that follows the diameter of the mask window. However, photoluminescence (PL) experiments may suggest the formation of crystal defects in these compact NWs, possibly due to coalescence of multiple narrow NWs.

The electrical transport properties of GaN NWs grown spontaneously on Si (111) and nanopatterned SiO_2/Si (111) substrates were determined, in order to evaluate the unintentional doping, and understand the surface states induced band-bending and the size effects on the conductivity of bottom-up grown GaN NWs. Conventional nanofabrication techniques were used to define multiple ohmic contacts to individual GaN NWs dispersed on SiO_2/Si (111) substrates, with NW diameters ranging from 30 to 140 nm and lengths ranging from 500 to 1900 nm. Current-Voltage (I-V) measurements indicated that the apparent resistivity values of GaN NWs depended on their diameter, due to carrier depletion induced by Fermi level pinning at the lateral NW surfaces. Assuming that $(E_C-E_F)_S$= 0.55 eV at the GaN NW lateral surface, a critical GaN NW

diameter of ~87 nm for full depletion (punch through) of the GaN NW was calculated, in agreement with the experimental observations. The actual resistivity of the GaN NW crystal was then calculated by subtracting the value of the critical GaN NW diameter from the nominal one, which resulted to resistivity values in the range of 0.01 to 0.03 Ωcm. The estimated average doping concentration was 5.2×10^{17} cm^{-3}.

The n-type behavior of GaN NWs was exploited in the first time, to our knowledge, fabrication of vertical p-Si/n-GaN NW heterojunction diodes. The diodes exhibited a clear rectifying behavior, although a non-optimized fabrication process was used, which is promising for future nanophotonic and nanoelectronic device applications (e.g. nanowire heterojunction solar cells).

The difficulties to develop a well-controlled SAG process for GaN NWs and nanofins, within a reasonable time frame, shifted our research interest to a top-down process for their formation from GaN-based films, using three processing steps: nanopatterning by electron-beam lithography (e-beam), reactive-ion etching (RIE) and anisotropic wet-chemical etching, based on a Tetramethylammonium hydroxide (TMAH) solution. The TMAH treatment removes the plasma damage and smoothens the lateral surface of the RIE-formed nanostructures, resulting to very steep and uniform GaN-based NWs and nanofins.

The research on FinFETs was focused on the exploitation of the two-dimensional electron gas (2DEG) channel of an AlN/GaN/AlN double barrier heterostructure, which has been proposed and analyzed previously by the lab, for planar High Electron Mobility Transistors (HEMTs). Transistors with metal-oxide-semiconductor (MOS) tri-gate around a fin-shaped channel (MOS-FinHEMTs) were investigated by combining device simulations and experimental device fabrication and characterization. A top-down process was used for the formation of AlN/GaN/AlN nanofins. Single-fin MOS-FinHEMT devices were fabricated for the first time, with fin width (W_{fin}) of 200, 350, 500 and 650 nm. Multi-fin MOS-FinHEMT devices, with channel consisting of 70 fins with W_{fin} = 200 nm, and conventional planar gate MOS-HEMTs, were also fabricated for comparison. The dependence of the threshold voltage (V_{th}) and the maximum drain-source current ($I_{ds,max}$) on the fin width (W_{fin}), as well as the effects of ohmic contact resistance, gate-drain and source-gate distance and of the Al_2O_3 gate dielectric thickness (t_{ox}), were determined. Fabricated single-fin MOS-FinHEMT devices, with t_{ox}= 20 nm, exhibited a positive shift of V_{th}, in comparison to a reference planar-gate device, ranging from +0.8 V for W_{fin} = 650 nm to +3.4 V for W_{fin} = 200 nm, due to lateral depletion of the channel by the gate contacts on the fin sidewalls. Device simulations were used to reproduce the experimental V_{th} values and also to predict the V_{th} of devices with narrower fins, down to W_{fin}=10 nm. The boundary for normally-off operation (V_{th}=0 V) was determined for W_{fin} = 17 nm that may increase up to 31 nm, if the tensile strain of the top AlN barrier in the fin nanostructure is elastically relaxed. A reduction of maximum drain-source current per top gate width ($I_{ds,max}/W_g$), with decreasing W_{fin} in the range of 200-650 nm, may result from increased ohmic contact resistance. However, for narrower fins, $I_{ds,max}/W_g$ was predicted to decrease significantly with decreasing W_{fin}, due to the lateral electron depletion in the

nanofins. The $I_{ds,max}/W_g$ will also decrease with increasing distance between the source, gate and drain contacts for any W_{fin}. The V_{th} and $I_{ds,max}/W_g$ values were also calculated for Al_2O_3 thickness in the range of 5 to 40 nm.

Finally, GaN V-NW FETs with a Schottky barrier gate (V-NW MESFETs) were fabricated for the first time, using a top-down process to form GaN NWs from a PAMBE GaN epilayer on sapphire (0001) substrate. A nanofabrication process with comprehensive design of all processing steps was developed and validated with the demonstration of GaN V-NW MESFETs, consisting of an array of 900 (30x30) GaN NWs with a diameter of 100 nm and all-around gate length of 250 nm. DC I-V characteristics exhibited normally-off operation and threshold voltage of +0.4 V, due to electron depletion region from the all-around Schottky barrier. The I-V characteristics were dominated by the high source and drain access resistances resulting from electron depletion due to Fermi level pinning by surface states at the lateral GaN NW sides. A maximum drain-source current density ($J_{ds,max}$) of 330 A/cm^2 and maximum transconductance ($g_{m,max}$) of 285 S/cm^2 were determined from I-V measurements. Optimization of the doping profile in the GaN epilayers, surface passivation and a self-aligned gate process technology could address the high access resistance issue.

Overall, the research carried out within this thesis, on both GaN-based FinHEMTs and V-NW MESFETs has established critical scientific understanding and technological know-how for achieving further progress in the future. Essential insight was gained for the performance capabilities of these devices, as well as the influence of nanoelectronic device design, nanofabrication processes and material parameters.

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Abbreviations

ALD	Atomic layer deposition
Al	Aluminum
AlGaN	Aluminum gallium nitride
AlN	Aluminum nitride
Al_2O_3	Aluminum oxide
APCVD	Atmospheric pressure chemical vapor deposition
Au	Gold
BHF	Buffered hydrofluoric acid
Cr	Chromium
CVD	Chemical vapor deposition
d_{crit}	Critical diameter
d_{eff}	Effective diameter
DI	Deionized
E_g	Energy band-gap
e-beam	Electron beam
EBL	Electron beam lithography
FET	Field-effect transistor
FIB	Focused-ion beam
FinFET	Fin-shaped channel field-effect transistor
FWHM	Full width at half maximum
g_m	Transconductance
GAA	Gate all-around
GaN	Gallium nitride
Ge	Germanium
$g_{m,max}$	Maximum transconductance
HEMT	High electron mobility transistor
HRTEM	High resolution transmission electron microscopy
HVPE	Hybrid vapor phase epitaxy
I_{ds}	Drain to source current
$I_{ds,max}$	Maximum drain-source current
I_{ds}-V_{ds}	DC output characteristics
I_{ds}-V_{gs}	DC transfer characteristics
I-V	Current-Voltage
InAlN	Indium aluminum nitride
InN	Indium nitride
IR	Infrared
IRDS	International roadmap for devices and systems
J-V	Current density-Voltage
KOH	Potassium hydroxide
L_g	Gate length
L_{gd}	Gate to drain distance
L_{sd}	Source to drain distance
L_{sg}	Source to gate distance
LED	Light emitting diode

LGAA	Lateral gate-all-around
MESFET	Metal semiconductor field-effect transistor
MIS	Metal-insulator-semiconductor
ML	Monolayer
MOS	Metal-oxide-semiconductor
MOSFET	Metal oxide semiconductor field-effect transistor
MOVPE	Metalorganic vapor phase epitaxy
N_A	Acceptor concentration
N_D	Donor concentration
n_s	Sheet electron concentration
Ni	Nickel
NW	Nanowire
PAMBE	Plasma assisted molecular beam epitaxy
P_{PZ}	Piezoelectric polarization
P_{SP}	Spontaneous polarization
P_T	Total polarization
PL	Photoluminescence
PR	Photoresist
PVD	Physical vapor deposition
Q_{if}	Fixed positive charge
$q\Phi_B$	Schottky barrier height
R_C	Contact resistance
R_{crit}	Critical radius
R_{ext}	Extension resistance
$R_{m/s}$	Metallization semiconductor resistance
R_{sem}	Semiconductor resistance
R_{sh}	Sheet resistance
R_{sp}	Spreading resistance
R_T	Total resistance
RF	Radio frequency
RIE	Reactive ion etching
RTA	Rapid thermal annealing
SAG	Selective area growth
SCL	Space charge limited
SEM	Scanning electron microscope
Si	Silicon
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
t_{ox}	Oxide thickness
TD	Threading dislocation
Ti	Titanium
TLM	Transmission line model
TMAH	Tetramethylammonium hydroxide
UV	Ultraviolet
u-GaN	undoped GaN
V_{bi}	Built-in potential
V_{ds}	Drain to source voltage
V_{gs}	Gate to source voltage

V_{th}	Threshold voltage
V-NW	Vertical nanowire
VGAA	Vertical gate all-around
W_{dep}	Depletion region width
W_{fin}	Fin width
W_g	Gate width
X_s	Electron affinity
ZnO	Zinc oxide
ΔE_C	Conduction band offset
ΔE_V	Valence band offset
ε_r	Dielectric constant or permittivity
μ	mobility
ρ_c	Specific contact resistivity
σ_{int}	Interface sheet charge
Φ_M	Metal work function
2-D	Two-Dimensional
2DEG	Two dimensional electron gas
3-D	Three-Dimensional

Chapter 1

Introduction

Gallium Nitride (GaN) and related III-Nitride semiconductors exhibit fundamental advantages, such as wide direct band gap, excellent electron transport properties, high breakdown voltage and high thermal conductivity [1–2]. The large spontaneous and piezoelectric polarization effects in III-Nitrides [1–2] can be exploited for the formation of a high density two-dimensional electron gas (2DEG) channel at an $Al_{1-x}Ga_xN/GaN$ [3] or $In_{1-x}Al_xN/GaN$ [4] heterointerface. In addition, GaN is a promising candidate to replace silicon (Si) for next-generation n-channel transistors of digital integrated circuits [5]. Device simulations of Chowdhury N. et al. [5] predict that n-type GaN nanowire (NW) field-effect transistors (FETs) with gate length of 5 nm would outperform Si and other semiconductors, due to the relatively higher electron effective mass and lower permittivity of GaN. These devices will operate at fully ballistic transport regime [5]. Chowdhury N. et al. [5] determined that if the transistors are tuned for the same off current then GaN will provide the lowest threshold voltage (V_{th}) and thus highest on current for the same supply voltage (V_{CC}). This is attributed to reduction of the source to drain direct tunneling by the relatively higher effective mass and better short-channel characteristics due to the lower permittivity of GaN [5]. It is also worth mentioning that the 2014 Nobel Prize in physics was awarded jointly to Isamu Akasaki, Hiroshi Amano and Shuji Nakamura, acknowledging their work on III-Nitrides for efficient blue Light Emitting Diodes (LEDs) [6].

1.1 The roadmap to GaN NWs and nanofins

The earliest mention of synthesis of GaN is traced back to 1932 by Johnson W. C. et al. [7], through a direct reaction between gallium and ammonia. Maruska H. P. and Tietjen J. J. [8] reported in 1969 the first epitaxial growth of GaN film on sapphire substrate by Hybrid Vapor Phase Epitaxy (HVPE). Poor crystal quality and high background electron concentration were observed. The first high-quality Metalorganic Vapor Phase Epitaxial (MOVPE) growth of GaN film on sapphire substrate, was reported by Amano H. et al. [9] in 1985, using an AlN buffer layer. This group also reported [10] in 1989, the first p-type doped GaN film by MOVPE, using Mg for doping and a low-energy electron-beam irradiation (LEEBI) treatment for lowering the resistivity and remarkable enhancement of the Photoluminescence (PL) efficiency [10]. They also used this process to develop a p-n GaN junction LED [10], which enabled the fabrication of Nitride-based optoelectronic devices [11].

Since the late 1990s, the pioneering work of the groups of Kishino K. [12] and Calleja E. [13] triggered the scientific interest to self-assembled (spontaneously) grown GaN nanowires (NWs). Spontaneous growth of GaN NWs [12–13] is a random process with

large deviations in shape and size of NWs, which was the main drawback for most device applications (e.g. vertical NW FETs). Therefore, a position-controlled growth was needed. The first selective area growth (SAG) of arbitrary shape GaN structures with Molecular Beam Epitaxy (MBE), was reported in 2000 by Gupta V.K. et al. [14], using a SiO_2 mask deposited on a GaN film, previously grown on a sapphire substrate. Two years later, Kawasaki K. et al. [15] used this technology for the formation of vertical SAG GaN NWs by MBE using a SiO_2 mask with circular openings. It took few years for new publications of SAG of NWs [16] and for the exploitation of this technique in the formation of GaN nanofins [17]. Kishino K. et al. [17] used a Ti mask that fully covered a Si substrate, while nanostripe window openings were patterned on the metallic mask with conventional nanofabrication techniques.

Nowadays, GaN NWs and nanofins are promising elemental building blocks in nanoelectronic and nanophotonic applications [18–21], due to their reduced dimensionality and high aspect ratio that could enhance the miniaturization of devices and lead to high device density, decreased power consumption and high operation frequency [18–21]. SAG technology [14–17, 22, 23] is increasingly employed to combine the high crystal quality of spontaneously grown GaN NWs with precise dimensioning and positioning, critical parameters for the fabrication of devices (e.g. vertical GaN NW transistors). However, the understanding of growth mechanisms and optimization of the patterned mask in SAG GaN technology is still under discussion in the literature [22–23]. Dielectric or metallic masks [14–17, 22, 23] are used and studied in order to eliminate the nucleation on the mask outside of the patterned window areas, while the influence of unmasked growth substrate is also investigated, with bare Si and GaN pseudosubstrates to be widely used [14–17, 22, 23]. In contrast to the case of SAG of GaN NWs, only few works for SAG of GaN nanofins are reported [17, 23], indicating that apart from the significant achievements reported in early years, further research efforts are needed.

The complexity of SAG techniques, combined with poor results [22–23], motivated the investigation of top-down approaches in order to improve the material quality of the formed GaN nanostructures [24], which is maybe the main drawback of these techniques. Top-down approaches for the formation of GaN-based NWs and nanofins are based on three processing steps: nanopatterning by electron-beam lithography (e-beam), reactive-ion etching (RIE) and/or anisotropic wet-chemical etching [25–32]. They have been used, since the early 2010s, for the formation of GaN [19, 27, 30] and $Al_{1-x}Ga_xN$/GaN [19, 30–32] nanofins for fabrication of transistor devices (FinFETs). A post RIE wet chemical-etching treatment (TMAH- or KOH-based) is widely used to remove the plasma damage and to smooth the lateral surface of the RIE-formed nanofins [19, 30, 32]. This wet chemical treatment was recently employed by Jo Y.-W. et al. [25] for the formation of top-down GaN NWs and the first demonstration of GaN-based vertical NW FETs [25]. Up to now, there has been a limited amount of experimental work on n-type GaN vertical NW (V-NW) FETs [25–29].

1.2 The roadmap to next generation devices

Moore's law [33] held true for over 50 years as the way to explain ongoing improvements in transistor scaling, associated with doubling the number of transistors every two years in a dense integrated circuit. The prospects for low power FETs for logic in the next 20 years, are described in the 2018 "International Roadmap for Devices and Systems (IRDS)" [34–35] and predict that Moore's law will keep alive.

According to IRDS [34–35] the scaling of devices is divided into three time periods. The first generation, the "geometrical scaling" lasted from 1975 to 2002 and includes reduction of the physical dimensions of planar transistors in conjunction with improved performance. The next generation was named "equivalent scaling" started at 2003 and will last up to 2024. The goal in this period is the reduction of horizontal dimensions in conjunction with the use of new materials and physical effects. New vertical structures will replace the planar ones. The future generation was named "3D Power Scaling" by the IRDS to include all the challenges facing the semiconductor and electronics industries in the next 15 years. In this period (2025-2040), vertical device structures will dominate offering heterogeneous integration in conjunction with reduced power consumption. In particular, lateral nanowire FET devices – corresponding to the Lateral Gate-All-Around (LGAA) technology – will be introduced in 2022 and will initially co-exist with the last period of the (Tri-Gate) FinFET technology. Vertical NW GAA (VGAA) technology is expected to start in 2027 and will dominate until 2034 together with 3D integration [34–35].

III-V NWs are anticipated to be used for n-channel MOSFETs from 2022, together with strained Si and Ge [34–35]. The use of III-V channels is considered necessary to deliver high performance logic chips with low power consumption [36]. However, the need for a careful holistic optimization is also anticipated, taking into account both the channel material parameters and the parameters and architecture of devices [34–35].

Up to date, FinFETs and vertical NW GAA (VGAA) technology have already gained significant attention, in consequence with the IRDS roadmap predictions, due to the enhanced electrostatic control of the gate on the channel that results to significant improvement of leakage current and current on/off ratio, in comparison to planar gate devices [25–32]. Intel and IBM lead the way in FinFET technology. Intel has been manufacturing silicon FinFETS in volume since 2011 starting with its 22nm Ivy Bridge and later Haswell micro-architecture processors using a bulk silicon approach [37]. The 14 nm micro-architecture processors became Intel's 2nd generation Si FinFET technology [38] with improved performance and reduced leakage power. On the other hand, IBM has taken a more experimental approach using silicon-on-insulator (SOI) substrates to simplify the manufacturing process and allow lower voltage operation. The FinFET process technology developed for IBM server processors at the 14-nm node [39] offers deep-trench embedded dynamic random access memory (eDRAM), multiple work-function FinFET devices and a hierarchical 17-level metal back-end of line. In 2015, IBM announced the fabrication of 7-nanometer node FinFETs [40] using silicon-germanium channels.

Beyond tri-gate devices, GAA technologies are promising candidates to extend the gate length and gate pitch scaling beyond what is possible with FinFETs. In 2017, IBM and its research alliance partners GlobalFoundries and Samsung have developed a process to build 5 nanometer (nm) chips [41] using a new gate all- around architecture that employs stacked silicon nanosheets, providing for better leakage control at smaller scales. At 2018 IEEE International Electron Devices Meeting (IEDM), IMEC reported significant progress in process enabling the introduction of GAA transistors with vertically stacked Ge NWs and nanosheets [42]. The VGAA nanowire technology instead of stacked NW technology is another promising way for ongoing device optimization. The earliest mention of Si NW VGAA transistor is traced back to 1988 by the inspiring work of the group of Masuoka F. [43]. This technology could be considered as the ultimate scaling of Si nanoelectronic FETs and further advancement should involve a new channel material. However, it took more than 15 years for new publications of NW VGAA transistors using a Si [44] or ZnO [45] NW channel. The first III-V (InAs) NW VGAA transistor was reported in 2006 [46], while the first demonstration of GaN NW VGAA transistor was reported recently in 2015 [25] by a top-down approach, which combines conventional nanofabrication techniques and wet etching.

The transition from low power (digital) to high power FET devices can be easily achieved by increasing the number of nanofins or lateral/vertical nanowires in FinFETs and nanowire FETs, respectively. Thus, the channel of these devices consisting of parallel connections of several fins or nanowires. Recently, Zhang Y. et al. [47] have demonstrated a GaN-based multi-fin channel FinFET device with breakdown voltage of over 1200 V, extremely high ON current of over 25 kA/cm^2 and low OFF current below 10^{-4} A/cm^2 at 1200 V. Therefore, V-NW transistors and FinFETs are promising nanoelectronic structures for both low power and high power device applications.

1.3 Motivation and overview of this work

At University of Crete, the MIS 377284 project: "Spontaneous growth, properties and devices of III-V semiconductor nanowires" (Nanowire), of the THALES program, was initiated in Fall 2012, to create fundamental understanding and develop a new NW device technology. A very ambitious target of the project was the development of GaN vertical NW FET (V-NW FET) device technology and this has been the core activity of the present PhD thesis. The last 4 years, GaN V-NW FET technology has gained significant research attention for fabrication of next generation devices, in consequence with the IRDS roadmap predictions that V-NW FET technology is expected to follow the FinFET technology and to dominate until 2034 together with 3D integration for fabrication of nanoelectronic structures. Fabrication and physical analysis of horizontal NW devices was also carried out in order to determine and understand the fundamental GaN NW properties. The spontaneously grown n-GaN NWs on p-Si (111) substrates were utilized in fabrication of p-Si/n-GaN NW heterojunction diodes, indicating a promising candidate for integrating GaN NW solar cells and light emission devices on Si substrates. Finally, research on GaN-based FinHEMTs, processed by a double barrier AlN/GaN/AlN

heterostructure, was undertaken as a technologically and scientifically intermediate device structure, bringing the know-how and understanding of planar GaN HEMTs with GaN NW transistors.

The manuscript of this dissertation is subdivided as follows: ***Chapter 2*** briefly covers the essential background on III-Nitride semiconductors. Their fundamental structural properties and the role of polarity/polarization effects in formation of III-Nitride based heterostructures, are discussed. ***Chapter 3*** describes the principal micro- and nanofabrication techniques used in this work, including photolithography, e-beam lithography, reactive ion etching, chemical vapor deposition, atomic layer deposition, plasma ashing, electron beam evaporation, rapid thermal annealing and wet – chemical treatment. ***Chapter 4*** focuses on the basic device operation and electrical DC characteristics of all kinds of devices fabricated in this thesis, including TLMs, p-n diodes, MOSFETs, MESFETs and HEMTs. A conventional planar geometry is assumed. ***Chapter 5*** briefly presents the experimental techniques used in this work for spontaneous growth or top-down formation of GaN-based NWs and nanofins. ***Chapter 6*** focuses on the evaluation and understanding of size effects on the conductivity of bottom-up grown GaN NWs on Si (111) substrates and the fabrication of GaN-based vertical NW diodes grown on p-Si (111) substrates by PAMBE. ***Chapter 7*** demonstrates experimental and modeling insights for scaling the channel width of fin-shaped AlN/GaN/AlN MOS-FinHEMTs. ***Chapter 8*** presents an innovative concept of fabrication of Schottky barrier gate normally-off GaN vertical NW MESFETs by a top-down approach. Comprehensive description of all fabrication steps and the DC characteristics of the fabricated devices, are reported. Finally, ***Chapter 9*** concludes the results obtained in this work and provides an outlook to future research work.

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Chapter 2

Properties of III-Nitride semiconductors

2.1 Structural properties

III-V semiconductors are compound materials containing elements from group III (B, Al, Ga and In) and V (N, P, As, Sb) of the Periodic Table of Elements. III-Nitrides is the family of III-V materials with the group V element being nitrogen (N). They can form binary (i.e. AlN, GaN, InN), ternary (i.e. $In_XGa_{1-X}N$, $In_XAl_{1-X}N$, $Al_XGa_{1-X}N$) and quaternary (i.e. $In_XAl_YGa_{1-X-Y}N$) compounds [1–2]. III-Nitrides exhibit advantageous features for electronic and optoelectronic applications [3–5]. Their direct band gap (E_g) covers an energy range of 0.65 eV (infrared) to 6.2 eV (deep ultraviolet), which contains the whole visible spectrum (photon energy of 1.77 to 3.10 eV). The energy band gap values for AlN, GaN and InN are 6.2 eV [4], 3.4 eV [4] and 0.65 eV [6], respectively. Ternary and quaternary compounds have band gaps among the above values. For ternary III-Nitrides ($A_XB_{1-X}N$) the band gap can be calculated using the following formula [2]:

$$E_g(A_xB_{1-x}N) = x \cdot E_g(AN) + (1 - x) \cdot E_g(BN) - x \cdot (1 - x) \cdot b \qquad (2.1)$$

where b is the bowing coefficient, which corrects the simple linear relation involving the A and B species [7]. For $Al_XGa_{1-X}N$ the bowing parameter takes the value of 1.0 eV as estimated over the entire composition range [7].

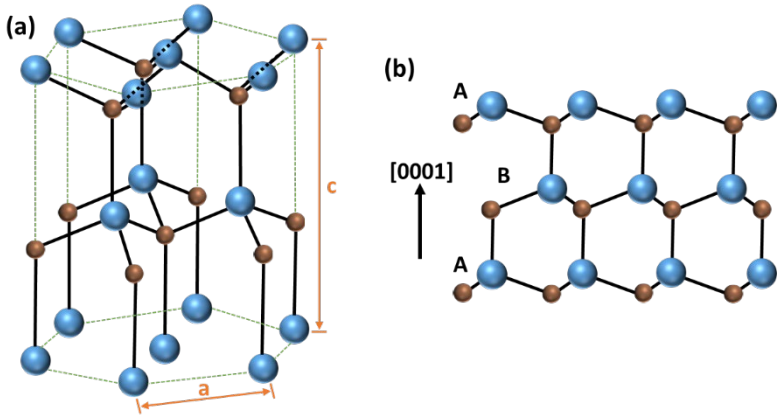

Figure 2.1: *Schematics showing the hexagonal wurtzite crystal structure of III-Nitride semiconductors: (a) unit lattice cell, and (b) stacking sequence of (0001) monolayers.*

The III-Nitride semiconductors commonly can have either a wurtzite (hexagonal) or a zincblende (cubic) crystal structure [2]. The wurtzite crystal structure is the dominant and most thermodynamically stable, whereas the zincblende structure is a metastable phase and can result from growing nitrides on cubic structures [1].

The wurtzite structure has a hexagonal unit cell and is composed of two interpenetrating hexagonal close-packed (hcp) sublattices (Fig. 2.1(a)) of the III and N elements that are shifted the distance of an III-N bond along the [0001] axis (c-axis) [1–2]. Each group III atom is bonded to four N atoms with covalent-ionic bonds and conversely, each N atom is bonded to four group III atoms, as shown in Fig. 2.1(a). The layer stacking along the [0001] direction follows an ABAB sequence (Fig. 2.1(b)) of two monolayers (MLs) A and B (i.e. each ML consists of an atom layer of Ga and N for GaN). The hexagonal structure is described by two lattice constants a and c (Fig. 2.1(a)), where a is the side length of the hexagon on the (0001) basal plane (or c-plane) and c is the height of the hexagonal prism (Fig. 2.1(a)), and by the internal dimensionless parameter u, which is the interatomic distance in the basic unit cell [5]. In an ideal wurtzite crystal structure the two lattice constants would have a ratio c/a = 1.633 [5]. In practice, the wurtzite cell is not perfect and the c/a ratio slightly differs from the ideal case. The lattice parameters at room temperature for GaN, AlN and InN semiconductors, are listed in Table 2.1 [4].

TABLE 2.1. The lattice parameters values of the wurtzite GaN, AlN and InN semiconductors [4].

	a_o (Å)	c_o (Å)	u	c_o/a_o
GaN	3.189	5.185	0.376	1.6259
AlN	3.112	4.982	0.380	1.6010
InN	3.540	5.705	0.377	1.6116

The lattice parameters for ternary and quaternary compounds are calculated according to the Vegard's law and in case of a ternary alloy ($A_XB_{1-X}N$) are given by [2] :

$$a\left(A_XB_{1-X}N\right) = x\cdot a\left(AN\right) + \left(1-x\right)\cdot a\left(BN\right) \quad (2.2)$$

$$c\left(A_XB_{1-X}N\right) = x\cdot c\left(AN\right) + \left(1-x\right)\cdot c\left(BN\right) \quad (2.3)$$

where *AN* and *BN* are the corresponding binary components and x the mole fraction.

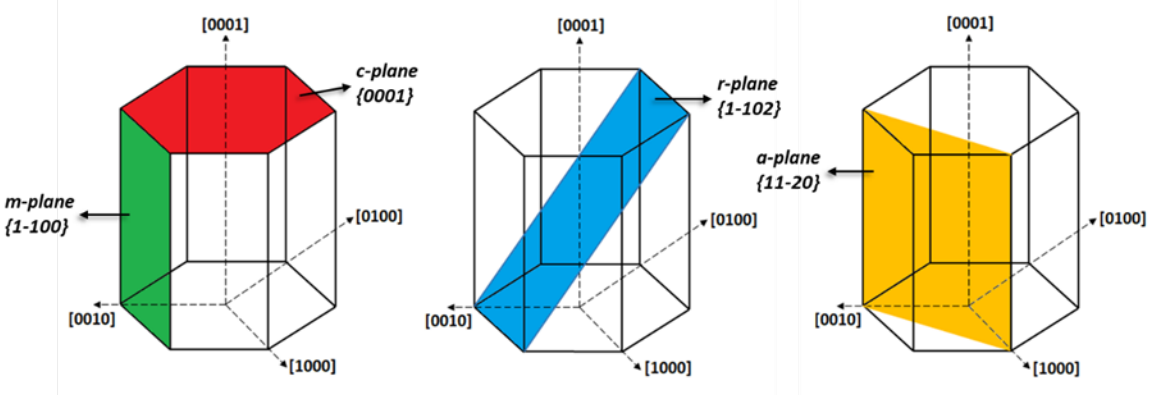

Figure 2.2: *The most important lattice planes in wurtzite crystal structure.*

The main planes of the wurtzite crystal structure as illustrated in Fig. 2.2, are the c-plane or basal-plane, the m-plane, the r-plane and the a-plane, which are indexed as {0001}, {1-100}, {1-102} and {11-20}, respectively, according to the Miller-Bravais notation {hkil} [5].

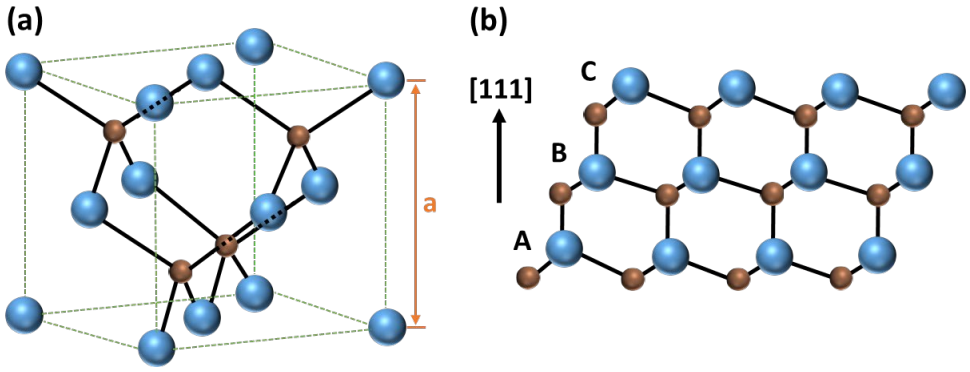

Figure 2.3: *Schematics showing the cubic zincblende: (a) crystal structure and (b) stack sequence, of III-Nitride semiconductors.*

The zincblende structure has a cubic unit cell and is composed of two interpenetrating face-centered cubic (fcc) sublattices of the III and N atoms, shifted by ¼ of the cubic cell's diagonal (Fig. 2.3(a)). Each atom is tetrahedrically coordinated with four atoms of other type, and vice versa. In zincblende structures, there is a 60° rotation along the [111] direction that causes an ABCABC sequence (Fig. 2.3(b)). Hence, the hexagonal planes along the [111] direction for the zincblende structure and along the [0001] direction for the wurtzite structure are rotated 60° with respect to each other. The cubic structure is described by a lattice parameter (a), which is the cell side length (Fig. 2.3(a)). The lattice parameters at room temperature for zincblende GaN, AlN and InN are 4.49, 4.37 and 4.98 Å, respectively [8].

2.2 Polarity and polarization effects

Wurtzite and zincblende crystal structures are both noncentrosymmetrical with polar axes [9]. Hence, for wurtzite Nitride structures the two opposite directions ([0001] and [000-1]) parallel to c-axis are not equivalent. This inherent property is called polarity [9]. The [0001] direction, the positive direction of c-axis, conventionally defined as the vector going from the metallic III-atom (anion) towards the N-atom (cation). The [000-1] direction is going from the N-atom towards the III-atom. The growth direction defines the polarity of a thin film with the wurtzite structure, which is Metal III-polar or III-face (Fig. 2.4(a)) and N-polar or N-face (Fig. 2.4(b)) for epitaxial growth towards the [0001] and [000-1] direction, respectively [9].

The properties of epitaxial III-Nitride semiconductor material are affected by its polarity. Reports have revealed significant differences in electrical, optical, structural and chemical properties by varying the polarity of epitaxial III-Nitride layers [10–12]. A

comparison of epitaxial grown GaN films with Ga- and N-face polarity resulted to reduced Schottky barrier [10], higher PL efficiency [11] and rougher surface morphology [11] for the N-face GaN films compared to the Ga-face ones. Moreover, an aqueous solution of Potassium Hydroxide (KOH) etches only the N-face GaN films, while the Ga-face GaN films remain unperturbed [12]. The deposition method, the substrate treatments, the nucleation conditions and layers, and the choice of substrate are critical parameters as they can vary the polarity of III-Nitride thin films and surfaces [13–16].

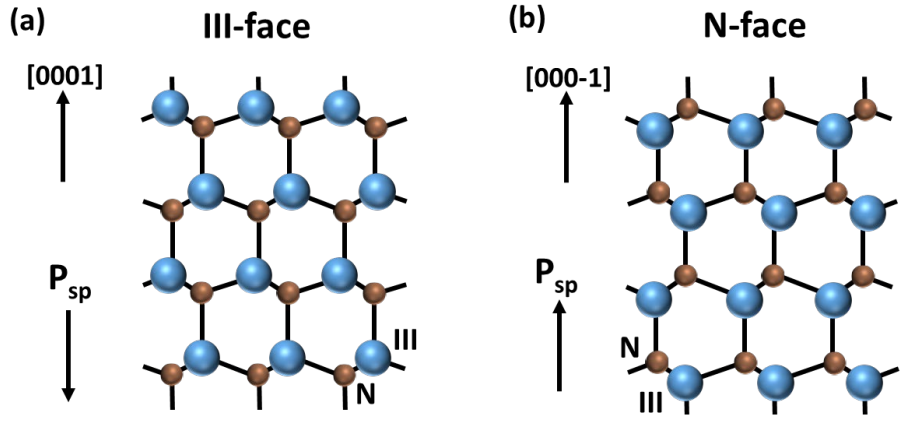

Figure 2.4: *Schematics showing the (a) III-face and (b) N-face directions in the III-N wurtzite cell. The spontaneous polarization P_{sp} vector is shown for both cases.*

Polarization in wurtzite III-Nitrides is an attractive inherent material property, which can impact the device operation considerably. The total polarization P_T is the sum of the intrinsic spontaneous polarization P_{SP} and the strain induced piezoelectric polarization P_{PZ} [9]:

$$P_T = P_{SP} + P_{PZ} \quad (2.4)$$

The partially ionic nature of the III-N bonds, due to the large difference in electronegativity between the N and group-III (metal) atoms, induces positive and negative charges (dipole moments) along each III-N bond [9]. The lower crystal symmetry of the wurtzite structure compared to the zincblende one and the deviation of the c/a ratio from the ideal value, result to the existence of a spontaneous polarization P_{sp} field along the polar axis, caused by the overall uneven distribution of the dipole moments along the c-axis. This polarization exists under the absence of any external field or internal strain and its positive value direction is along the [000-1] crystal direction, as shown in Fig. 2.4.

The values of P_{SP} for relaxed GaN, AlN and InN are equal to -0.034 C/m^2, -0.090 C/m^2 and -0.040 C/m^2 [17], respectively, when the positive polarization value has been defined along the [0001] direction. The P_{SP} for ternary III-Nitrides can be calculated (in C/m^2) by [9]:

$$P^{SP}_{A_XB_{1-X}N} = xP^{SP}_{AN} + (1-x)P^{SP}_{BN} + bx(1-x) \qquad (2.5)$$

where P^{SP}_{AN} and P^{SP}_{BN} are the spontaneous polarization of the binary components and *b* is a characteristic parameter describing the nonlinearity, with typical values of 0.021 C/m^2, 0.037 C/m^2 and 0.070 C/m^2 [17] for the ternary AlGaN, InGaN and AlInN alloys, respectively.

When biaxial strain is applied to the crystal, an additional polarization is induced, the piezoelectric polarization P_{pz}, which is determined along the c-axis by [9]:

$$P_{PZ} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad (2.6)$$

where a_0 is the equilibrium basal-plane lattice constant, a is the actual (strained) basal-plane lattice constant, e_{31} and e_{33} are the piezoelectric coefficients, and C_{13} and C_{33} are the elastic constants. In wurtzite III-Nitrides the term [e_{31}- e_{33} (C_{13}-C_{33})] of Eq. (2.6) is negative as e_{31} takes always negative values and e_{33}, C_{13} and C_{33} take always positive values. Hence the piezoelectric polarization P_{pz} is negative for tensile ($a > a_0$) strain and positive for compressive ($a < a_0$) strain in a layer.

2.3 III-Nitride based heterostructures

A heterostructure or heterojunction is formed when two different materials are brought in contact, practically by deposition and epitaxial growth methods. In the case of a semiconductor heterostructure/heterojunction the two semiconductor layers usually differ in energy band-gap (E_g) and electron affinity (X_s) [18]. The interface between these two semiconductors is called heterointerface. The deposition/growth of a semiconductor with larger bandgap (e.g. $Al_xGa_{1-x}N$) on a semiconductor with lower bandgap (e.g. GaN) is the basic heterostructure for formation of a High Electron Mobility Transistor (HEMT). For n-channel HEMTs, as shown in Fig. 2.5(a), the semiconductor with the higher conduction band and the semiconductor with the lower conduction band (in an equilibrium band diagram) are called barrier and channel layer, respectively.

The band lineup at the heterointerface induces discontinuities at the conduction and valence band, the conduction band (ΔE_C) and valence band (ΔE_V) offsets, respectively [18]. Figure 2.5(b) illustrates a typical band diagram of an $Al_xGa_{1-x}N$/GaN based heterostructure. The conduction band (ΔE_C) offset and the polarization induced interface sheet charges (σ_{int}) at the $Al_xGa_{1-x}N$/GaN heterointerface result to the formation of a two dimensional electron gas (2DEG) at an approximately triangular potential well (Fig. 2.5(b)). The origin and basic physics of this 2DEG will be discussed below.

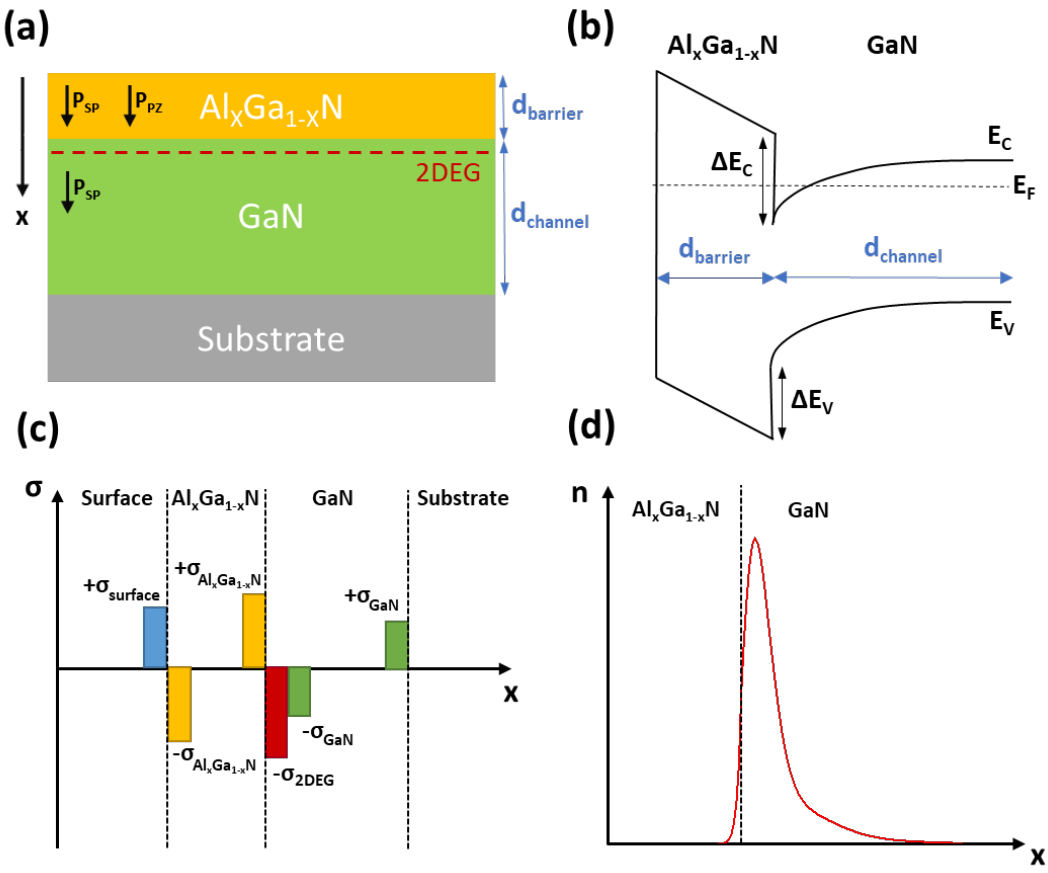

Figure 2.5: *(a) The layers of the heterostructure, the polarization vectors and the interfacial location of 2DEG, (b) Energy band diagram at thermal equilibrium, (c) Distribution of interfacial charges and (d) Profile of electron concentration of the polarization-induced 2DEG, in an $Al_xGa_{1-x}N$/GaN based structure with Ga-face polarity.*

The existence of spontaneous P_{SP} and strain induced piezoelectric polarization P_{PZ} in III-Nitrides were described in Section 2.2. At the interface of two III-Nitride materials with different total polarization P_T (Eq. 2.4), a sheet of static charge (σ_{int}) is formed at the interface, which is calculated in the [0001] direction by [5]:

$$\sigma_{\text{int}} = P_T^{top\ layer} - P_T^{bottom\ layer} \qquad (2.7)$$

If Eq. 2.7 takes a positive value, free electrons compensate this charge and form a 2DEG, when the band structures of these materials at the interface allows also this to happen (Fig. 2.5(b)). For an $Al_xGa_{1-x}N$/GaN heterointerface Eq. 2.7 takes the form:

$$\sigma_{\text{int}} = P_T^{Al_xGa_{1-x}N} - P_T^{GaN} = P_{SP}^{Al_xGa_{1-x}N} + P_{Pz}^{Al_xGa_{1-x}N} - P_{SP}^{GaN} - P_{PZ}^{GaN} \qquad (2.8)$$

where Eq. 2.4 was applied for the total polarization. The P_{PZ}^{GaN} is zero since the channel layer is assumed to be strain-free. The $Al_xGa_{1-x}N$ is grown pseudomorphically on Ga-face polarity GaN under in-plane tensile strain [9]. This results to a piezoelectric polarization in the $Al_xGa_{1-x}N$ layer in addition to the spontaneous polarization, which will have the same sign and will add up (Fig. 2.5(a)). Figure 2.5(c) illustrates the charge distribution profile in an $Al_xGa_{1-x}N$/GaN based structure with Ga-face polarity.

The profile of electron concentration of polarization-induced 2DEG for pseudomorphic Ga-face $Al_xGa_{1-x}N$/GaN and $Al_xIn_{1-x}N$/GaN heterostructures is shown in Fig. 2.5(d). The sheet electron concentration (n_s) of the 2DEG is given approximately by [17]:

$$n_s = \frac{\sigma_{\text{int}}}{q} - \frac{\varepsilon_0 E_F}{q^2}\left(\frac{\varepsilon_{r,barrier}}{d_{barrier}} + \frac{\varepsilon_{r,GaN}}{d_{GaN}}\right) - \frac{\varepsilon_0 \varepsilon_{r,barrier}}{q^2 d_{barrier}}\left(q\Phi_B + \Delta - \Delta E_C\right) \qquad (2.9)$$

where q is the elementary charge, ε_0 is the dielectric constant of the vacuum, $\varepsilon_{r,barrier}$ and $\varepsilon_{r,GaN}$ are the relative dielectric constants of the constituent layers, E_F is the position of the Fermi level with respect to the GaN conduction band at the GaN-substrate interface, $q\Phi_B$ is the Schottky barrier height of the top gate contact (or the surface potential), Δ is the magnitude of the depth of the quantum well in the conduction band below the Fermi level, ΔE_C is the conduction band offset and $d_{barrier}$ and d_{GaN} are the thicknesses of the barrier and the channel layer, respectively. Δ is calculated as a function of n_s by [17]:

$$\Delta = E_0 + \frac{\pi\hbar^2}{m_{GaN}^*} n_s \qquad (2.10)$$

with E_0 the lowest subband level of 2DEG, which is given by [17]:

$$E_0 = \left[\frac{9\pi\hbar q^2}{8\varepsilon_0\sqrt{8m_{GaN}^*}}\frac{n_s}{\varepsilon_{GaN}}\right]^{\frac{2}{3}} \qquad (2.11)$$

where m_{GaN}^* is the electron effective mass of GaN and $\hbar$ is the h-bar Planck's constant.

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Chapter 3

Micro- and nanofabrication techniques

3.1 Introduction

Microfabrication and nanofabrication refer to the design and manufacture of devices with dimensions in the range of micrometers and nanometers, respectively. These techniques are widely developed for applications in semiconductor industry into clean room environments. The fabrication of next generation GaN-based nanoscale devices requires the combination of several micro- and nanofabrication techniques in a complicated process flow [1–2].

This chapter describes the principal micro- and nanofabrication techniques used in this work, including photolithography, e-beam lithography, reactive ion etching, chemical vapor deposition, atomic layer deposition, plasma ashing, electron beam evaporation, rapid thermal annealing and wet – chemical treatment. This research infrastructure is available at the laboratory of the Microelectronics Research Group (MRG) of IESL/FORTH and Physics Department/ University of Crete, at Heraklion, Crete into a Class 1000 clean room facility of the Physics Department.

3.2 Photolithography

Photolithography is a microfabrication technique that is used to transfer desired patterns onto a sample/substrate and enables the fabrication of discrete semiconductor devices, as well as complex integrated circuits. It generally requires an ultraviolet (UV) light source to transfer the geometric pattern from a photomask to a light-sensitive photoresist [3].

The photolithographic process flow steps are shown schematically in Fig. 3.1. In the first step, the sample is subjected to a wet chemical treatment to clean its surface from ions, native oxides and organic contaminants (Fig. 3.1(a)). Afterwards, a light-sensitive photoresist is spun onto the sample surface and baked on a hotplate to drive off excess photoresist solvents (Fig. 3.1(b)). The spinning speed and the photoresist viscosity will determine the final thickness of the photoresist film. All these parameters (spinning speed/time, hotplate temperature/time) are critical for the photolithographical process and are provided in datasheet by the manufacturer of the photoresist [4]. Then, the photomask is aligned with the sample and the photoresist is exposed to UV light under the clear/transparent (glass) regions of the photomask, while under opaque (Cr coated) regions the sample remains unexposed (Fig. 3.1(c)). There are three different exposure techniques: contact, proximity and projection printing [5]. Figure 3.1(c) shows the contact exposure technique used in this work, in which the photoresist is brought into physical contact with the glass photomask during the exposure. In proximity technique,

a small gap is maintained between the sample and the photomask, while in projection technique there is a larger gap as an image of the pattern of the photomask is projected onto the photoresist [5]. UV exposure changes the chemical structure of the exposed photoresist layer depending on the type of photoresist: positive or negative. In positive photoresists, UV-exposed regions break down and become soluble in a subsequent development stage, while in negative photoresists exposed areas become crosslinked/polymerized and remain intact after a developing solution (Fig. 3.1(d)). Negative resists require an additional bake before the pattern's development stage [4].

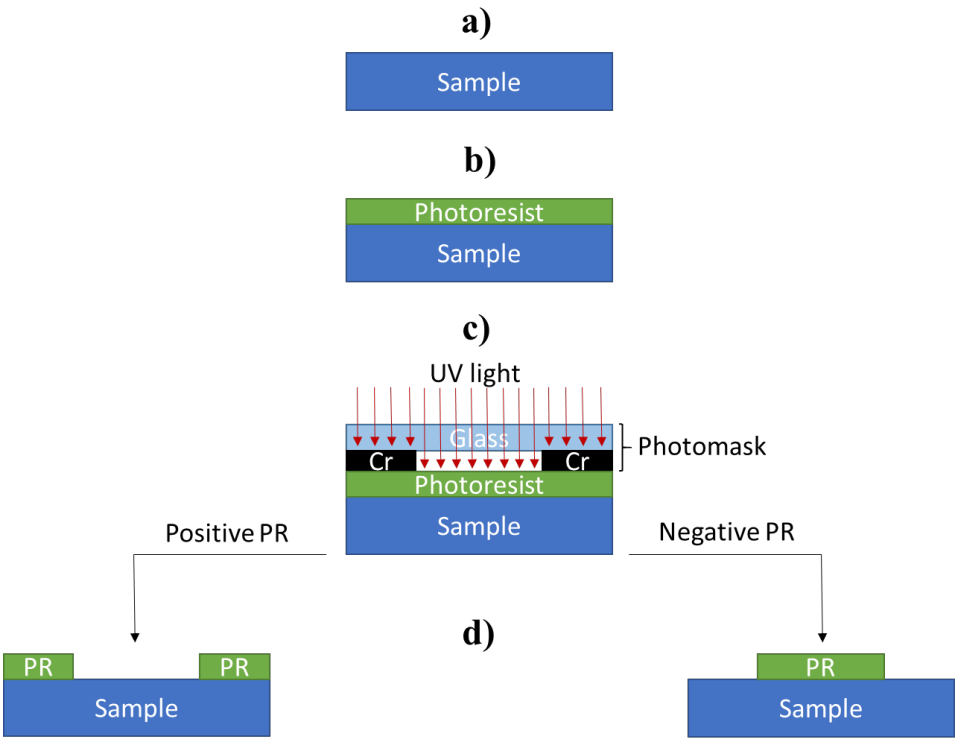

Figure 3.1: *Schematic drawing of the photolithographic steps using a positive or negative photoresist (PR).*

3.3 Electron beam lithography

Electron beam lithography (EBL) is a powerful nanolithography technique that uses a focused electron beam (e-beam) to write patterns instead of the electromagnetic radiation used in the case of conventional photolithography technique. The EBL working principle is very similar to photolithography and is shown schematically in Fig. 3.2. In the first step, the sample is cleaned by a wet chemical treatment to remove surface ions, native oxides and organic contaminants (Fig. 3.2(a)). Afterwards, an electron beam resist is spin-coated over the surface of the sample and baked on a hotplate (Fig. 3.2(b)) to remove its solvents. Then, the highly focused e-beam is moving over the sample to write out a pattern, designed with suitable CAD tools, without the need of photomask (Fig. 3.2(c)). The e-beam changes the solubility of the resist and enables the selective removal

of either the exposed (positive resist) or non-exposed (negative resist) regions of the resist in the pattern's development stage (Fig. 3.2(d)).

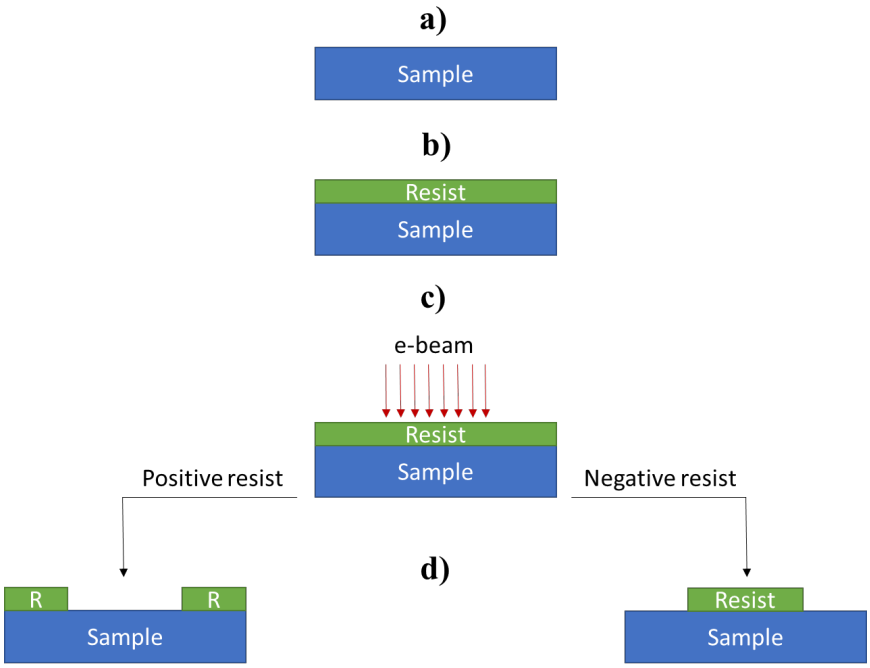

Figure 3.2: *Schematic drawing of the e-beam lithography steps using a positive or negative resist.*

The main advantage of EBL over photolithography is the higher resolution because of the shorter wavelength of electrons compared to photons. As the resolution is not limited by the diffraction effect, state of the art EBL systems can achieve resolutions of few nanometers [6]. The absence of photomasks also gives flexibility to draw the desired complex patterns directly on samples by using a CAD software. Another key advantage of EBL is the ability to control energy and e-beam dose during resist exposure. However, EBL has some disadvantages that have to be mentioned. The main drawback is the poor time and cost efficiency of this technique. EBL is slower than the optical lithography and more expensive, as a complex vacuum system is included. Moreover, a limitation in resolution is caused by forward and back-scattering of the e-beam inside the resist and substrate, respectively [6–7].

3.4 Reactive ion etching

Reactive ion etching (RIE) is a plasma dry etching technology used to etch, in the presence of reactive ions, various materials (including semiconductors, dielectrics, metals, polymers and photoresists) from areas identified by a lithography process [8]. A typical parallel plate RIE system consists of two electrode plates (anode and cathode), within a cylindrical vacuum chamber (Fig. 3.3) [8]. Samples are placed on a wafer platter situated on the lower electrode (cathode) of the chamber (Fig. 3.3). Gases are initiated

through the showerhead in the top electrode (anode) and then activated by applying RF power at 13.56 MHZ to the cathode, while the anode is grounded (Fig. 3.3). The oscillating electric field ionizes the gas molecules by stripping them of electrons, creating a plasma [9]. A negative DC bias is induced at the sample substrate by the free electrons, which accelerates the plasma ions towards the sample surface. The ions strike the sample surface vertically, where they react to form volatile species that are removed by the vacuum system and thus enable the etching mechanism.

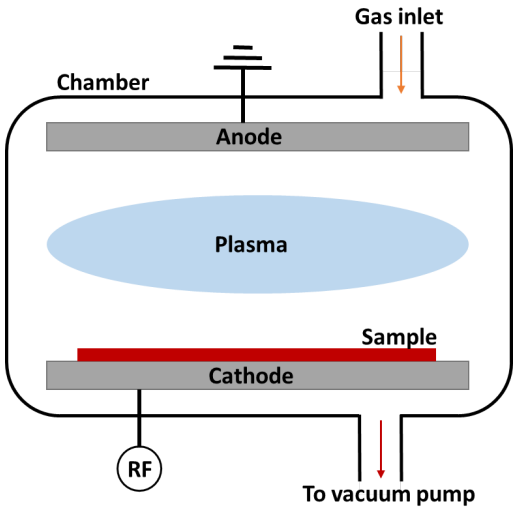

Figure 3.3: *Schematic diagram of a reactive ion etching (RIE) plasma system.*

3.5 Chemical vapor deposition

Chemical vapor deposition (CVD) is a process used to produce a wide range of solid thin-films (dielectrics, metals) and nowadays is commonly used to synthesize high-quality 2-D materials [10–11]. The main idea of this procedure involves the reaction or decomposition of vapor phase volatile precursors over a heated substrate, placed in a reaction chamber. Gas flow through the reaction chamber removes volatile by-products that are frequently produced [10–11].

There are several types of CVD technologies, including plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD) and atmospheric pressure chemical vapor deposition (APCVD), differing generally in the means by which chemical reactions are initiated. The PECVD method, which has been used in this work, utilizes plasma to provide the required energy in order the chemical reactions to take place on the substrate's surface. This has the advantage of lower deposition temperatures, critical in many applications to avoid device damage. Deposition is achieved by introducing the reactant gases into the process chamber [10–11] through the showerhead of a top electrode (Fig. 3.4). An RF potential is applied to the top electrode to generate the plasma, while the bottom parallel electrode is grounded (Fig. 3.4). The capacitive

coupling between the electrodes excites the reactant gases into a plasma, which induces chemical reactions and results in the reaction product being deposited on the substrate. The substrate, which is placed on the grounded electrode, is typically heated to 250 – 350 °C, depending on the specific film requirements.

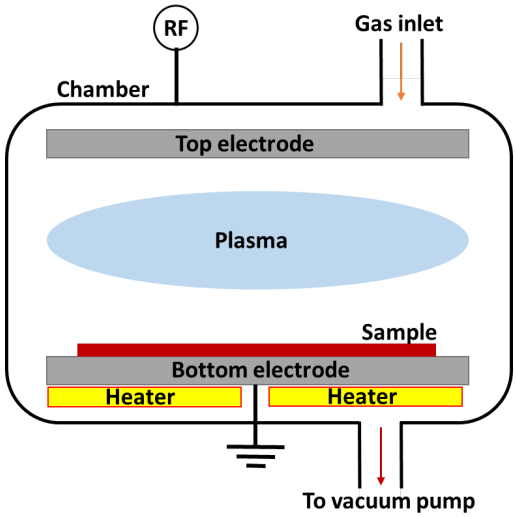

Figure 3.4: *Schematic diagram of a plasma enhanced chemical vapor deposition (PECVD) system.*

3.6 Atomic layer deposition

Atomic layer deposition (ALD) is an advanced surface-controlled CVD technique [12], based on the sequential use of a gas phase chemical process that allows the precisely controlled (atomic layer by atomic layer) deposition of thin films (e.g. high k dielectrics). The majority of ALD processes use two chemicals called precursors. The surface of the sample is exposed alternatively to each one of these precursors and through the repeated exposure and formation of atomic layers, the desired thin film thickness is deposited [12].

Figure 3.5 shows the schematic of the sequential, self-limiting surface reactions during ALD process for a metal-oxide deposition. The surface of the sample has to be hydroxyl (-OH) group terminated (Fig. 3.5(a)) in order to serve as the initial nucleation site for reaction with ALD precursors. Then the sequential ALD process is started by introducing to the reactor a pulse of a metal containing volatile precursor (Fig. 3.5(b)), which reacts with active sites on the sample surface in a self-limiting way. A purge step with a carrier gas (typically N_2 or Ar) removes excess precursor and reaction products (byproducts) forming the first ALD layer (Fig. 3.5(c)). Afterwards, a pulse of an oxygen containing volatile precursor (typically H_2O) is introduced (Fig. 3.5(d)), which reacts with the first chemisorbed precursor, again in a self-limiting way. A second purge step with the carrier gas removes excess precursor and byproducts forming the second ALD layer, with the surface prepared (-OH terminated) to react with another pulse of the first precursor (Fig.

3.5(e)). By carrying out a certain number of ALD cycles, the targeted film thickness can be obtained.

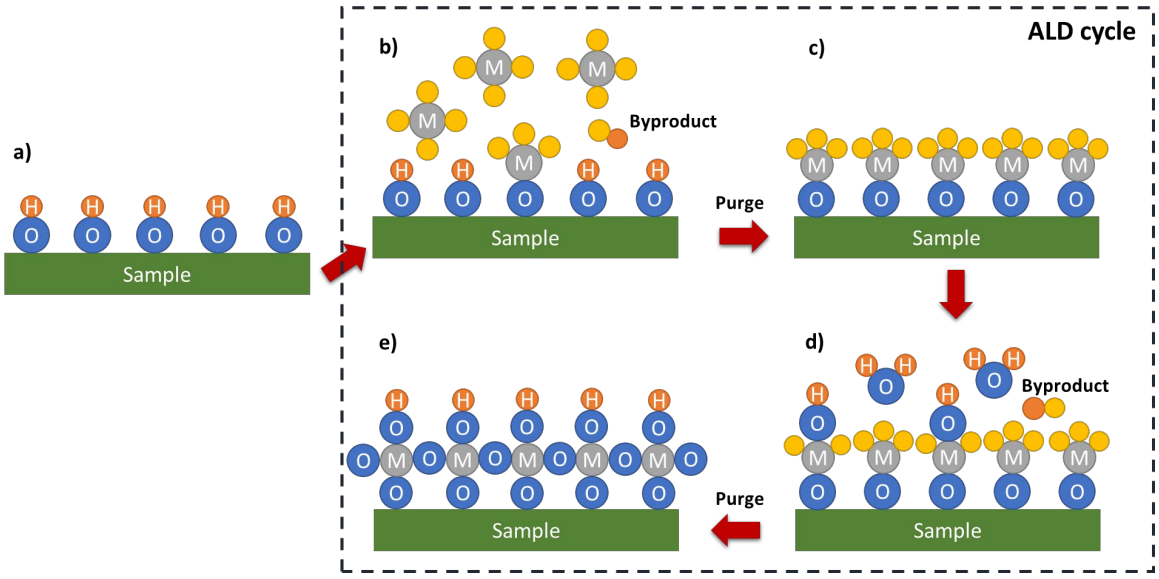

Figure 3.5: *Schematic illustration of a typical ALD process cycle.*

3.7 Plasma ashing

Plasma ashing is a cleaning process using in semiconductor manufacturing to remove organic materials (e.g. photoresists) from a sample surface, through the application of plasma [13–14]. Ashing is commonly performed with oxygen or fluorine reactive gases. An RF field is applied and a monatomic substance (known as reactive species) of the reactive gas is generated under the plasma source [13–14]. The reactive species react with organics to form volatile compounds (byproducts) known as ashes, which are removed with a vacuum pump.

3.8 Electron beam evaporation

Electron beam (e-beam) evaporation is a physical vapor deposition (PVD) technique widely used in metallization processes, as well as in many other applications, including dielectric and optical coatings [15]. Figure 3.6 shows the schematic diagram of e-beam evaporation in a vacuum environment. During e-beam evaporation process, current is passed through a tungsten filament and heats it to the point that electron emission takes place [15]. A strong magnetic field is used to focus and direct the electrons toward the crucible that contains the target material. This highly focused beam of electrons heats the target material and causes its evaporation for deposition onto the sample surface.

One major advantage of this technique, compared to a simple thermal evaporation technique, is the ability to use a multi-crucible material holder with different target materials, which are placed into the path of the electrons by rotation of the holder so that multiple thin films can be deposited sequentially without breaking the vacuum. Compound non-metallic thin films can be deposited by adding to the chamber a partial pressure of reactive gas (e.g. oxygen, nitrogen) during evaporation.

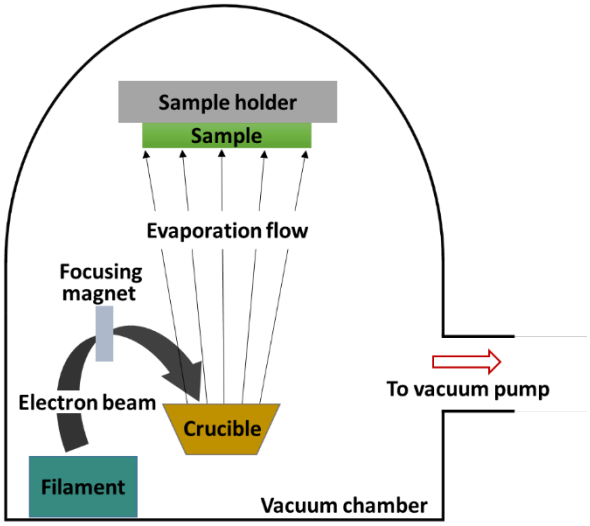

Figure 3.6: *Schematic diagram of an electron beam evaporation system.*

3.9 Rapid thermal annealing

Rapid thermal annealing (RTA) is a semiconductor manufacturing process which heats the sample to high temperatures (over 500 °C) and is mainly used to form low resistance ohmic contacts [16–17]. During heating, sample temperature is brought up rapidly to the desired high temperature in which the sample remains for several seconds (or few minutes) and then is brought down. An RTA system could be also used as a conventional heating stage. The speed of temperature changes may be slow down to prevent thermal effects such as wafer breakage due to thermal shock. The RTA system consists of a vacuum chamber, a sample holder, an infrared (IR) lamp and an infrared (IR) pyrometer.

The sample with the metal-semiconductor ohmic contacts is placed on the sample holder inside a vacuum chamber and an IR lamp is used for heating. The temperature of the wafer is determined with an infrared IR pyrometer. Thermal annealing results to the formation of alloys from initial metal multilayer stacks, which diffuse into the semiconductor material and change drastically the electrical properties of metal-semiconductor interface. The heating temperature and process time are critical parameters for the formation of low resistance ohmic contacts on III-V semiconductors and are of great scientific interest over the last decades [16–17].

3.10 Wet – chemical treatment

Wet – chemical treatments are used at different stages of device fabrication process for sample cleaning or etching. During these processes, the sample is dipped in room temperature or higher temperature solutions. A "cleaning" wet- chemical treatment is necessary before and after each fabrication process to remove any native oxides, metal and organic contaminants. The III-V samples are first dipped in organic solvents (acetone, isopropanol) to remove organic contaminants and then in HCl or HF solutions to remove native oxides and metal contaminants, followed by rinse in deionized (DI) water. Wet-etching treatments are used to etch material from the sample in specific patterns defined by photoresist or metal masks.

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Chapter 4

Fundamentals of device characteristics

4.1 Introduction

The scaling of devices and the shift to vertical architectures keep Moore's law alive and enable the ongoing improvement in device characteristics [1–2]. According to IRDS (International Roadmap for Devices and Systems) tri-gate fin-type technology (FinFETs) and vertical nanowire gate all-around (GAA) technology (Vertical GAA transistors) with 3D integration, are expected to dominate until 2034 [3]. III-V NWs are anticipated to be used for n-channel MOSFETs from 2022, together with strained Si and Ge [3]. Nowadays, fin-type GaN-based MOSFETs [4] and MOS-HEMTs [5–7], as well as vertical GaN-based NW MESFETs [8] and MOSFETs [9–10], have already fabricated and exhibited improved device performances compared to the planar ones [4–6].

This chapter focuses on the basic device operation and electrical DC characteristics of all kinds of devices fabricated in this work, including TLMs, p-n diodes, MOSFETs, MESFETs and HEMTs. A planar device architecture is presented for the sake of simplicity, as the basic device characteristics are independent of device architecture. For a more detailed description of the physics and operational characteristics of these devices the reader should look into books of physics of semiconductor devices, such as of S. M. Sze and K. K. Ng [11] and M. Shur [12]. Especially for p-n junction diodes, the book of G. W. Neudeck [13] is recommended.

4.2 Transmission line model structures

The transmission line model (TLM) structures are test structures fabricated to assess the quality of the ohmic contacts, as well as the electrical properties of the semiconductor material [14]. An ideal metal-semiconductor ohmic contact is defined as a contact with negligible junction resistance relative to the total resistance of the semiconductor device [11]. In an ideal contact (no effect of surface/interface states), ohmic contact behavior is achieved when the work function of the metal (Φ_M) is lower than that of the n-type semiconductor (Φ_S), so that ($\Phi_M < \Phi_S$). The work function of a crystal is defined as the energy required to remove an electron from the Fermi level to the vacuum level (E_0) [11–12]. Another way to achieve ohmic contact is to dope heavily the n-type semiconductor surface (n+), close to the contact region, in order to reduce the width of the potential barrier and efficient quantum-mechanical tunneling can take place [11–12].

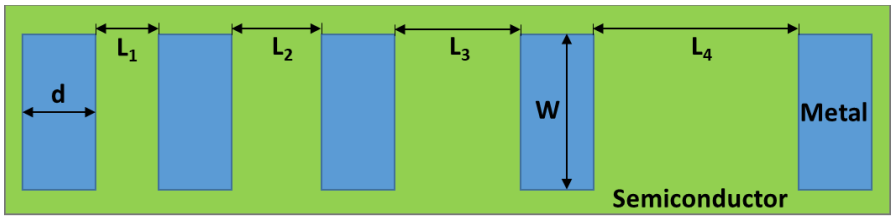

Figure 4.1: *Schematic configuration of a rectangular type TLM structure.*

Figure 4.1 shows the schematic configuration of a TLM structure consisting of rectangular metal contact pads with certain length (L) and width (W). The spacing (L_1, L_2, L_3, L_4) between the contact pads is varied (Fig. 4.1) along the TLM structure. The total resistance (R_T) measured across two metal pads is given by [14]:

$$R_T = 2R_M + 2R_C + R_{sem} \qquad (4.1)$$

where R_M is the resistance due to the metal contact, R_C is the contact resistance associated with the metal/semiconductor interface and R_{sem} is the resistance of the semiconductor layer. By assuming that R_M is negligible compared to the R_{sem} ($R_{sem} >> R_M$), Eq. 4.1 takes the form:

$$R_T = 2R_C + R_{sem} \qquad (4.2)$$

The R_{sem} is given by [14]:

$$R_{sem} = R_{sh}\frac{L}{W} \qquad (4.3)$$

where R_{sh} is the semiconductor sheet resistance. The R_C is given by [14]:

$$R_C = R_{sh}\frac{L_T}{W} \qquad (4.4)$$

where L_T is the transfer length defined as the length of the contact used for transferring most of the current from the metal to semiconductor and vice versa [14].

The plot of the total resistance (R_T) as a function of the contact pad spacing (L) is illustrated in Fig. 4.2, where a linear fit to the measured data is obtained. Four contact parameters can be extracted from this plot: a) the sheet resistance (R_{sh}), b) the contact resistance (R_C), c) the current transfer length (L_T) and d) the specific contact resistance (ρ_C). The slope of the linear fit curve gives the R_{sh}/W value and the intercept with y-axis gives the value of $2R_C$ (Fig 4.2). Typically, the R_C is normalized by multiplication with the W value. The intercept of the linear fit curve with the x-axis gives the $-2L_T$ value (Fig 4.2). The ρ_C is then calculated by [14]:

$$\rho_C = R_{sh}L_T^2 \qquad (4.5)$$

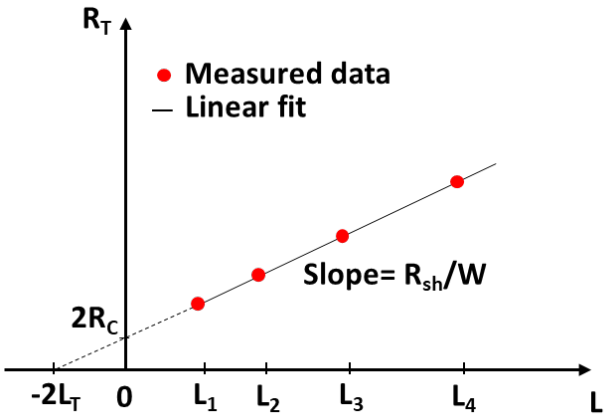

Figure 4.2: *Total resistance (R_T) as a function of contact pad spacing (L) of a typical TLM structure.*

4.3 p-n junction diode

The p-n junction diode is a two-terminal device which is created when two types of semiconductor materials, p-type and n-type are placed in contact [13]. N-type is a semiconductor material with concentration of donor atoms (N_D) greater than that of acceptor atoms (N_A), while $N_A > N_D$ for a p-type semiconductor material. The behavior of the junction is very different from either type of material alone, as free electrons in the n-type semiconductor diffuse across the junction to the p-type semiconductor and combine with the holes that compensate the negative charge of the acceptor ions [13]. In a similar way, the positive charge of donor ions is not compensated by free electrons in the p-type region. Thus, in the n-type and p-type semiconductor, a region near the junction becomes positively and negative charged, respectively, creating a space charge region that is a carrier depletion region [13].

4.3.1 Thermal equilibrium

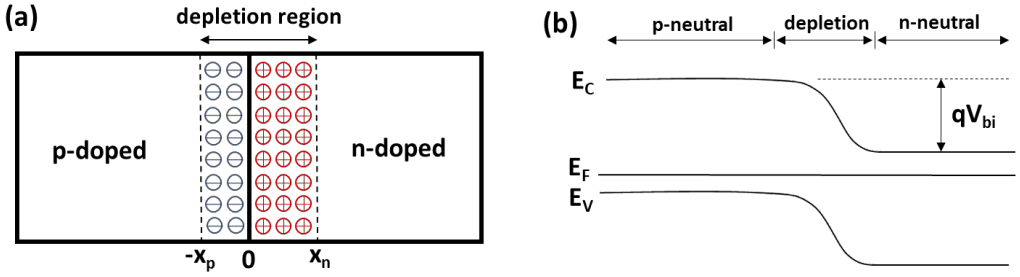

Figure 4.3: *(a) The one dimensional geometry and (b) the energy band diagram of a p-n junction in thermal equilibrium.*

Figure 4.3(a) shows a p–n junction in thermal equilibrium (zero-bias voltage applied) with the formed carrier depletion region near the junction. The x_n and x_p correspond to the depletion region width inside the n-type and p-type semiconductor, respectively. The energy band diagram of this p-n junction is illustrated in Fig. 4.3(b), where the band bending of the conduction-band edge (E_C) in the n-doped region yields to the formation of a built-in potential (V_{bi}), which is calculated by [13]:

$$V_{bi} = \frac{KT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \qquad (4.6)$$

where *K* is the Boltzmann constant, *T* is the absolute temperature and n_i is the semiconductor intrinsic carrier concentration.

The charge density (ρ), in a good crystalline quality semiconductor, is equal to the imbalance between the charge carriers and the ions [13]:

$$\rho = q\left(\mathrm{p} - \mathrm{n} + N_D - N_A\right) \qquad (4.7)$$

By assuming the "depletion approximation" [13], the charge density is zero in the bulk neutral regions, while in the depletion region the carrier concentration (n and p) is negligible compared to the net doping concentration (N_A and N_D), and thus from Eq. 4.7 we have:

$$\rho = -qN_A \text{ for } -x_p \le x \le 0 \qquad (4.8)$$

and

$$\rho = +qN_D \text{ for } 0 \le x \le x_n \qquad (4.9)$$

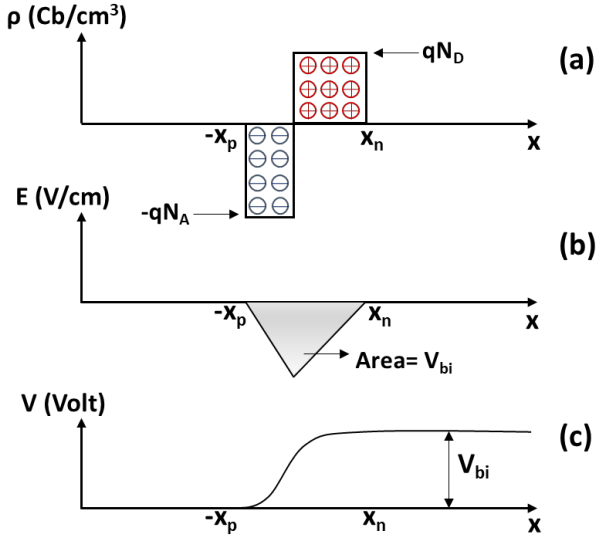

Figure 4.4: *(a) The charge density, (b) the electric field and (c) the potential distribution along a p-n junction in thermal equilibrium.*

In this case, the charge density distribution along the p-n junction is illustrated in Fig. 4.4(a) and since the electric field is zero in the bulk neutral regions of the semiconductor, the total negative charge per unit area in the p-side will be equal to the positive charge per unit area in the n-side [11–13] :

$$N_A x_p = N_D x_n \qquad (4.10)$$

From the Poisson equation the electric field inside the junction (Fig. 4.4(b)) can be obtained from the following equations [11–13]:

$$E(x) = -\frac{qN_A\left(x + x_p\right)}{\varepsilon_s} \quad \text{for } -x_p \le x \le 0 \qquad (4.11)$$

and

$$E(x) = -E_m + \frac{qN_D x}{\varepsilon_s} = -\frac{qN_D}{\varepsilon_s}\left(x_n - x\right) \quad \text{for } 0 \le x \le x_n \qquad (4.12)$$

where ε_s is the permittivity of the semiconductor and E_m the maximum field at the interface of semiconductors (x=0), given by [13]:

$$E_m = \frac{qN_D x_n}{\varepsilon_s} = \frac{qN_A x_p}{\varepsilon_s} \qquad (4.13)$$

In Fig. 4.4(b) the area under the curve of the electric field (E) gives the V_{bi} of the junction. The potential function V(x) within the depletion region derive from the equation [13]:

$$\frac{dV}{dx} = -E \qquad (4.14)$$

The neutral bulk p-region is chosen to be the zero potential reference and then the potential function in the p-type and n-type region, as illustrated in Fig 4.4(c), is given by [13]:

$$V(x) = \frac{qN_A}{2\varepsilon_s}\left(x_p + x\right)^2 \quad \text{for } -x_p \le x \le 0 \qquad (4.15)$$

and

$$V(x) = -\frac{qN_D}{2\varepsilon_s}\left(x_n - x\right)^2 + V_{bi} \quad \text{for } 0 \le x \le x_n \qquad (4.16)$$

Moreover, the total depletion width (W) of the p-n junction can be calculated by [13]:

$$W = x_n + x_p = \left[\frac{2\varepsilon_s V_{bi}}{q}\frac{\left(N_A + N_D\right)}{N_A N_D}\right]^{1/2} \qquad (4.17)$$

4.3.2 Forward and reverse bias

The application of voltage to the p-n junction diode varies the potential difference, the electric field and thus the depletion region width (Fig. 4.5). When a positive voltage is applied to the p-region (Fig. 4.5(a)), electrons and holes are "pushed" toward the junction and decrease the depletion region width and hence the resistance of the device [11–13]. In this case, the p-n junction is forward biased. On the contrary, when negative voltage is applied to the p-region (Fig. 4.5(b)), holes and electrons are "drawn away" of the junction, the depletion region width is increased and hence the resistance of the device is also increased [11–13]. This corresponds to the reverse bias condition of the p-n junction.

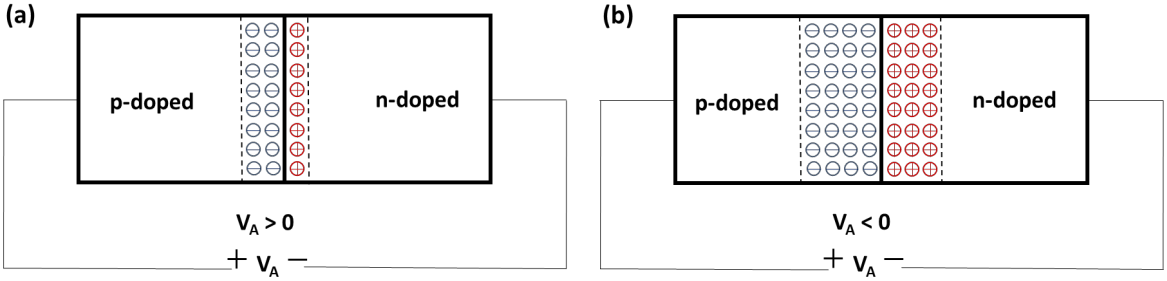

Figure 4.5: *(a) Forward and (b) reverse biased p-n junction diode.*

The depletion region width of the p-n junction when a positive (forward bias) or negative (reverse bias) voltage (V_A), is applied to the p region is given by [13]:

$$W = x_n + x_p = \left[\frac{2\varepsilon_s}{q} \left(V_{bi} - V_A \right) \frac{N_A + N_D}{N_A N_D} \right]^{1/2} \qquad (4.18)$$

which results from the equilibrium equation of depletion width (Eq. 4.17) by using V_{bi}-V_A instead of V_{bi}. This ensures the increased depletion width W for negative V_A and the decreased W for positive V_A.

4.3.3 Current-Voltage characteristics

Figure 4.6 shows the Current-Voltage (I-V) characteristics of a p-n junction diode. When the diode is forward biased, a positive current (from p to n region) passes through the junction. For forward voltages below a threshold voltage (V_{th}), this positive current is almost negligible [11–13]. The V_{th} is the voltage that has to be applied to the diode so that the depletion region will be narrow enough and the electrons and holes of the n and p region, could be efficiently injected to the p and n region, respectively [11–13]. For voltages above V_{th}, the forward current increases rapidly producing an approximatively linear curve as shown in Fig. 4.6, which is determined by the internal resistance of the diode. When the diode is reversed biased, only a small leakage current is observed (Fig. 4.6), as the wide depletion region blocks the flow of the current. This leakage current is

attributed to the minority charge carrier current through the junction and remains very low up to a breakdown voltage (V_{br}) [11–13]. When the negative voltage exceeds V_{br}, the junction breaks down and the reverse current is increased rapidly (Fig. 4.6).

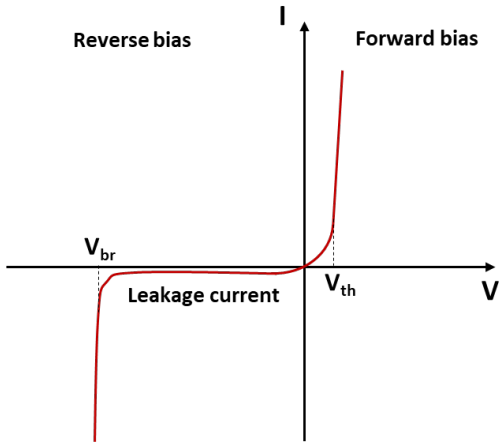

Figure 4.6: *Typical I-V characteristics of a p-n junction diode.*

4.4 Metal oxide semiconductor field effect transistor

A metal oxide semiconductor field-effect transistor (MOSFET) is a type of field-effect transistor (FET) that uses an electric field vertical to the current flow, to control the magnitude of the current [11–12]. MOSFETs have three terminals called source (S), drain (D) and gate (G). The gate terminal is electrically isolated from the main semiconductor channel by a thin layer of insulating material (e.g. aluminum oxide, silicon oxide, silicon nitride). Thus, a metal-oxide-semiconductor (MOS) capacitor or generally a metal-insulator-semiconductor (MIS) capacitor is formed in the gate region [11–12].

The MOSFET is an important solid-state device for modern devices, which is widely used as active element in integrated circuits for switching [15] or amplifying signals [16]. To understand its operation, a metal-oxide-semiconductor (MOS) capacitor has first to be considered.

4.4.1 Metal-oxide-semiconductor capacitor

The band diagram of an ideal n-type metal-oxide-semiconductor (n-MOS) capacitor at thermal equilibrium (zero voltage applied) is illustrated in Fig. 4.7, for the case of an MOS structure with flat bands at zero applied voltage (V_{FB}=0V) and oxide thickness d. The consideration of an ideal MOS structure assumes [11–12]: a) the absence of charges in the oxide layer or any surface states at the oxide-semiconductor interface and b) infinite resistivity of the insulator and thus no current through the insulator under DC biasing conditions. Hence the difference between the metal work function (Φ_M) and the semiconductor work function (Φ_S) is zero [11–12]:

$$\Phi_{MS} = \Phi_M - \left(X + \frac{E_g}{2q} - \Phi_n \right) = \Phi_M - \left(X + \frac{\left(E_C - E_F\right)}{q} \right) = 0 \qquad (4.19)$$

where q is the absolute value of electron charge, X is the electron affinity of semiconductor, E_C is the conduction-band edge, E_V is the valence-band edge, E_g is the energy band gap of the semiconductor and Φ_n (E_F-E_i) is given by [11–12]:

$$\Phi_n = \frac{KT}{q} \ln\left(\frac{N_D}{n_i} \right) \qquad (4.20)$$

where K is the Boltzmann constant, T is the absolute temperature, N_D is the donor concentration in n-semiconductor and n_i is the semiconductor intrinsic carrier concentration (for GaN $n_i = 2 \times 10^{-10}$ cm^{-3} [11]).

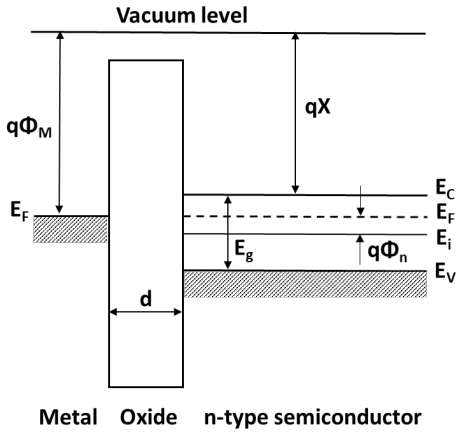

Figure 4.7: The energy band diagram of an ideal n-MOS capacitor with V_{FB}= 0V at thermal equilibrium. *(Based on Physics of semiconductor devices - S.M. Sze and K.K. Ng* [11]).

When a positive voltage (V> 0) is applied to the metal plate, the E_C bends downwards near the surface and comes closer to the Fermi level E_F (Fig. 4.8(a)). The band bending causes an accumulation of majority carriers (electrons) near the semiconductor surface, since the carrier density depends exponentially on the energy difference (E_C – E_F) [11–12]. This corresponds to the accumulation regime and is shown schematically in Fig. 4.8(a). The depletion regime is illustrated in Fig. 4.8(b) in which a small negative voltage (V< 0) is applied to the metal plate. In this case, the bands bend upward and the majority carriers (electrons) are depleted (Fig. 4.8(b)). When a larger negative voltage is applied, the bands bend even more upward so that the E_i at the surface would cross over the E_F (Fig. 4.8(c)). At this point the number of holes (minority carriers) at the surface exceeds that of electrons and the carrier type at the surface region is inverted. This corresponds to the inversion regime and is shown schematically in Fig. 4.8(c). However, it is impossible for wide energy band gap semiconductors (i.e. GaN) to form a surface inversion layer, due to an extremely long generation time at room temperature

and typically only a deep-depletion behavior is observed for high negative applied voltages [17–18].

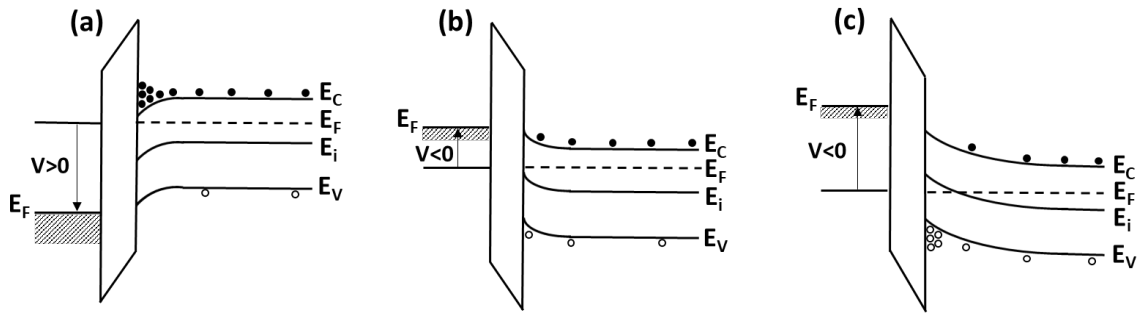

Figure 4.8: The energy band diagrams of ideal n-MOS capacitors under different bias conditions: (a) accumulation, (b) depletion and (c) inversion. *(Based on Physics of semiconductor devices - S.M. Sze and K.K. Ng* [11]).

A MOS capacitor can be also formed on p-type semiconductor material (p-MOS). Similar results (accumulation, depletion and inversion regime) are obtained in this case, but the polarity of the voltage should be changed compared to an n-type MOS capacitor semiconductor [11–12].

4.4.2 Operational characteristics of Si MOSFETs

Two basic types of Si MOSFETs are p-MOSFETs (Fig. 4.9(a)) and n-MOSFETs (Fig. 4.9(b)) concerning p-type and n-type conductivity channel, respectively [11–12]. The channel in conventional Si MOSFETs is formed by biasing the gate MOS capacitor to bring the Si surface region (channel) in carrier inversion condition. The p-MOSFET uses an n-type Si substrate and has heavily doped p+ source and drain regions (Fig. 4.9(a)). The application of negative gate voltage results the electrons present beneath the oxide layer to feel a repulsive force that pushes them downward into the semiconductor substrate (depletion). The negative gate voltage attracts also holes from p+ source and drain regions and enhances the creation of a hole channel region (inversion) between source and drain electrodes. The gate voltage controls the concentration of the holes into the channel (inversion layer) and electric current flows due to the drifting of holes, when a voltage is applied between the source and drain electrodes [11–12].

On the contrary, the n-MOSFET uses p-type Si substrate and has heavily doped n+ source and drain regions (Fig. 4.9(b)). The application of positive gate voltage results the holes present beneath the oxide layer to feel repulsive force and to push downward into the semiconductor substrate (depletion). The positive gate voltage attracts also electrons from n+ source and drain regions into the semiconductor channel region (inversion). The gate voltage controls the electron concentration of the channel and electric current flows due to the drifting electrons when a voltage is applied between the source and the drain electrodes [11–12].

It is critical to mention that III-V semiconductors can be easily grown on insulating substrates or insulating buffer layers. In this case, the applied gate voltage can alter the concentration of the minority carriers at the surface area of device and thus a conductive channel can be formed without need for formation of an inversion layer.

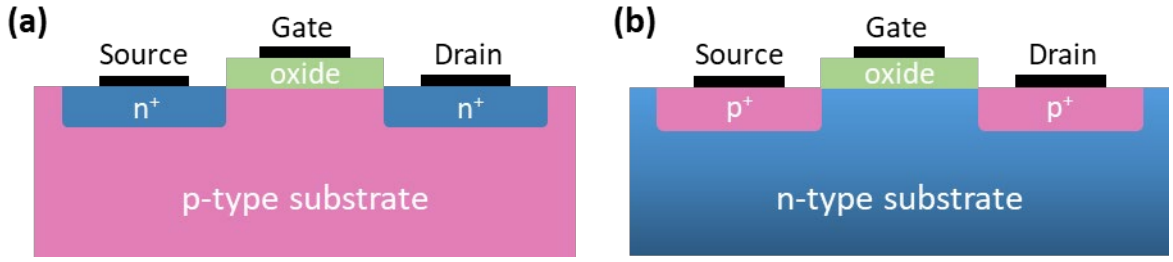

Figure 4.9: Schematic structure of: (a) p-MOSFET and (b) n-MOSFET.

The MOSFETs can function in two modes [11–12]: the depletion mode (normally-on) and the enhancement mode (normally-off). In depletion mode, when zero voltage is applied on the gate, the channel is conductive and the MOSFET is "ON". Positive or negative gate voltage for p-MOSFETs and n-MOSFETs, respectively, is required in order to decrease the conductivity and switch the MOSFET "OFF". In enhancement mode, when zero voltage is applied on the gate the channel is not conductive and the MOSFET is "OFF". Positive (n-MOSFETs) or negative (p-MOSFETs) voltage on the gate is required in order to increase the conductivity and switch the MOSFET "ON".

Table 4.1 summarizes the "ON" and "OFF" states of all types of MOSFETs by applying zero, positive (+V) and negative (-V) gate to source voltage (V_{gs}). The positive and negative V_{gs} exceed the required threshold voltage.

TABLE 4.1: ON and OFF states of all types of MOSFETs by applying different values of V_{gs} bias.

	$V_{gs}=+V$	$V_{gs}=0$	$V_{gs}=-V$
n-MOSFET (Depletion)	ON	ON	OFF
n-MOSFET (Enhancement)	ON	OFF	OFF
p-MOSFET (Depletion)	OFF	ON	ON
p-MOSFET (Enhancement)	OFF	OFF	ON

4.5 Metal semiconductor field effect transistor

A metal semiconductor field-effect transistor (MESFET) is a type of field-effect transistor (FET) with a Schottky (metal-semiconductor) junction diode for gate terminal instead of MOS junction (MOSFET). A depletion region is formed underneath the gate contact that is controlled by the gate voltage and controls the conductivity of the semiconductor channel (modifies the carrier density) [11–12]. The main advantage of the MESFET over the MOSFET is the higher transconductance values and the absence of issues related to oxide-semiconductor interface, such as traps and interface states that are usual in III-V semiconductors [11–12]. However, the Schottky contact induces limitation on bias range applied on the gate to turn the device "ON" [11–12].

4.5.1 Schottky junctions

The energy band diagram of a high work function metal (Φ_M) and an n-type semiconductor that are not in contact, is shown in Fig. 4.10(a). The electron affinity of the semiconductor (X), as well as the energy difference ($q\Phi_n$) between the conduction-band edge (E_C) and the Fermi level (E_F), are also illustrated (Fig. 4.10(a)). In an ideal Schottky contact, as shown in Fig. 4.10(b), an electrostatic potential barrier (Schottky barrier) would be formed at the metal-semiconductor interface (Fig. 4.10(b)) that would depend on the Φ_M, X and Φ_n values. Electrons from the semiconductor flow into the metal creating a depletion region (Fig. 4.10(b)) in the semiconductor. The ideal Schottky junction assumes the absence of surface states and other instabilities at the interface. The formed barrier height ($q\Phi_b$) can be calculated by [11–12]:

$$q\Phi_b = q\left(\Phi_{\mathrm{M}} - \mathrm{X}\right) \qquad (4.21)$$

The existence of this barrier height charges positively the semiconductor and negatively the metal and the resulting potential difference (Fig. 4.10(b)), the built-in potential (V_{bi}), is given by [11–12]:

$$V_{bi} = \Phi_b - \left(\frac{E_C - E_F}{q}\right) \qquad (4.22)$$

The depletion region width (Fig. 4.10(b)) is given by [11–12]:

$$W_d = \sqrt{\frac{2\varepsilon\left(q\Phi_b - KT\ln\dfrac{N_C}{N_D - N_A}\right)}{q^2\left(N_D - N_A\right)}} \qquad (4.23)$$

where ε is the semiconductor permittivity, N_C is the effective density of states in the conduction band, N_D and N_A are the donor and acceptor concentrations of semiconductor, respectively. Equation 4.23 assumes that zero voltage is applied to the junction.

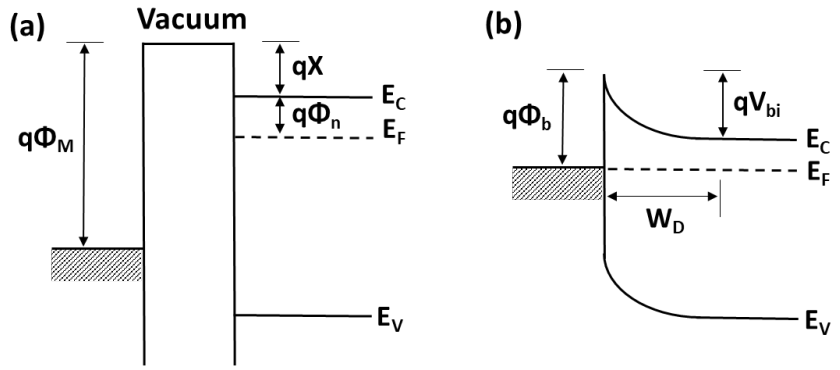

Figure 4.10: Energy band diagram of a metal-semiconductor junction: (a) in separated systems and (b) connected into one system at equilibrium. *(Based on Physics of semiconductor devices - S.M. Sze and K.K. Ng* [11]).

4.5.2 Operational characteristics of MESFETs

The MESFET consists of a conducting channel (n- or p-type) positioned between the source and drain contact region [11–12]. The current flows from source to drain and controlled by the Schottky gate terminal. The gate bias changes the depletion region thickness underneath the gate contact and thereby modulates the channel conductivity. Figure 4.11 shows the schematics of p-channel and n-channel MESFETs. The p-channel MESFET (Fig. 4.11(a)) has a thin p-type active region and heavily p-type doped regions underneath source and drain contacts. The n-channel MESFET (Fig. 4.11(b)) has respectively a thin n-type active region and heavily n-type doped regions underneath the source and drain ohmic contacts to reduce the contact resistance. N-channel MESFETs are preferable for high speed operation due to the higher mobility of electrons than that of holes (p-channel MESFETs) [11–12].

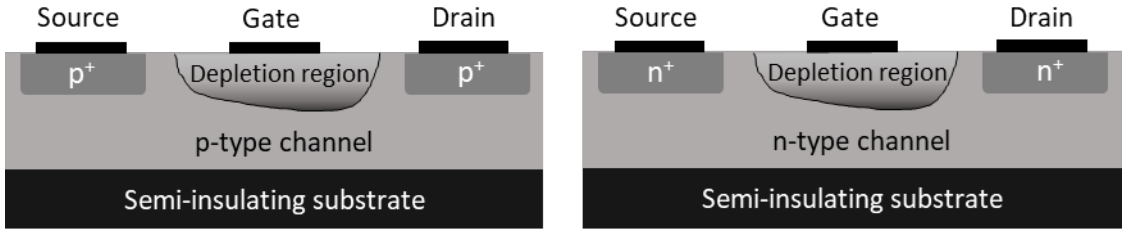

Figure 4.11: Schematic structure of: (a) p-MESFET and (b) n-MESFET.

The MESFETs can function in two modes [11–12]: the depletion mode (normally-on) and the enhancement mode (normally-off). In depletion mode the depletion region does not extend up to the substrate and a conductive channel exists across source and drain terminals even at zero gate bias. A gate voltage is needed to increase the width of the depletion region up to the substrate (pinch off the channel) and turn the device "OFF". In enhancement mode, the MESFET is "OFF" even at zero gate bias as the channel

is totally depleted. A gate voltage is needed to shrink the depletion region and turn the MESFET "ON".

4.6 High electron mobility transistor

The high electron mobility transistor (HEMT) or heterostructure field effect transistor (HFET) is a type of FET that uses a heterojunction (section 2.3) with a high density two-dimensional electron gas (2DEG) as the channel, instead of a doped region (i.e. MESFET) [11–12]. Unlike $Al_xGa_{1-x}As$/GaAs HEMT [19], requiring intentional doping to form the 2DEG channel, in $Al_xGa_{1-x}N$/GaN based HEMTs (Fig. 4.12) the 2DEG is induced by the net-positive polarization charge at the $Al_xGa_{1-x}N$/GaN interface (section 2.2) [20–22]. The $Al_xGa_{1-x}N$/GaN based HEMTs, and especially the AlN/GaN heterostructure that offers the highest 2DEG density, are the ultimate candidates for high frequency and high-power switching applications [20–22]. The following section will focus on the $Al_xGa_{1-x}N$/GaN based HEMTs that have been investigated in this work.

The operation of $Al_xGa_{1-x}N$/GaN HEMTs is based on the formation of a triangular potential well, the 2DEG, due to the polarization discontinuity at the $Al_xGa_{1-x}N$/GaN interface (Fig. 4.12). The 2DEG density depends also on the $Al_xGa_{1-x}N$ barrier thickness. The increase of the $Al_xGa_{1-x}N$ thickness reduces the built-in electric field due to a fixed surface potential, within the $Al_xGa_{1-x}N$ barrier, and deepens the 2DEG triangular quantum well [20]. The modulation of the current in the channel is performed by applying a gate voltage through the Schottky (Fig. 4.12) or MOS gate contact. This type of HEMT is typically normally-on and a negatively biased gate is needed in order to turn it off.

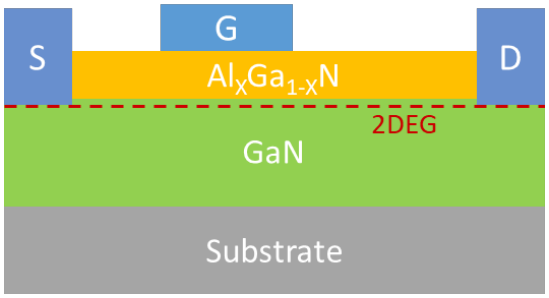

Figure 4.12: Schematic structure of an $Al_xGa_{1-x}N$/GaN HEMT.

4.7 Current-Voltage DC characteristics of transistors

In this section, some basic terms for evaluation of transistor performance will be defined. These terms are typical for all kinds of transistors (MOSFETs, MESFETs and HEMTs) analyzed in this chapter.

4.7.1 Geometrical parameters of transistors

The basic geometrical parameters of transistors, as illustrated in Fig. 4.13, are the gate length (L_g), the gate width (W_g), the source to drain distance (L_{sd}), the source to gate distance (L_{sg}) and the gate to drain distance (L_{gd}). All these parameters, as well as the oxide thickness (t_{ox}) for MOSFETs (Fig. 4.13), are critical for transistor performance. Minimizing transistor dimensions increases the number of chips per wafer and also provides faster and more efficient devices.

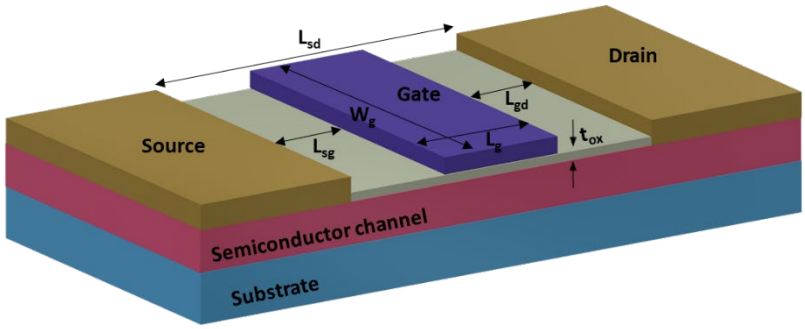

Figure 4.13: Schematic configuration of a typical MOSFET with all the geometrical parameters identified.

4.7.2 Output and transfer I-V characteristics

The DC behavior of transistors is characterized by current-voltage (I-V) measurements known as output and transfer I-V characteristics [11–12]. The output I-V characteristics (Fig. 4.14(a)) show the variation of drain to source current (I_{ds}) with drain to source voltage (V_{ds}) for various fixed gate to source voltages (V_{gs}). The output characteristics can be divided into five regions (Fig. 4.14(a)): a) the linear, b) the nonlinear, c) the saturation and d) the breakdown region. In linear region, V_{ds} takes small values and I_{ds} is proportional to V_{ds}, while in nonlinear region, I_{ds} gradually levels off and in saturation region takes its maximum value and remains essentially constant and independent of V_{ds}. Finally, in breakdown region, V_{ds} takes high values, which are causing breakdown of the drain to source channel and I_{ds} is increasing drastically (Fig. 4.14(a)). The fixed V_{gs} voltages can take positive or negative values depending on the kind of transistor (Table 4.1).

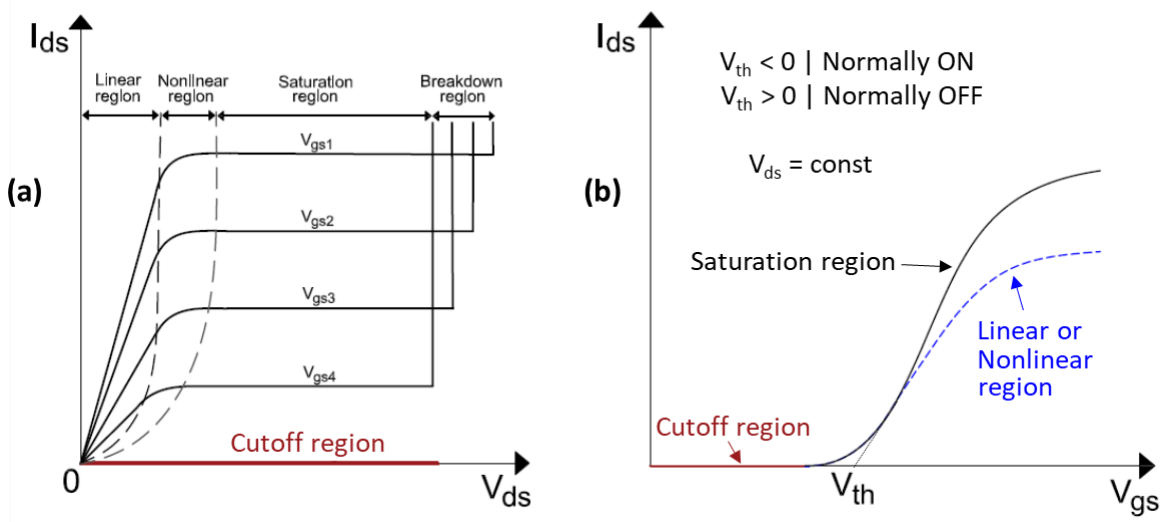

Figure 4.14: (a) Output and (b) Transfer I-V characteristics of a conventional transistor.

The transfer characteristics (Fig. 4.14(b)) show the variation of I_{ds} with V_{gs} when V_{ds} takes a fixed value. Figure 4.14(b) shows the corresponding output characteristic regions (linear, nonlinear, cutoff and saturation) as depicted in a transfer characteristic curve. In cutoff region, I_{ds} remains zero until V_{gs} exceeds the value of a threshold voltage (V_{th}). The V_{th} is defined as the gate bias intercept of the linear extrapolation of I_{ds} to 0 A (Fig. 4.14(b)). As V_{gs} exceeds $V_{th,}$ current passes through the device and I_{ds} increases. For a fixed V_{ds} value in the saturation region (Fig. 4.14(a)), I_{ds} takes the maximum saturated values of Fig. 4.14(a) by varying V_{gs} ($V_{gs} > V_{th}$). This characteristic curve is illustrated in Fig. 4.14(b) with black color. For a fixed V_{ds} value in the linear or nonlinear region (Fig. 4.14(a)), I_{ds} curve will exhibit a similar behavior but decreased I_{ds} values, as shown indicatively in Fig. 4.14(b) with the bluish dashed curve.

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Chapter 5

Growth and formation of GaN NWs and fins

5.1 Introduction

The GaN nanowires (NWs) and GaN-based films studied in this thesis were grown by Plasma Assisted Molecular Beam Epitaxy (PAMBE) in a 32P RIBER MBE system [1–3]. PAMBE is a catalyst-free method that combines an ultra-high vacuum environment and high-impurity starting elements to grow high-quality GaN NWs [4–6] without extended crystalline defects. There are several other methods for the spontaneous (bottom-up) synthesis of GaN NWs, including plasma enhanced chemical vapor deposition (PECVD) [7], metal-organic chemical vapor deposition (MOCVD) [8] and laser-assist catalytic growth (LCG) [9]. The major disadvantage of the spontaneous (bottom-up) approach for formation of GaN NWs concerns the randomness of their positions and dimensions. However, these are critical parameters for the assembly of vertical nanoscale electronic and optoelectronic devices and led to research of different approaches for formation of GaN NWs, such us selective area growth (SAG) [10–12] and top-down NW fabrication techniques [13–15]. SAG is a method to selectively grow straight, vertical GaN NWs at sites of the substrate specified by a dielectric [10–11] or metal mask [12]. The complexity of this method has recently shifted interest to a top-down approach for formation of vertical GaN NWs from GaN films, by combining conventional nanofabrication techniques and a wet-chemical treatment [13–15].

In this chapter, all the experimental techniques used in this thesis for bottom-up growth or top-down formation of GaN-based NWs and fins, will be briefly discussed. The GaN NWs and nanofins were used for the fabrication of GaN-based NW devices and FinFETs, respectively. The advantages and disadvantages of each technique, focusing on the potential to fabricate advanced nanoscale devices, will be presented.

5.2 Spontaneous growth of GaN NWs

The spontaneous growth of GaN NWs by PAMBE is a bottom-up NW formation technique, which involves nanoscale atomic interactions for nucleation and growth of GaN NWs on a substrate [16]. Spontaneously grown GaN NWs may be used in device applications, such as sensors [17], solar cells [18], and piezoelectric generators [19], in which the accurate control of the location and arrangement of GaN NWs on the substrate are not critical.

In this work, GaN NWs were grown spontaneously by PAMBE under N-rich conditions, on Si (111) substrates [5–6, 20]. Initially, a very thin AlN pre-layer was deposited to enhance the GaN nucleation [6]. The main axis of the formed NWs is parallel to the [0001] direction (c-axis), as confirmed by XRD measurements [20]. For an in depth analysis

of the mechanisms and physics in growth of these GaN NWs, the reader is cited to the Ph.D. dissertation of S. Eftychis [20].

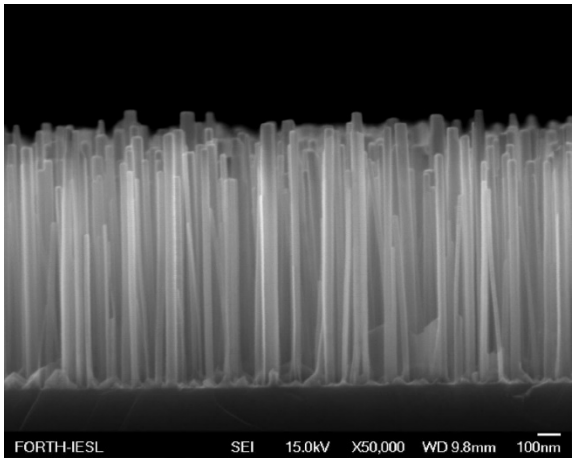

Figure 5.1: *Cross-section SEM image of GaN NWs grown on Si (111) substrate.*

Figure 5.1 shows a cross-section SEM image of GaN NWs grown on a Si (111) substrate, with an average height of ~1μm and diameters varying from 15-65 nm. The average height and diameter of GaN NWs depended on growth time and increased linearly as the growth duration increased [20]. The coalescence of GaN NWs during growth resulted to larger diameter NWs.

5.3 Selective area growth of GaN NWs and fins

Selective area growth (SAG) has been actively developed for aligning GaN NWs on different substrates without using metal catalysts [10–12]. This is accomplished by patterning a dielectric [10–11] or metal mask [12] on a suitable substrate by electron-beam lithography and reactive-ion etching. The SAG of GaN NWs at predefined sites (windows) on masked substrates allows the accurate control of their position, dimensions and density and the formation of nanowire arrays, which will be suitable for the processing of vertical nanowire devices, such as vertical GaN NW transistors.

In this work, two different substrates were used for the SAG of GaN NWs: a) Si (111) substrates with thermally grown SiO_2 (silicon dioxide) mask on top, and b) GaN (000-1) buffer layer on Si (111) substrates, with 25 nm ALD deposited SiO_2 mask on top. The main advantage of the first case is its simplicity, as only one lithographic and one epitaxial growth process step are needed [11]. There is no need to grow any buffer layer below the mask, while the Si substrate is used to grow the high-quality SiO_2 mask by thermal oxidization. Nevertheless, our initial study of GaN NWs SAG on Si (111) substrates patterned with a thermally grown SiO_2 mask, revealed the difficulty of filling Si mask windows with a spacing (pitch) shorter than the diffusion length of Ga adatoms on the SiO_2 surface [11, 20]. To overcome this limitation, the PAMBE SAG of NWs on patterned GaN buffer layers has been investigated. This case involves epitaxial growth of a GaN (000-1) buffer layer and ALD deposition of a SiO_2 film on the GaN (000-1) buffer layer.

The SiO_2/Si patterned substrates have been prepared by collaborating researchers (P. Dimitrakis, A. Olziersky and P. Normand) of the Institute of Nanoscience and Nanotechnology, National Center of Scientific Research (NCSR) "Demokritos". The deposition and nanopatterning of dielectric SiO_2 mask on the (000-1) GaN/Si substrates (prepared by Dr. A. Adikimenakis at FORTH) have been accomplished by Dr. D. Mailly of the Centre National de la Recherche Scientifique (CNRS), Marcoussis, Paris, France. The SiO_2/GaN/Si nanopatterning research work received funding from the EU-H2020 programme under grant agreement No 654360 having benefitted from the access provided by CNRS within the framework of the NFFA-Europe Transnational Access Activity.

5.3.1 GaN growth on SiO_2/Si patterned substrates

The formation of the mask started by oxidizing the Si (111) substrate to thermally grow a 20 nm thick SiO_2 layer on its surface. Subsequently, nano-patterning was carried out by e-beam lithography and RIE with a CHF_3/Ar (Trifluoromethane/Argon) gas mixture [11, 20]. The final nano-patterned areas comprised square and hexagonal arrays of circular windows with nominal diameters and pitches (window spacing) ranging from 20 nm to 200 nm and from 50 nm to 10 μm, respectively [11, 20]. The arrangement of mask windows inside the arrays of hexagonal or square pattern are shown in Fig. 5.2(a) and Fig. 5.2(b), respectively. Moreover, horizontal nanoribbons with 150 nm width, 3 μm length and 6 μm pitch, were also nano-patterned.

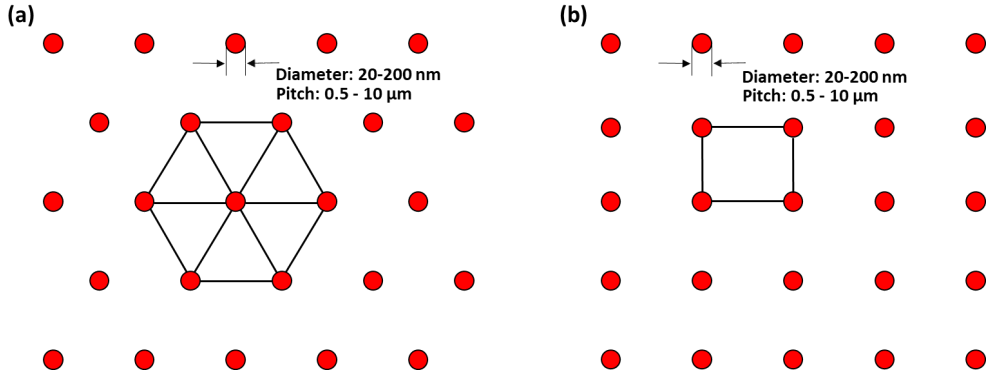

Figure 5.2: *Schematic configuration of mask windows arrangement with: (a) hexagonal and (b) square pattern.*

Prior to loading the nano-patterned SiO_2/Si substrates to the PAMBE system, a wet etching treatment was performed by dipping the samples into a 1% HF solution for 20 sec, in order to remove the residual native oxide formed in the mask windows [11, 20]. SEM images indicated that this chemical treatment didn't significantly affect the nominal dimensions of mask openings [11, 20]. Afterwards, approximately 2 ML of AlN were deposited to enhance the GaN nucleation and GaN was subsequently deposited for a total growth time of 3h, at a constant substrate temperature of 760 °C. The Ga:N incident flux ratio was kept constant at approximately 1:5 [11, 20].

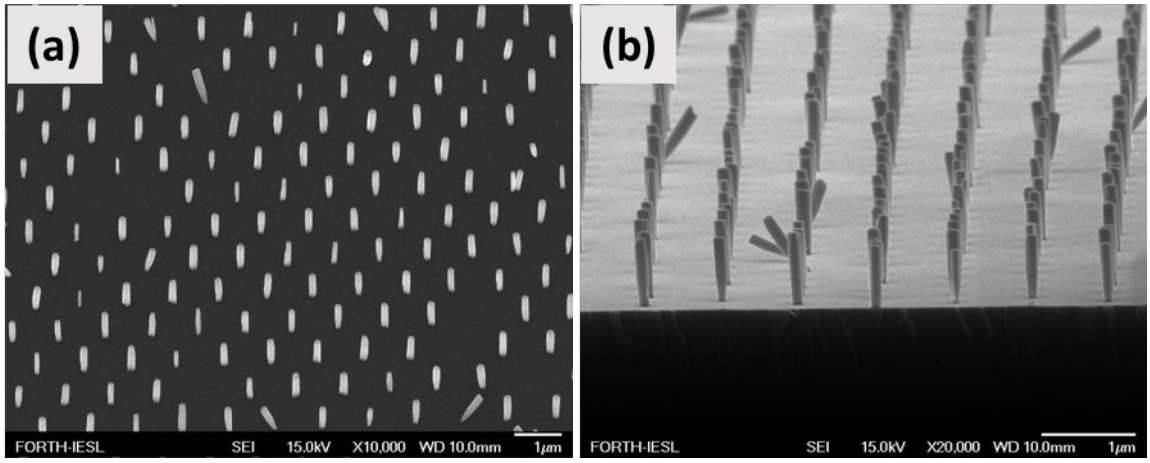

Figure 5.3: *SEM images in (a) titled view and (b) bird's eye view of GaN NWs grown on masked Si (111) substrates with window spacing of 1μm and diameter of 40 nm.*

Figure 5.3(a) illustrates, in tilted view, a SEM image of GaN NWs with average height of 600 nm, on mask region with 40 nm diameter and 1 μm window spacing. A systematic analysis [11, 20] indicated that a window diameter less than 50nm and a window spacing larger than 500nm can provide single NW nucleation in nearly all mask windows [11, 20]. The diameter of the GaN NWs was larger than the diameter of the mask window in which they were nucleated [11, 20]. Hence, it is difficult to control the diameter and spacing of GaN NWs grown by SAG on bare Si (111) substrates, critical parameters for the fabrication of vertical devices, such as vertical GaN NW transistors. Moreover, the deviation from the desired straight, vertical growth of few GaN NWs and thus the existence of inclined NWs, as shown in the bird's eye view SEM image of Fig. 5.3(b), may also result to short-circuit issues on the fabrication of NW devices.

Figure 5.4: *SEM image in titled view of GaN fins grown on masked Si (111) substrates with 150 nm width, 3 μm length and 6 μm pitch.*

Except of the circular windows, nanoribbons (stripes) had been also patterned on the SiO_2/Si (111) substrates. The main objective of this pattern was to explore the potential to grow GaN fins, which are widely used for the fabrication of FinFETs [21–22]. Figure 5.4

shows, in tilted view, a SEM image of GaN grown within nanoribbons with 150 nm width, 3 μm length and 6 μm pitch. It is obvious (Fig. 5.4) that the GaN-on-Si nucleation resulted to the growth of multiple GaN NWs inside each nanoribbon, instead of a compact fin material.

5.3.2 GaN growth on SiO_2/GaN/Si patterned substrates

In order to overcome the issues described in previous section for SAG nano-patterning on SiO_2/Si substrates, a more complicated but also more promising procedure was examined by patterning GaN (000-1) buffer layers on Si (111) substrates. Initially, a 500 nm thick n+ GaN (000-1) N-face film was epitaxial grown by PAMBE on a 3-inch diameter Si (111) wafer. The formation of the mask started by ALD deposition of a 25 nm thick SiO_2 dielectric layer. Then, the nano-patterning was carried out by e-beam lithography and RIE using a SF_6/O_2 (Sulfur hexafluoride/Oxygen) gas mixture. The final nano-patterned areas consisted of hexagonal arrays of circular windows with nominal diameters and pitches (window spacing) ranging from 60 nm to 150 nm and from 250 nm to 1 μm, respectively. The arrangement of mask windows inside the arrays followed the hexagonal pattern shown in Fig. 5.5.

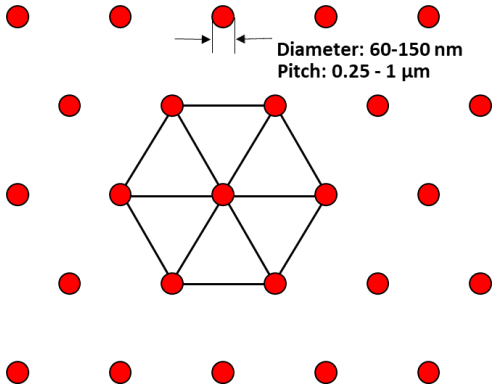

Figure 5.5: *Schematic configuration of hexagonal pattern arrangement of mask windows formed on SiO_2/GaN/Si substrates.*

Prior to loading the samples into the PAMBE system, a wet etching pre-treatment was performed by dipping the samples into a H_2SO_4:H_2O_2 (1:4) solution for 20 min to remove any contaminants during processing steps and subsequently to a HCl: H_2O (1:10) solution for 5 min to remove native oxides formed in the GaN mask windows [11, 20]. GaN was then deposited for a total growth time of 8h, at a constant substrate temperature of 750 °C, while Ga:N incident flux ratio was kept constant at approximately 1:3 [11, 20].

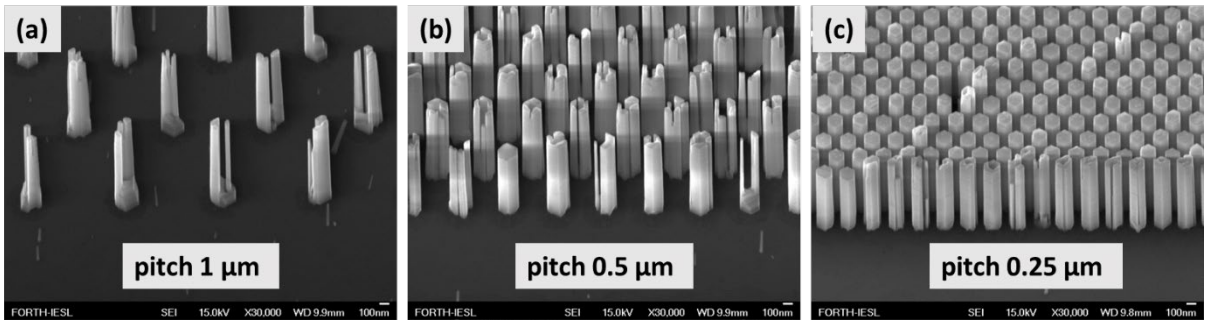

Figure 5.6: *SEM images in titled view of GaN NWs grown on SiO_2/GaN/Si patterned substrates, with window spacing of: (a) 1 μm, (b) 0.5 μm and (c) 0.25 μm.*

Figure 5.6 illustrates, in titled view, SEM images of ~1.5 μm height GaN NWs, grown on mask regions with windows of 100 nm diameter and pitch of 1 μm (Fig. 5.6(a)), 0.5 μm (Fig. 5.6(b)) and 0.25 μm (Fig. 5.6(c)). As shown in Fig. 5.6, the deposition of GaN material was enhanced by the reduction of window pitch, contrary to the results observed by using SiO_2/Si patterned substrates [11, 20]. Separate GaN NWs of narrow diameter were grown at the edges of windows with 1000 nm pitch (Fig. 5.6(a)), while a unique large diameter GaN NW (nanorod) was apparent within each GaN window for 250 nm pitch (Fig. 5.6(c)). An intermediate structure was observed for the intermediate pitch of 500 nm (Fig. 5.6(b)). These findings indicate the enhancement of the condensation of incident Ga and N atoms at the short pitch SiO_2/GaN mask areas and is attributed to a higher state-steady flux of adatoms on the GaN NW sidewalls resulting from adatoms re-evaporated from the adjacent NW sidewalls, when they are incident far from one diffusion length from the {0001} top NW face. However, photoluminescence experiments revealed superior properties for the separate narrow NWs, which may suggest the formation of defects in the compact large diameter NWs due to coalescence of multiple narrow NWs.

Further investigations are ongoing to obtain a deeper understanding for the NW structure and properties on the patterned SiO_2/GaN/Si (111) substrates. In case of vertical GaN device fabrication a dense GaN NW array would increase the integration density but also complicates the device fabrication process, as shadow effects may occur, for vapor material depositions. Nevertheless, the existence of a single thick GaN NW inside each mask window that follows the dimensions of the patterning, makes this technique promising for future exploitation in the fabrication of vertical GaN NW transistors.

5.3.3 Top-down formation of GaN NWs and GaN-based Fins

The complexity and the issues mentioned in previous sections for SAG growth of GaN NWs have recently shifted interest to a top-down approach for formation of vertical GaN NWs from GaN films by three processing steps: nanopatterning by electron-beam lithography (e-beam), reactive-ion etching (RIE) and anisotropic wet-chemical etching based on a Tetramethylammonium hydroxide (TMAH) or Potassium hydroxide (KOH)

solution [13–15]. This method is also applied for formation of GaN-based fins from GaN-based films [21–22].

Figure 5.7 shows the schematics and corresponding SEM images of the overall process flow steps used for the formation of vertical GaN NWs from GaN films. The first step includes the patterning of a circular metal etch-mask on the surface of the sample (Fig. 5.7(a)). Afterwards, RIE is carried out to form the trapezoidal GaN structures shown in Fig. 5.7(b). Without removing the metal mask, a wet etching treatment was then performed by dipping the samples into a TMAH solution (Fig. 5.7(c)). This treatment not only removes the plasma damage but also smooths the lateral surface of the RIE-formed NWs and further reduces their diameter [13–15]. Due to its strong anisotropic behavior, with negligible etching along the c-axis [23–24], very steep and uniform GaN NWs are obtained (Fig. 5.7(c)). The final diameter of GaN NWs depends on the dipping time into the TMAH or KOH solution and reduces as this time increases [24].

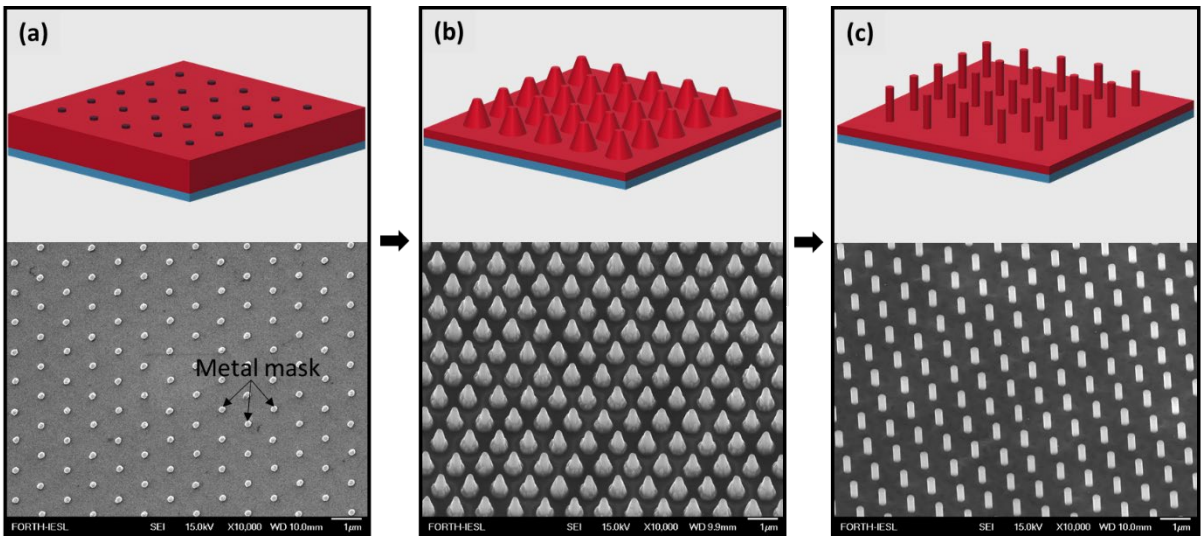

Figure 5.7: *Schematics and corresponding SEM images showing the process flow steps for formation of GaN NWs from GaN films after the following processing steps: (a) patterning of a metal etch-mask, (b) reactive ion etching of GaN film through the patterned metal mask and c)TMAH-based wet chemical etching treatment.*

A similar procedure is used for the formation of GaN-based fins (Fig. 5.8) [21–22]. The process flow starts with the patterning of the metal etch-mask, which in this case has ribbon shape patterns (Fig. 5.8(a)). Subsequently, RIE is carried out to form the GaN-based fins (Fig. 5.8(b)) and then a TMAH or KOH solution is performed to remove the plasma damage and also to smooth the lateral surface of the RIE-formed fins (Fig. 5.8(c)).

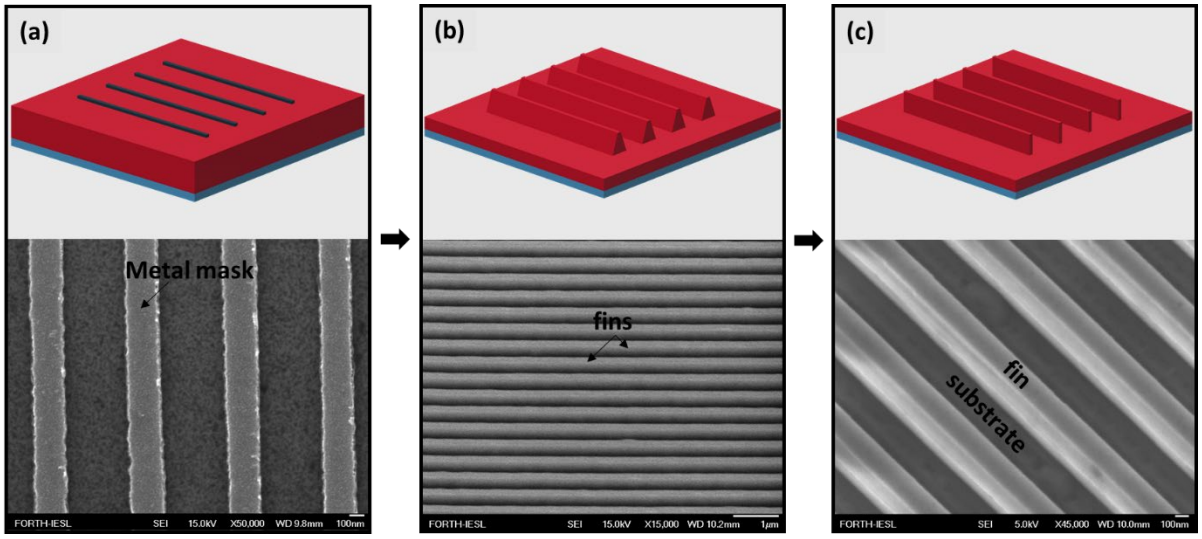

Figure 5.8: *Schematics and corresponding SEM images showing the process flow steps for formation of GaN-based fins from GaN films after the following processing steps: (a) patterning of a metal etch-mask, (b) reactive ion etching of GaN film through the patterned metal mask and c) TMAH-based wet chemical etching treatment.*

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Chapter 6

Bottom-up GaN nanowire devices

6.1 Introduction

Nanodimensional III-Nitrides, such as GaN nanowires (NWs), are promising elements for the reduction of dislocation density and due to their small sizes for application in high performance devices [1–3]. Epitaxial bottom-up grown GaN NWs [4–6] are expected to enable the realization of perfect semiconductor crystals on dissimilar high lattice-mismatched substrates and provide a unique exploitation potential for monolithic integration of heterogeneous materials for nanoelectronics and microsystems [7–8].

This chapter focuses on the evaluation and understanding of size effects on the conductivity of bottom-up grown GaN NWs on Si (111) substrates and the fabrication of GaN-based vertical NW diodes grown on p-Si (111) substrates by PAMBE. A NW device fabrication process based on electron beam lithography (EBL) was designed in order to characterize the bottom-up grown GaN NWs. Multiple ohmic contacts were defined by EBL, followed by e-beam evaporation to individual GaN NWs dispersed on SiO_2/Si substrates with diameters ranging from 30 to 140 nm and lengths ranging from 500 to 1900 nm. The electrical transport properties of individual GaN NWs were evaluated by DC I-V measurements. The p-Si/n-GaN NW heterojunction diodes were fabricated using conventional nanofabrication techniques and characterized by I-V measurements. Circular ohmic contacts with diameters of 180 μm and 390 μm were defined on the top 200 nm part of a group of GaN NWs with average height of 800 nm. The p-Si (111) substrate used as the bottom p-type contact (anode). The diodes exhibited a clear rectifying behavior, although a non-optimized fabrication process was used.

6.2 Surface depletion effects in GaN NWs

The electronic properties of semiconductor surface are markedly different compared to that of bulk material, due to the existence of surface states [9]. The large surface-to-volume ratio of GaN NWs and thus the high density of surface states is expected to play a critical role in the determination of NW conductivity. Fermi level pinning at the surface is a usual phenomenon in III–V semiconductors and is also present in GaN [10–11]. The presence of surface states on the free lateral sides of GaN NW induce Fermi level pinning at the surface and create a band bending along the radius of the NW and corresponding carrier depletion inside the GaN NW crystal (Fig. 6.1), as if a Schottky barrier contact was present on the surface [10–11].

The schematic of Fig. 6.1(a) shows a possible energy band profile along a radial x-direction of a cylindrical n-type GaN NW with diameter d_1, when surface states at the

lateral GaN NW sides pin the Fermi level (E_F) at energy $q\Phi_B$ below the conduction band edge E_C [12]. The radial x-direction is assumed to lie on a circular cross-section of the NW perpendicularly to its axis, with x= 0 being the center and d_1 the diameter of the NW cross-section cycle [12]. The surface potential $q\Phi_B$ would create band bending and carrier depletion for depth W_{dep} along the radial x-direction toward the NW center (x= 0) that could be approximated (the accurate solution should be based on cylindrical coordinates [13]) with the standard equation of the one-dimensional planar case [14]:

$$W_{dep} = \sqrt{\frac{2\varepsilon\left(q\Phi_B - KT\ln\frac{N_C}{N_D - N_A}\right)}{q^2\left(N_D - N_A\right)}} \quad (6.1)$$

where ε is the permittivity, K is the Boltzmann constant, T is the absolute temperature, N_C is the effective density of states in the conduction band, N_D and N_A are the donor and acceptor concentrations in GaN, respectively, q is the absolute value of electron charge and $q\Phi_B = (E_C - E_F)$ is the surface potential on the lateral sides of GaN NW (x= $\pm d_1/2$) [12].

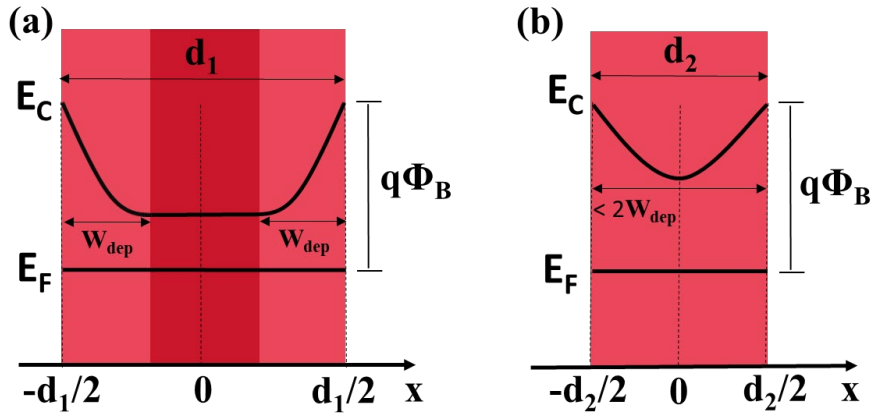

Figure 6.1: *Effect of Fermi level (E_F) pinning at the lateral NW surface on the profile of the conduction band edge (E_C) along a radial x-direction of a cylindrical vertical n-GaN NW with diameter (a) $d_1 > 2W_{dep}$ and (b) $d_2 < 2W_{dep}$* [12].

The schematic of Fig. 6.1(a) assumes that $d_1 > 2W_{dep}$, and thus a central cylindrical part of the NW with diameter $d - 2W_{dep}$ will be undepleted (neutral). However, as shown in Fig. 6.1(b) full depletion (punch through) of the NW will occur if $d_2 < 2W_{dep}$ and this defines a critical NW diameter $d_{crit} = 2R_{crit} = 2W_{dep}$ that will depend on the equilibrium electron concentration $n = N_D - N_A$ in neutral GaN, according to Eq. 6.1 [12]:

$$d_{crit} = 2W_{dep} = \sqrt{\frac{8\varepsilon\left(q\Phi_B - KT\ln\frac{N_C}{N_D - N_A}\right)}{q^2\left(N_D - N_A\right)}} \quad (6.2)$$

As we mentioned above, Eqs. 6.1 and 6.2 give an estimation for the carrier depletion depth (W_{dep}) and critical NW diameter (d_{crit}), respectively. The accurate solutions should be based on solution of the Poisson's equation using cylindrical coordinates [13] and in this case the $d_{crit(cyl)}$ is given by [10, 13]:

$$d_{crit(cyl)} = 2\sqrt{2}W_{dep} = \sqrt{\frac{16\varepsilon\left(q\Phi_B - KT\ln\frac{N_C}{N_D - N_A}\right)}{q^2\left(N_D - N_A\right)}} \quad (6.3)$$

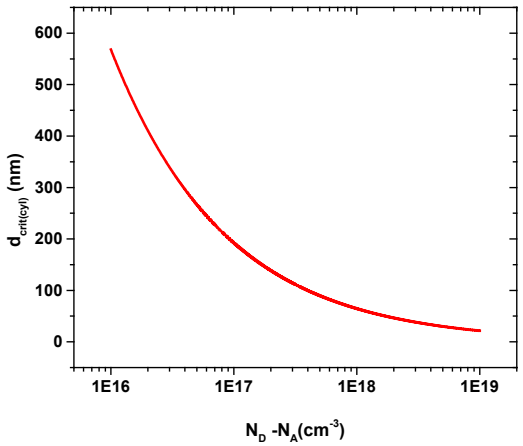

Figure 6.2: *Critical GaN NW diameter ($d_{crit(cyl)}$) calculated by solving Poisson's equation with* cylindrical coordinates, *as a function of background electron concentration ($N_D - N_A$).*

Figure 6.2 illustrates the expected $d_{crit(cyl)}$ for n-type GaN NWs as a function of $N_D - N_A$ according to Eq. 6.3, by assuming room temperature ($kT \approx 0.026$ eV), $N_C = 2.2\times10^{18}$ cm^{-3} [10–11,14] and $q\Phi_B = 0.55$ eV [10–11]. The calculation of W_{dep} in cylindrical coordinates ($W_{dep(cyl)}$) has a non-trivial solution as $W_{dep(cyl)}$ also depends on the NW radius ($r = d/2$) [13]. A transcendental equation is obtained for $W_{dep(cyl)}$ as a function of r [13]:

$$\left(\frac{r - W_{dep(cyl)}}{r}\right)^2\left[1 - \ln\left(\frac{r - W_{dep(cyl)}}{r}\right)^2\right] = 1 - \frac{2\xi^2}{r^2} \quad (6.4)$$

where

$$\xi = \sqrt{\frac{2\varepsilon\left(q\Phi_B - KT\ln\frac{N_C}{N_D - N_A}\right)}{q^2\left(N_D - N_A\right)}} \quad (6.5)$$

the characteristic depletion depth of the one-dimensional planar case [14]. Equation 6.4 can be rewritten in terms of dimensionless quantities as [13]:

$$y\left(1-\ln y\right)=1-x \quad (6.6)$$

where $y=\left(r-W_{dep(cyl)}\right)^2/r^2$ and $x=2\xi^2/R^2$. The value of x is fixed and Eq. 6.6 can be solved numerically for y. By determining a value of y that satisfies Eq. 6.6, the $W_{dep(cyl)}$ is given by [13]:

$$W_{dep(cyl)}\left(r\right)=r\left[1-\sqrt{y\left(x\right)}\right] \quad (6.7)$$

From the above equations (Eqs. 6.4 to 6.7) it is difficult to obtain an analytical solution of $W_{dep(cyl)}$ as a function of N_D-N_A. However, a graphical approach was used to find an approximate solution and the results are illustrated in Fig. 6.3, for GaN NWs with radius of 50, 100, 150 and 250 nm. The one-dimensional (1D) solution (Eq. 6.1) of carrier depletion depth (W_{dep}) is also depicted for comparison reasons (Fig. 6.3).

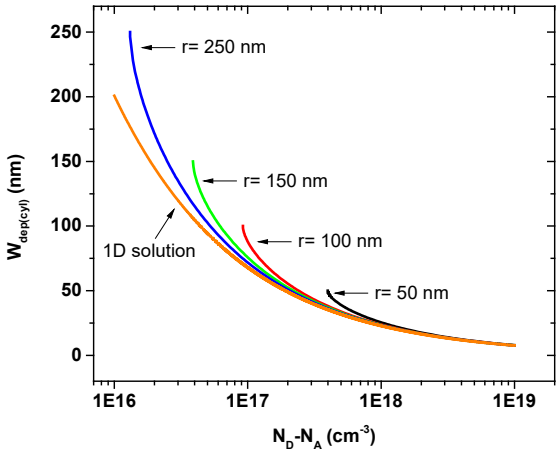

Figure 6.3: *Carrier depletion depth ($W_{dep(cyl)}$) of GaN NWs in* cylindrical coordinates *as a function of background electron concentration ($N_D - N_A$) for different NW radius (r). The1D solution of carrier depletion depth (W_{dep}) is also illustrated.*

6.3 Horizontal NW-devices of individual GaN nanowires

The GaN NWs were grown spontaneously [5] by PAMBE under N-rich conditions on bare Si (111) substrates (Fig. 6.4(a)) and selectively [6] at sites specified on masked SiO_2/Si (111) substrates (Fig. 6.4(b)). Their height and diameter ranged from 500 to 1900 nm and from 30 to 140 nm, respectively. Shorter (500-650 nm) and thicker (90 to 140 nm) GaN NWs were obtained in case of selective growth, while longer (1500-1900 nm) and thinner (30 to 98 nm) GaN NWs were obtained in case of spontaneous growth. In order to fabricate and characterize single NW devices, GaN NWs had to be released from their growth substrate. The suspension of GaN NWs onto SiO_2/ Si substrates was firstly studied and the results were employed for the fabrication of horizontal NW devices.

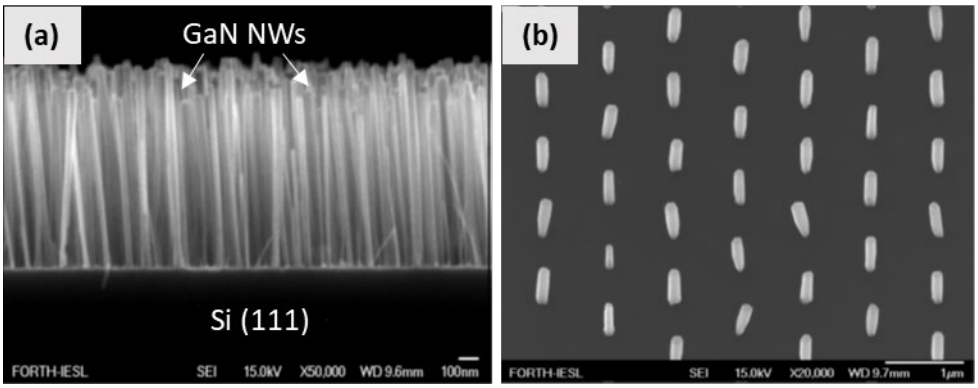

Figure 6.4: *Cross section and tilted SEM images of GaN NWs grown: (a) spontaneously on Si (111) substrates and (b) selectively on masked SiO_2/Si substrates, respectively.*

6.3.1 Suspension of GaN nanowires onto the SiO_2/Si substrate

The suspension of individual GaN NWs onto the SiO_2/Si substrate was achieved by applying the following process steps. Firstly, a piece of the sample with the as-grown GaN NWs (Fig.6.4) was placed in isopropyl alcohol solvent and afterwards the mixture was ultrasonically agitated for 30 min at 35 KHz. A suspension of GaN NWs in isopropyl alcohol was produced and dispersed with a pipette on 300 nm thermally grown, SiO_2 coated p-Si (111) substrate. The SiO_2/p-Si substrate was set on a hot plate at 110 °C during the dispersion of GaN NWs to enhance the evaporation of the solvent. By controlling the density of GaN NWs in the isopropyl alcohol solution, sparse (Fig. 6.5(a)) to dense (Fig. 6.5(b)) distributions of GaN NWs can be achieved.

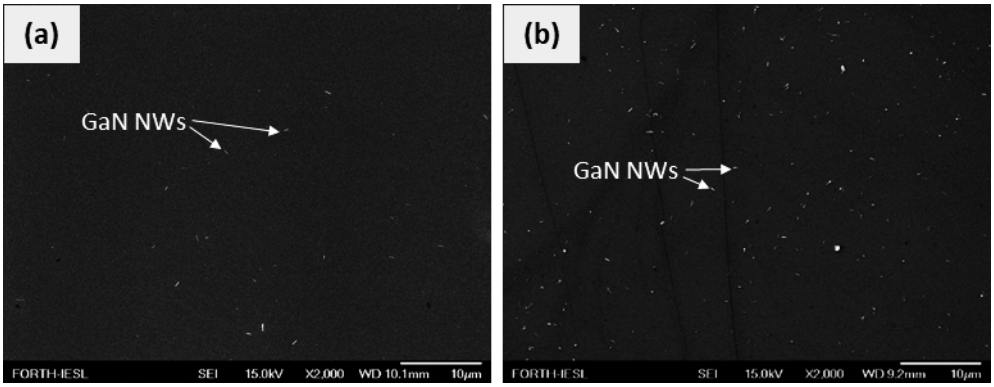

Figure 6.5: *SEM images of: (a) sparse and (b) dense* distributions of GaN NWs onto the SiO_2 coated p-Si (111) substrates.

The time that GaN NWs remain stored in isopropyl alcohol solvent, before the dispersion, is a critical point that had to be optimized. GaN NWs have to be immediately dispersed on the SiO_2/p-Si substrate after the ultrasonic agitation, otherwise an aggregation of GaN NWs will be observed on the SiO_2/p-Si substrate after the evaporation of the isopropyl alcohol solution (Fig. 6.6). This is mainly attributed to capillary

forces that take place in high aspect-ratio nanoparticles [15] and/or to probably poor solubility of GaN NWs in isopropyl alcohol solution [16]. This issue can be eliminated by applying an additional ultrasonic agitation (10 min, 35 kHz) to the solution with GaN NWs before every new dispersion.

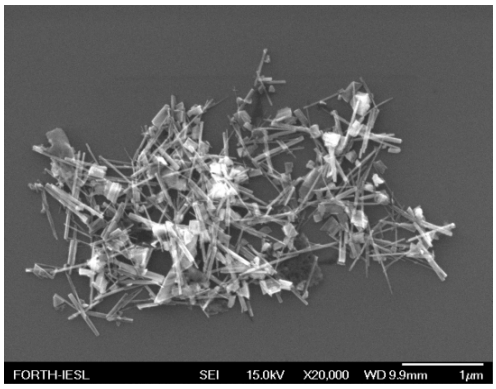

Figure 6.6: *Aggregation of GaN NWs* on the surface of a SiO_2/ Si substrate.

6.3.2 Fabrication of horizontal GaN nanowire devices

The fabrication of horizontal GaN NW devices started by formation of Cr/Au (5/100 nm) alignment marks, using e-beam evaporation on a 300 nm, thermally grown, SiO_2 coated p-Si (111) substrate. The metallic alignment marks covered the whole area of the substrate with a spacing of 200 μm (Fig. 6.7). Afterwards, spontaneously grown GaN NWs on Si (111) substrates and GaN NWs selectively grown on masked SiO_2/Si (111) substrates were sonicated and dispersed onto the SiO_2 /p-Si (111) substrate by following the procedure described in previous section (section 6.3.1). The precise positions (x,y) of these individual GaN NWs relating to a reference point (0,0) were determined by SEM. Then, ohmic contacts were defined by EBL and subsequently, Ti/Al/Ni/Au (15/85/15/20 nm) metals were deposited by e-beam evaporation on GaN NWs with diameters and lengths ranging from 30 to 140 nm and from 500 to 1900 nm, respectively. The fabrication was completed with the formation of pads for the metal contacts, by Cr/Au metallization on the SiO_2/ Si surface, followed by rapid thermal annealing (RTA) at 700 °C for 1 min. Consequently, RTA was not applied directly after the formation of ohmic contacts but postponed after the final fabrication step. The reason for this decision will be discussed in section 6.3.3.

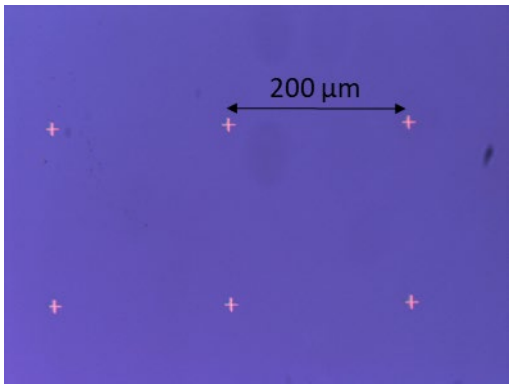

Figure 6.7: *Optical microscopy image of the metallic alignment marks.*

Two patterns were designed by EBL for the formation of the ohmic contacts. The first pattern is illustrated in Fig. 6.8(a) and shows an individual 45 nm diameter GaN NW with two metallic ohmic contacts at its edges, while Fig. 6.8(b) depicts with high magnification the corresponding GaN NW area. The total length of the spontaneously grown GaN NW is 1500 nm and the spacing between the contacts is equal to 600 nm. Hence, 450 nm in each side of GaN NW is totally covered by the ohmic metal. A misalignment error of 550 nm is also observed (Fig. 6.8(b)), as the NW is not positioned at the center of the contact metals. Precise stage movement and beam positioning are essential to minimize misalignment EBL errors, which in case of nano-dimensional structures are very critical [17]. However, it is not critical for the scope of this structure shown in Fig. 6.8(b).

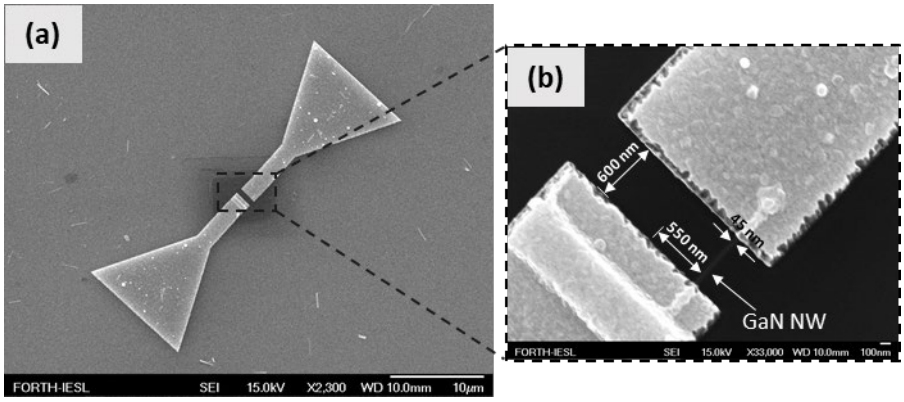

Figure 6.8: *SEM images of the contact pattern used for ohmic contacts on individual horizontal NWs: (a) after the formation of the ohmic contacts and (b) the area of the GaN NW, in high magnification.*

The finally fabricated horizontal GaN NW device after the deposition of Cr/Au metal pads and interconnects, is illustrated in Fig. 6.9. The final pads (Fig. 6.9) have dimensions of 150 x 150 nm and are compatible with I-V characterization equipment.

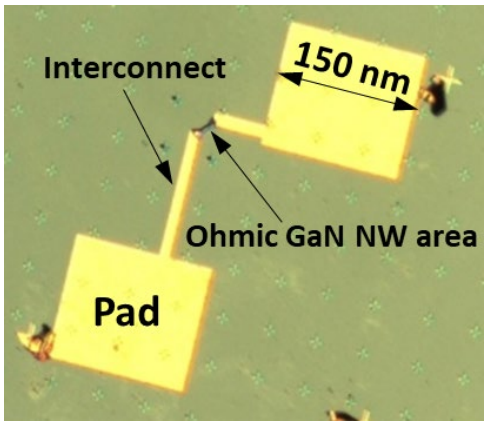

Figure 6.9: *Optical microscopy image with the finally fabricated horizontal GaN NW device.*

Misalignment errors was the main issue in fabrication of these devices and a different methodology had to be developed in order to fabricate devices from GaN NWs grown on masked SiO_2/Si (111) substrate, due to their shorter lengths (500 - 650 nm) in the range of the reported misalignment error. There were two options: the first concerns a way to reduce misalignment errors during EBL and the second the use of a pattern with higher tolerance in misalignment issues.

For the first option, alignment marks with reduced spacing (50 μm) were deposited on SiO_2/Si substrates but the results were not encouraging. A new optimized pattern (Fig. 6.10) was then designed consisting of 14 parallel Ti/Al/Ni/Au (15/85/15/20 nm) metal stripes with width of 180 nm and spacing of 120 nm. The total length of the metal stripes varied from 3 μm to 9.5 μm, while a small interconnect pad (2 μm x 2 μm) was designed at the edge of each metal stipe (Fig. 6.10), allowing the final interconnection with bigger Cr/Au pads (100 μm x 100 μm). A very dense array of this pattern with a pitch of 5 μm was also deposited to cover a certain area of the SiO_2/Si surface with the sparse dispersion of GaN NWs on top. The main idea was that a certain number of GaN NWs will be "caught" by the metal contacts with this random deposition.

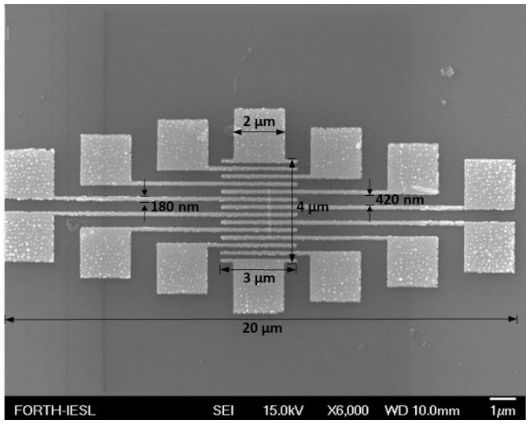

Figure 6.10: *SEM image of the new ohmic pattern, consisting of 14 parallel metal stripes with width of 180 nm and spacing of 120 nm.*

Figure 6.11 shows SEM images of fabricated horizontal GaN NW devices with multiple ohmic contacts per NW and varied spacing between contacts, depending on the position/alignment of GaN NWs. A well-aligned GaN NW with 92 nm diameter and 7 ohmic contacts in a length of 1900 nm, is illustrated in Fig. 6.11(a). Random aligned horizontal GaN NW devices with diameters of 35 (Fig. 6.11(b)), 72 (Fig. 6.11(c)) and 98 nm (Fig. 6.11(d)) and corresponding lengths of 1400 nm (4 contacts), 1500 nm (4 contacts) and 1600 nm (3 contacts), respectively, are also illustrated (Figs. 6.11(b) - 6.11(d)). This EBL pattern was successfully used for fabrication of horizontal GaN NW devices, with 2 ohmic contacts, from NWs grown on patterned SiO_2/Si substrates (Fig. 6.11(e)). The GaN NW of Fig. 6.11(e) had a conical shape with 550 nm length and diameter varying from 90 to 140 nm, as shown at higher magnification in Fig. 6.11(f).

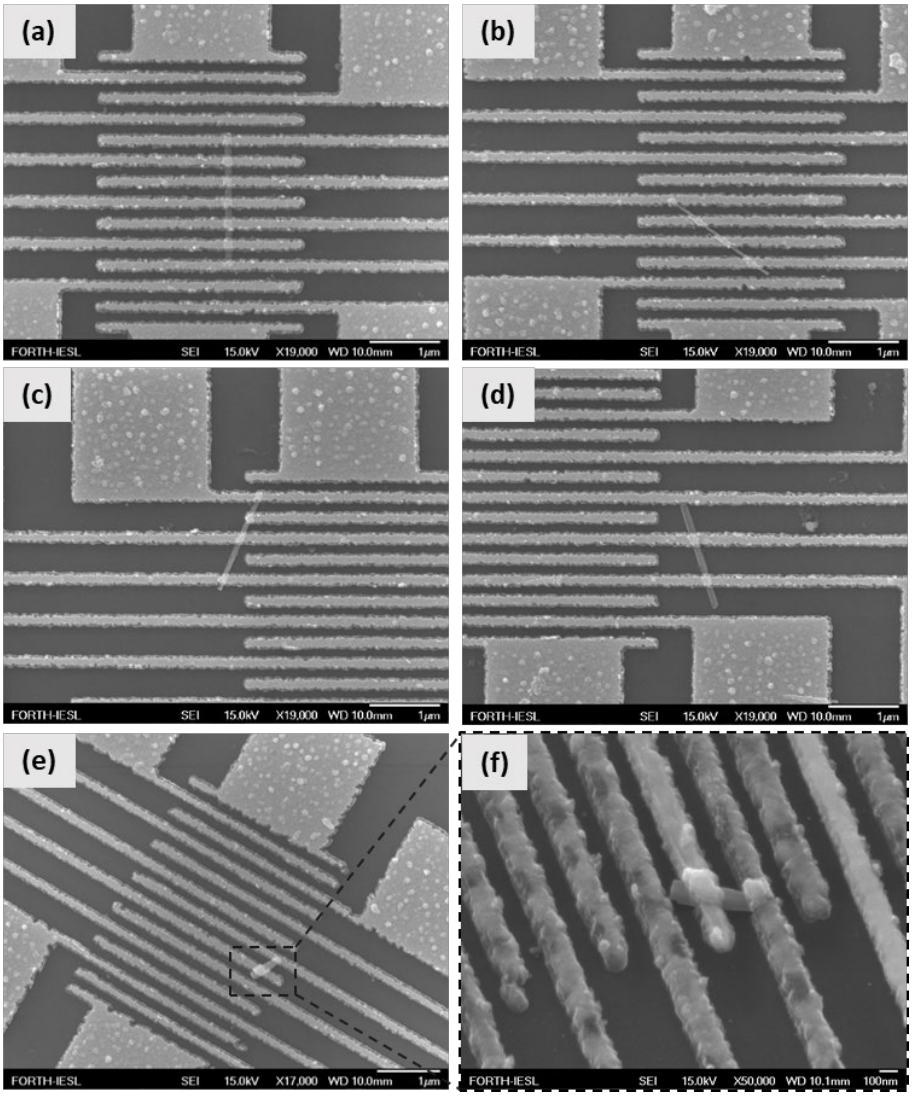

Figure 6.11: *SEM images of* fabricated horizontal GaN NW devices: with spontaneously grown GaN NWs with length and diameter of: (a) 1900 and 92 nm, (b) 1400 and 35 nm, (c) 1500 and 72 nm, (d) 1600 nm and 98 nm, respectively, and (e) with a selectively grown GaN NW with length of 550 nm and diameter varying from 90 to 140 nm, (f) a higher magnification image of the area of the GaN NW present in (e).

The final interconnection with bigger metal contact pads was achieved by EBL and subsequently, Cr/Au metallization on the SiO_2/ Si surface. The Cr/Au interconnects were used to connect the small pad (2 μm x 2 μm) of each metal stripe that includes a single contact with a GaN NW, with a new simultaneously deposited bigger (100 μm x 100 μm) Cr/Au pad (Fig. 6.12). Figure 6.12(a) and Fig. 6.12(b) show SEM pictures with 2 and 5 interconnections with such bigger contact pads, respectively, while Fig. 6.12(c) shows an optical microscopy image of the finally fabricated design, providing ohmic contacts to over 25 horizontal GaN NWs.

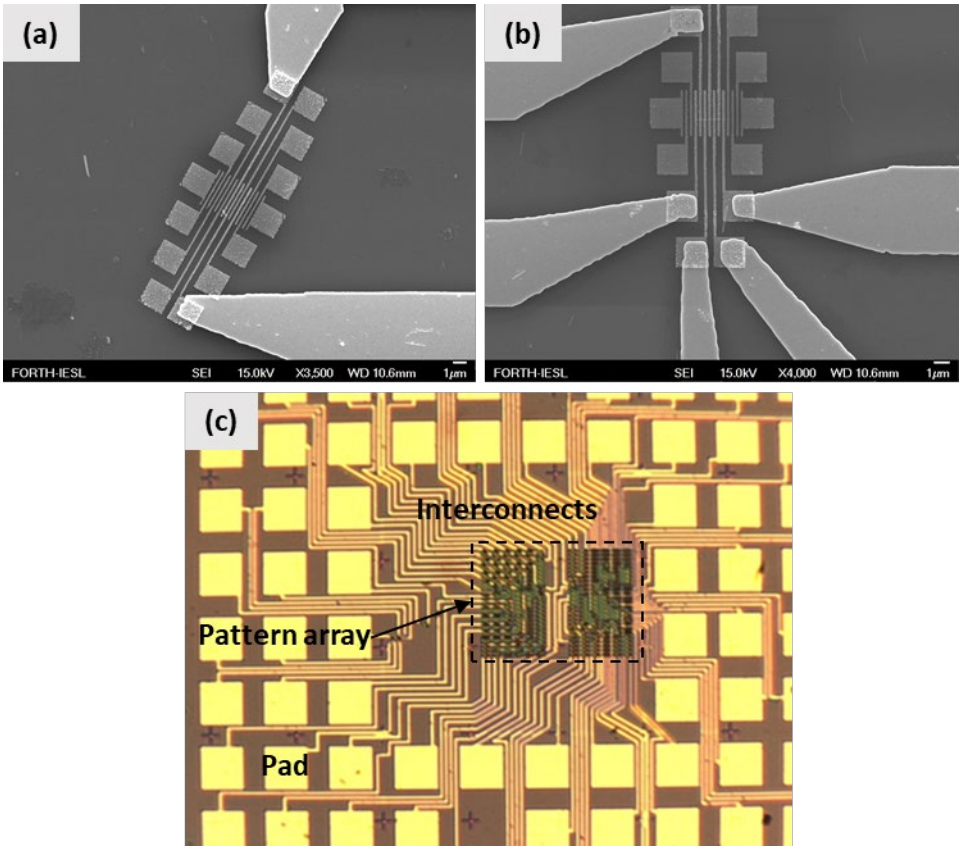

Figure 6.12: *SEM images of horizontal GaN NW devices with: (a) 2 and (b) 5 final metal interconnections with bigger contact pads and (c) optical microscopy image of the finally fabricated design, providing ohmic contacts to over 25 horizontal GaN NWs.*

Parasitic resistances induced by metal interconnects and pads may affect the device performance [18–19], if their value is comparable with the resistance of GaN NWs. In order to address this issue a "short circuited" design of Fig. 6.13 was also deposited on the SiO_2/Si substrate, simultaneously with the formation of the correct one that contained the GaN NWs (Fig. 6.12(c)). This test design contains the Cr/Au interconnects and pads of the original one (Fig. 6.13(a)) up to the point that the interconnects end up to the small pads (Figs. 6.13(b)). At this point, the interconnects were short circuited instead to leaving a free area for the positioning of GaN NWs, as illustrated in the higher magnification optical microscopy image of Fig. 6.13(c).

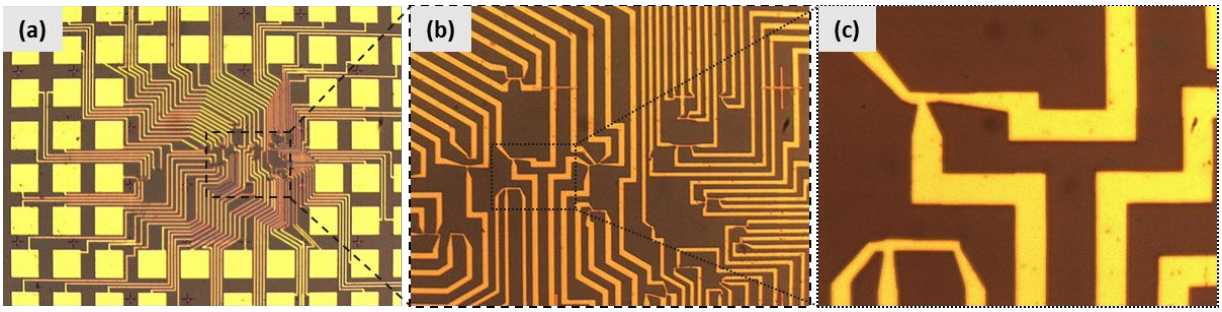

Figure 6.13: *Optical microscopy images of "short circuited" test structures with: (a) the overall design of the pattern, (b) the area of interconnects in higher magnification and (c) even higher magnification image of the area where GaN NWs should be present in the correct contact pattern.*

6.3.3 Results and discussion

The fabricated horizontal GaN NW devices were characterized by DC Current-Voltage (I–V) measurements using a Keithley 4200 semiconductor characterization system, in order to identify the conductivity of GaN NWs and the dependence on their diameter and growth conditions. I-V measurements were initially made for horizontal GaN NW devices before the RTA step (section 6.3.2). In this case, I-V results didn't show ohmic behavior, as expected for low conductivity undoped GaN NWs.

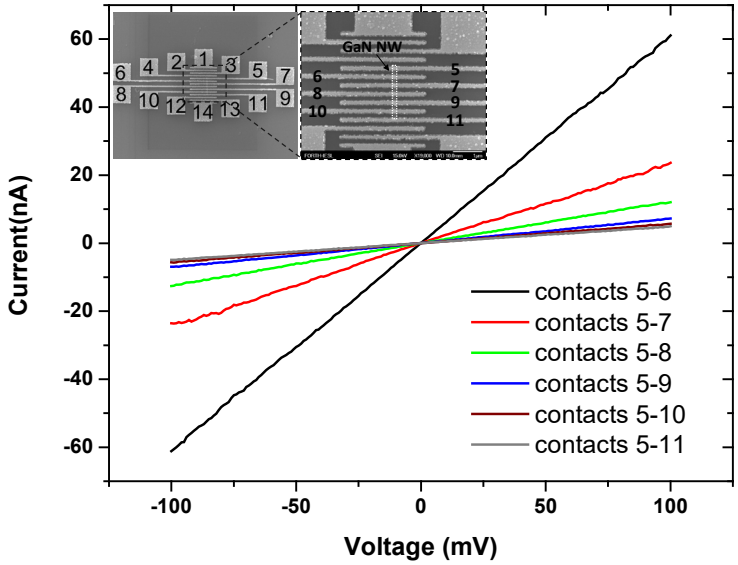

Figure 6.14: *I-V characteristics, after annealing, of a single GaN NW device with 7 ohmic contacts along a GaN NW with 1900 nm length and 92 nm diameter. The insets show the conventional numbering of metal stripes.*

After annealing, GaN NWs with diameters larger than 90 nm exhibited ohmic I-V behavior, while GaN NWs with diameters less than 75 nm were not conductive. As there

were no fabricated devices with diameters of GaN NWs in the range of 75 to 90 nm, the critical GaN NW diameter, as described in section 6.2, is expected to have a value in this range. This means that the electron concentration in the NW is expected to be in the range of 4.97 x 10^{17} to 7.30 x 10^{17} cm^{-3} (Fig. 6.2).

Figure 6.14 depicts the I-V characteristics after the RTA step, of a fabricated horizontal GaN NW device, consisting of 7 ohmic contacts with 180 nm width and 120 nm spacing, along a GaN NW with 1900 nm length and 92 nm diameter. The insets in Fig. 6.14 show SEM images of the fabricated GaN NW device. Using different pairs of contact fingers (no 5-11), allowed to carry I-V measurements for different lengths of the same NW: 120 nm (between contacts 5&6), 420 nm (between contacts 5&7), 720 nm (between contacts 5&8), 1020 nm (between contacts 5&9), 1320 (between contacts 5&10) and 1620 nm (between contacts 5&11). These I-V measurements are shown in Fig. 6.14. The slope of each I-V curve represents the resistance (R_{NW}) of a certain length of GaN NW (corresponds to a certain contact finger distance), as:

$$I = \frac{1}{R_{NW}} V \quad (6.8)$$

The apparent GaN NW resistivity is calculated by [20]:

$$\rho = \frac{R_{NW} \pi r^2}{l} \quad (6.9)$$

The calculated resistances and the corresponding apparent GaN NW resistivity, for all the different NW contact distances of the above GaN NW are given in Table 6.1:

TABLE 6.1: Calculated resistances and corresponding resistivity values for different lengths between contacts of the horizontal GaN NW.

Contacts	*Length (nm)*	*Resistance (MΩ)*	*Resistivity (Ωcm)*
5-6	120	1.43	7.92
5-7	420	4.67	7.39
5-8	720	8.11	7.48
5-9	1020	11.92	7.76
5-10	1320	14.87	7.42
5-11	1620	17.52	7.19

The overall fabricated horizontal GaN NW devices, for GaN NWs spontaneously grown on Si (111) substrates with diameters larger than 90 nm, exhibited after annealing ohmic behavior and apparent room temperature resistivity (ρ) in the range of 6-9 Ωcm using Eq. 6.9. GaN NWs selectively grown on SiO_2/Si substrates with conical shapes and diameters ranging from 90 to 140 nm exhibited ohmic behavior and ρ in the range of 8 x 10^{-2} to 1.2 x 10^{-1} Ωcm, by assuming an average diameter for the measured NW length. This significant difference of the resistivity results cannot be attributed to different carrier concentrations due to the growth process but rather to the existence of a critical diameter (d_{crit}) for full depletion of GaN NWs (section 6.2). In order to calculate the d_{crit} from Eq. 6.3, an estimation of the doping concentration (N_D) inside the undoped GaN NWs is necessary.

According to Benner O. et al. [20], an estimation of N_D can be carried out by the following analysis. N-type behavior is expected in nominally undoped GaN NWs according to literature reports [10–11] and the following formula can be used for the calculation of the resistance of n-GaN NWs [20]:

$$R_{NW} = \frac{l}{q\mu_{GaN} N_D A_{eff}} \quad (6.10)$$

where μ_{GaN} is the electron mobility of GaN as a function of doping concentration (N_D) and A_{eff} is the effective cross sectional area of the GaN NW due to surface depletion, given by:

$$A_{eff} = \pi\left(r - W_{dep}\right) \quad (6.11)$$

The Hilsum equation may be used for the calculation of μ_{GaN} [20–21]:

$$\mu_{GaN} = \frac{\mu_o}{\sqrt{0.25 + \frac{N_D}{10^{17} cm^{-3}}}} + 20\frac{cm^2}{Vs} \quad (6.12)$$

and the estimated A_{eff} by assuming the one-dimensional case for the depletion width W_{dep} (Eq. 6.1) is given by [20]:

$$Aeff = \pi\left(r - \sqrt{\frac{2\varepsilon\left(q\Phi_b - KT\ln\frac{N_C}{N_D - N_A}\right)}{q^2\left(N_D - N_A\right)}}\right) \quad (6.13)$$

The R_{NW} is then given by (Eqs. 6.10- 6.13):

$$R_{NW} = \frac{l}{qN_D\pi\left(\frac{\mu_o}{\sqrt{0.25+\frac{N_D}{10^{17}}}}+20\right)\left(r-\sqrt{\frac{2\varepsilon\left(q\Phi_B - KT\ln\frac{N_C}{N_D-N_A}\right)}{q^2\left(N_D-N_A\right)}}\right)^2} \quad (6.14)$$

A graphical solution of GaN NW resistance per NW length (R_{NW}/l) as a function of NW radius (r) is plotted in Fig. 6.15 for 4 fixed values of N_D (5.2 x 10^{17}, 5.3 x 10^{17}, 5.4 x 10^{17} and 5.5 x 10^{17} cm^{-3}), by assuming μ_o= 440 cm^2/Vs [20] and Φ_B = 0.55 eV [20]. In Fig. 6.15 the corresponding experimental R_{NW}/l values are also depicted. Comparing the measured values to the modeled data, an estimated N_D ranging from 5.0 x 10^{17} to 5.5 x 10^{17} cm^{-3}, can be identified. Then, from Eq. 6.3, a d_{crit} of 89.8 and 85.8 nm is calculated for N_D = 5.0 x 10^{17} cm^{-3} and N_D = 5.5 x 10^{17} cm^{-3}, respectively. By assuming an average critical diameter (d_{crit}) of 87 nm, the effective diameter (d_{eff}) of conductive GaN NW is given by:

$$d_{eff} = d_{NW} - d_{crit} = d_{NW} - 87nm \quad (6.15)$$

By using in Eq. 6.9 the value of d_{eff} instead of the nominal diameter (r) of GaN NW, a room temperature resistivity in the range of 0.015 to 0.030 Ωcm and 0.010 to 0.020 Ωcm, is calculated for GaN NWs spontaleously grown on Si (111) substrates and selectively grown on SiO_2/Si substrates, respectively. The values now are in a good agreement, which confirms the great influence of surface states in GaN NW conductivity. According to Benner O. et al. [20], the electron mobility of GaN NWs for N_D in the range of 5.0 x 10^{17} to 5.5 x 10^{17} can also be estimated from Eq. 6.12 and an average value of 205 cm^2/Vs, is identified.

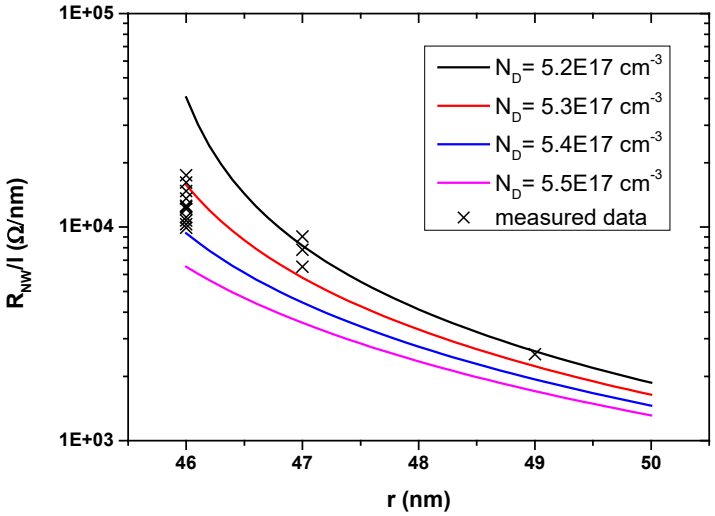

Figure 6.15: *Simulated and experimental plots of GaN NW resistance per NW length (R_{NW}/l) as a function of NW radius (r) for 4 fixed values of N_D used for simulations.*

In conclusion, horizontal GaN NW devices consisting of GaN NWs spontaneously grown on Si (111) substrates and selectively grown on SiO_2/Si (111) substrates with heights and diameters ranging from 500 to 1900 nm and from 30 to 140 nm, respectively, were fabricated. An optimized ohmic contact pattern with 14 parallel Ti/Al/Ni/Au metal stripes (finger contacts) was used to eliminate misalignment errors induced by EBL. The random array deposition of this pattern resulted to an easy and fast way to fabricate horizontal GaN NW devices. Surface states on the GaN NWs induce Fermi level pinning at their lateral surface and thus a carrier depletion inside the GaN NW. A critical GaN NW diameter (d_{crit}) of ~87 nm for full depletion (punch through) of GaN NW was calculated, in agreement with the experimental observations. The doping concentration (N_D) and electron mobility (μ_{GaN}) of GaN NWs were estimated with an average value of 5.2 x 10^{17} cm^{-3} and 205 cm^2/Vs, respectively. A room temperature resistivity in the range of 0.01 to 0.03 Ωcm, in agreement with other literature reports [22–23], was also estimated for the overall GaN NWs by using an effective diameter (d_{eff}) in calculations.

6.4 Vertical p-Si/n-GaN NW heterojunction diodes

The GaN NWs were grown spontaneously by PAMBE under N-rich conditions on bare 1-10 Ωcm p-Si (111) substrates. The average height and diameter of GaN NWs was 800 nm and 50 nm, respectively. Characterization of individual GaN NWs indicated n-type behavior with doping concentration (N_D) in the range of 5.0 x 10^{17} to 5.5 x 10^{17} (section 6.3). Thus, n-GaN NWs grown on a p-Si substrate is expected to form a p-n heterojunction. The p-Si/n-GaN NW junction could provide fundamental information for the GaN/Si heterojunction formation but it is also interesting for integrating GaN NW solar cells and light emission devices on Si.

6.4.1 Fabrication of p-Si/n-GaN NW heterojunction diodes

The fabrication of devices started with the spin coating of a Polymethyl methacrylate (PMMA) resist. The PMMA resist with 1.5 μm thickness was spun to completely cover the NWs. Then it was exposed to DUV for 50 sec and developed at Methyl isobutyl ketone: Isopropyl alcohol (MIBK:IPA) solution with a ratio of 1:3 to remove the resist from the top 200 nm part of GaN NWs, as shown in Fig. 6.16(a). Afterwards, Ti/Al/Ni/Au ohmic metals were deposited by e-beam evaporation using a metallic mask consisting of circular patterns with diameters of 190 and 380 μm. During this step, ohmic metals were deposited only on the top part of GaN NWs forming the cathode contact. The back side of p-Si substrate was entirely covered with Al for the anode ohmic contact formation [24]. A cross sectional view of the final fabricated p-Si/n-GaN NW heterojunction diode is illustrated in Fig. 6.16(b).

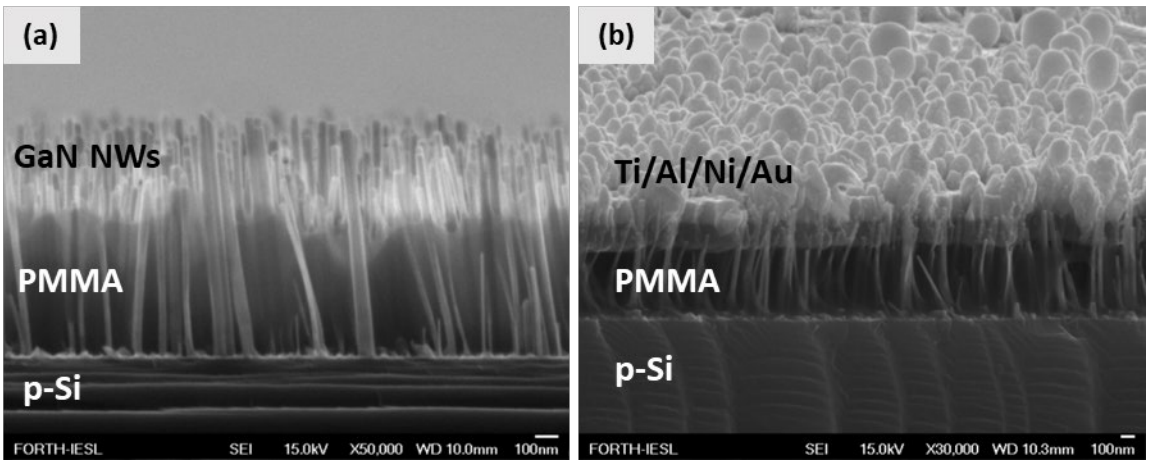

Figure 6.16: *SEM images in cross sectional view showing the process flow for vertical p-Si/n-GaN NW heterojunction diodes after: (a) the removal of PMMA resist from the 200 nm top part of GaN NWs and (b) the final fully-processed vertical device.*

6.4.2 Results and discussion

The fabricated devices were characterized by DC I–V measurements using a Keithley 4200 semiconductor characterization system. An issue occurred during these measurements, was that the typical straight tungsten probe/needle [25] of the I-V measurement equipment removed the metal contacts (Fig. 6.17(a)) and the GaN NWs (Fig. 6.17(b)) of the heterojunction diode, due to the existence of the "soft" PMMA resist as anode to cathode insulator spacer (Fig. 6.16). In order to eliminate this problem, a probe with a tungsten wire crimped into a nickel plated copper [26] was used to allow flexing of tungsten wire without damaging the device.

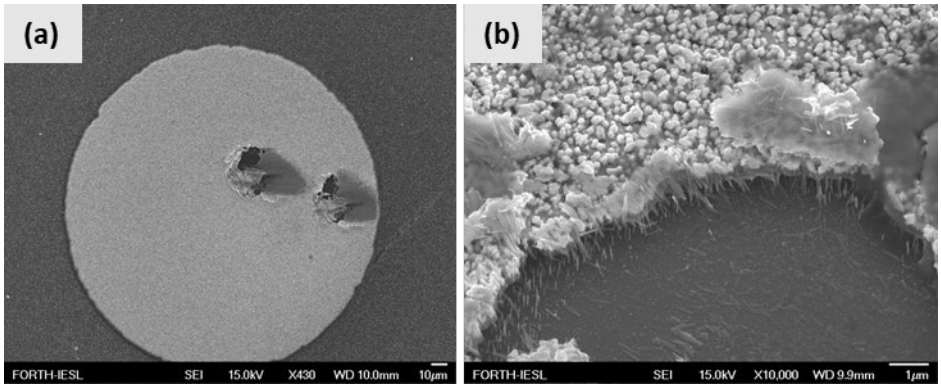

Figure 6.17: *SEM images of fabricated p-Si/n-GaN NW heterojunction diodes after I-V measurements, showing the removed (a) metal contacts and (b) GaN NWs.*

Figure 6.18 depicts the current density-voltage (J-V) characteristics in linear (Fig. 6.18(a)) and logarithmic scale (Fig. 6.18(b)) of a fabricated vertical p-Si/n-GaN NW

heterojunction diode with diameter of 180 μm. The current density has been calculated by using the formula:

$$J = \frac{I}{x\pi r^2} \quad (6.16)$$

where I is the measured current of the device, *r* the diameter of the diode and x the percentage of area coverage with GaN NWs (0.85 in our case).

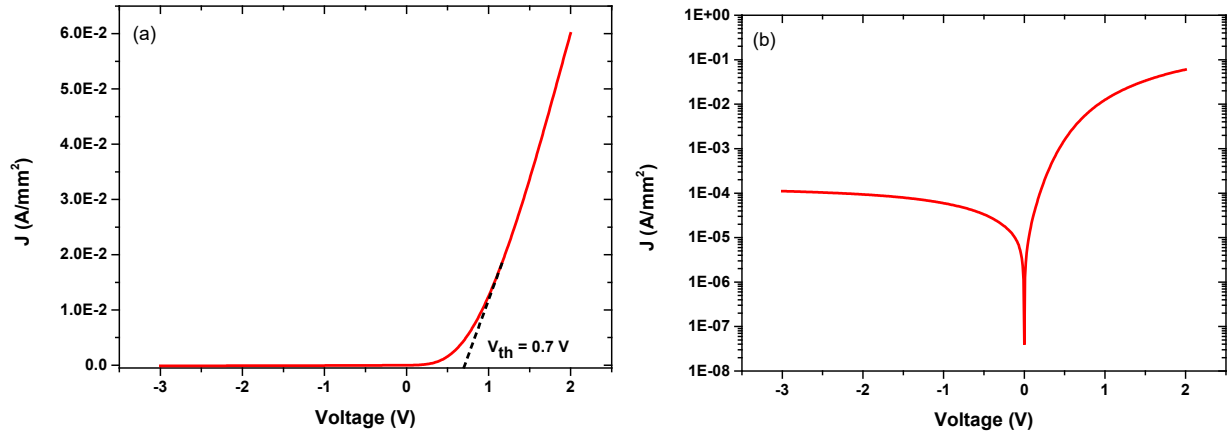

Figure 6.18: *J-V characteristics in (a) linear and (b) logarithmic scale of a fabricated vertical p-Si/n-GaN NW heterojunction diode with diameter of 180 μm.*

The junction is forward biased for positive voltage applied to p-Si substrate (anode) and exhibits a clear rectifying behavior, although a non-optimized fabrication process was used. A maximum current density of 6.0 x 10^{-2} A/mm^2 is observed at V= 2V. The threshold voltage (V_{th}) of the p-n heterojunction is 0.7 V (Fig. 6.18(a)), while the ratio of forward to reverse current density (J_F/J_R) at $|V| = 2$ V is equal to 10^3. The V_{th} is defined as the voltage bias intercept of the linear extrapolation of J to 0 A/mm^2. These results are considered indicative for the potential to explore the p-Si/n-GaN NW heterojunction as active device junction in device applications. The p-type Si could offer the holes that are difficult to create in GaN layers and the GaN NWs provide the defect-free GaN crystal that is impossible to realize by heteroepitaxial growth of planar GaN on Si.

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Chapter 7

Top-down AlN/GaN/AlN MOS-FinHEMTs

7.1 Introduction and motivation

The polarization discontinuity at the $Al_xGa_{1-x}N$/GaN [1] or $In_xAl_{1-x}N$/GaN [2] heterointerface induces a high density two-dimensional electron gas (2DEG) that provides the channel of high electron mobility transistors (HEMTs). The highest 2DEG density is achieved with pure AlN barrier [3–4] and thus AlN/GaN HEMTs are the ultimate device structures for high-power and high-frequency applications [5–6].

The AlN/GaN single barrier heterostructure requires the initial growth of a GaN buffer layer [7] with a thickness of 2-4 μm to reduce the threading dislocation density in the GaN channel. However, the growth of an unintentionally doped GaN buffer layer with a background electron concentration of 10^{16} cm^{-3} [8] results to the formation of an undesirable leakage path in the GaN buffer layer underneath the 2DEG channel, while the growth of a semi-insulating p-doped GaN buffer layer [9–10] induces deep-level traps and defects [9–10]. Hence the AlN/GaN/AlN double heterostructure is preferable for efficient carrier confinement in the channel, due to the large band discontinuity and the large negative polarization charge at the bottom GaN/AlN interface that raises the conduction band and depletes the bottom part of the GaN layer [11–12] . The grown AlN back layer also exhibits high resistivity, without the need to incorporate dopants for introducing electron trapping deep levels.

The difficulties in fabrication of horizontal GaN-based single NW devices, as presented in chapter 6, shifted our interest to a top-down approach for the formation of fin-shaped GaN-based structures (section 5.3.3) that could support the design of GaN-based FinHEMTs for either low-power (digital) or high-power applications. Field effect transistors (FETs) with tri-gate around a fin-shaped channel (FinFETs) enable enhanced electrostatic control of the gate on the channel that could result to significant improvement of leakage current and current on/off ratio, in comparison to planar gate devices.

The advantages of the FinFET device configuration have been exploited also in AlGaN/GaN [13–16] and AlN/GaN [13] HEMT structures (FinHEMTs), where the fin channel geometry is particularly attractive as an approach to realize normally-off GaN power transistors, due to positive shift of the threshold voltage by reducing the fin width (W_{fin}) [14–19]. However, in Ref. [20] the threshold voltage exhibited a negative shift by reducing the W_{fin}. The reported results have also revealed significant inconsistencies in the comparative maximum drain-source current ($I_{ds,max}$) and transconductance ($g_{m,max}$) per top gate width (W_g) of FinHEMT and planar HEMT devices, fabricated from the same structure. The larger $I_{ds,max}/W_g$ and $g_{m,max}/W_g$ values were exhibited by FinHEMTs in Refs. [13], [16] and [21]. In contrast, in Refs. [19–20] and [22–23] the planar HEMTs displayed

higher values, while in Ref. [24] the same values were observed for both types of device. For the only reported case of AlN/GaN HEMT structure [13], the FinHEMT device exhibited 2.5 times larger $I_{ds,max}/W_g$ compared to the planar HEMT, although Schottky-like source and drain contacts were reported (the I_{ds} was nearly zero for drain-source voltage up to 2-3V). The effect of different W_{fin} on $I_{ds,max}/W_g$ has been described in few works related to AlGaN/GaN FinHEMT devices [16, 17, 19], that show a reduction of $I_{ds,max}/W_g$ with decreasing W_{fin} in the range of 60-210 nm, which becomes less evident for the wider fins.

This chapter presents a thorough experimental and device simulation investigation for understanding and predicting the DC characteristics of FinHEMT devices based on an AlN/GaN HEMT structure with AlN back barrier. Experimental work includes the fabrication of test FinHEMT devices with metal-oxide-semiconductor (MOS) tri-gate based on Al_2O_3 dielectric (MOS-FinHEMTs) starting from a planar AlN/GaN/AlN double barrier heterostructure (top-down approach). The transistor channel consists of a single-fin with width (W_{fin}) of 200, or 350, or 500 or 650 or a multi-fin (n= 70) with W_{fin}= 200 nm. The experimental results were compared to three-dimensional (3D) device simulations of the single-fin MOS-FinHEMTs, taking into account also strain relaxation of the top AlN barrier. Extension of the device simulations to narrower W_{fin} of 50, 20 and 10 nm was employed to identify W_{fin} conditions for normally off operation. In addition, simulations were used to predict the effects of different device parameters for a fixed W_{fin} value. The results provide valuable insight for the dependence of the threshold voltage (V_{th}) and maximum drain-source current ($I_{ds,max}$) on the fin width (W_{fin}), as well as the effects of drain and source contact resistance, gate-drain and source-gate distance and of the Al_2O_3 gate dielectric thickness (t_{ox}). Processing issues were also identified for optimized device fabrication.

7.2 Polarization effects in AlN/GaN/AlN heterostructures

The AlN/GaN/AlN heterojunction [11–12] induces an energy barrier at the bottom interface of the GaN/AlN heterojunction, due to the polarization difference between the channel and the back barrier. The main benefit of this barrier is the limitation of the electron penetration into the buffer layer under high bias operation, by lifting upward the conduction band below the channel [26–27] , which can result to enhanced device performance with limited sub-threshold drain leakage currents and increased breakdown voltages [26–27].

Simulations of AlN/GaN/AlN heterostructures were performed by using Silvaco Atlas software and a 2D self-consistent Schrödinger-Poisson model to determine the equilibrium energy band profiles and carrier distributions of the HEMT structures. The calculations employed the material properties listed in Table 7.1 [28–29]. For the boundary conditions, the energy difference (E_C-E_F) between E_C and E_F at the GaN surface (surface potential) was set at 1 eV, while neutrality (flat bands) was considered at the

bottom (AlN) side. The donor concentrations of $N_D=10^{13}$ cm^{-3} for AlN and $N_D=10^{16}$ cm^{-3} for GaN, were assumed, considering the typical electron concentration of undoped GaN epilayers and the high resistivity exhibited by AlN epilayers [8, 28, 29].

TABLE 7.1: Material properties (bandgap, effective electron masses in the growth and perpendicular to the growth direction, lattice constant and polarization parameters) used in simulations [Refs. 28 and 29]

	GaN	*AlN*
E_g @300K (eV)	3.42	6.28
$m_{e,l}^*/m_0$	0.18	0.25
$m_{e,t}^*/m_0$	0.20	0.33
α_0 (*Å*)	3.189	3.112
e_{33} (C/m^2)	0.67	1.50
e_{31} (C/m^2)	-0.34	-0.53
P_{sp} (C/m^2)	-0.034	-0.09

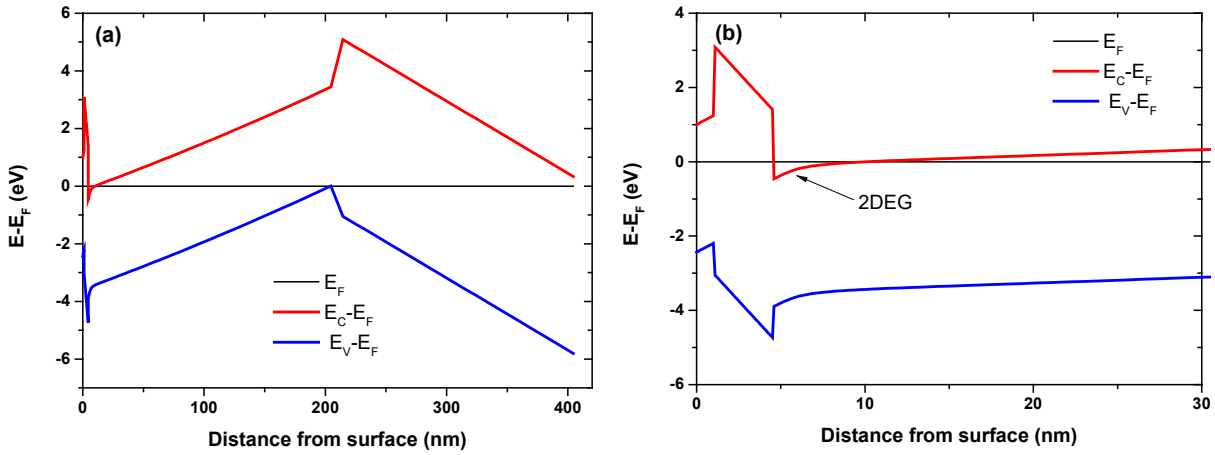


Figure 7.1: *Simulated band diagram profile of an AlN/GaN/AlN (1 nm GaN cap / 3.5 nm AlN / 200 nm GaN / 200 nm AlN) heterostrucfore for: (a) the entire range of the structure and (b) the first 30 nm region of the structure.*

The simulated band diagram profile of an AlN/GaN/AlN metal-face (0001) heterostructure consisting (from top-surface to bottom-substrate) of 1 nm GaN cap / 3.5 nm AlN / 200 nm GaN / 200 nm AlN, is illustrated in Fig. 7.1(a) for the entire structure. The bottom GaN/AlN interface induces a strong electric field within the 200 nm GaN buffer layer and thus a large barrier (back barrier) for electron motion toward the substrate (Fig. 7.1(a)). Figure 7.1(b) shows an expanded view of the corresponding band diagram profile with high magnification for the first 30 nm region, where the 2DEG quantum well is

formed at the AlN/GaN interface. The electron concentration profile of the structure, which is mainly attributed to 2DEG, is shown in Fig. 7.2. A 2DEG sheet carrier density of 3 x 10^{13} cm^{-2} was estimated by integrating the curve of electron concentration over the distance from surface (x-axis) range (Fig. 7.2).

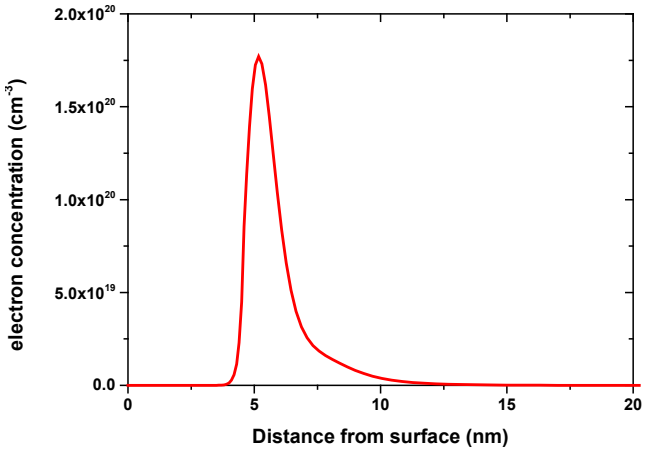


Figure 7.2: *Simulated electron concentration profile of the AlN/GaN/AlN (1 nm GaN cap / 3.5 nm AlN / 200 nm GaN / 200 nm AlN) heterostructure.*

7.3 Epitaxial growth and material characterization

The AlN/GaN/AlN metal-face (0001) heterostructure consisted (from top to bottom) of 1 nm GaN cap / 3.5 nm AlN / 200 nm GaN / 30 nm AlN, grown by plasma assisted molecular beam epitaxy (PAMBE) on a 1µm AlN (0001) buffer layer, previously grown on sapphire (0001) substrate by metalorganic vapor phase epitaxy (MOVPE). A 2DEG density of 1.6 x 10^{13} cm^{-2} and electron mobility of approximately 750 cm^2 V^{-1} s^{-1} have been determined by conductivity and Hall-effect measurements in a similar heterostructure of previous work [11–12]. The structural quality of the sample was evaluated by high resolution X-ray diffraction (HR-XRD) and room temperature photoluminescence (PL) measurements, respectively. The PL spectra were measured using He-Cd continuous wave (CW) laser excitation at 325 nm wavelength.

The HR-XRD ω-2theta scan measurements suggested high crystal quality of the 200 nm GaN epilayer, exhibiting a full width at half maximum (FWHM) of 207 arcsec for the (0002) reflection (Fig. 7.3(a)) and 900 arcsec for the (10-15) reflection measured in skew geometry. The lattice constants of the GaN layer c = 5.208 Å and a= 3.166 Å were determined by HR-XRD, using the extended Bond method and indicate that the GaN layer is under compressive in-plane strain of 7.2 x 10^{-3} [30]. This corresponds to relaxation of 70% of the misfit strain of GaN on AlN (0001). The room temperature PL measurements exhibited a strong band edge emission at 3.434 eV from the GaN layer, as shown in Fig. 7.3(b). This value is blue shifted with respect to the strain free value of 3.425 eV due to

compressive stress. The narrow PL FWHM value and the absence of yellow luminescence indicate a low crystal defect density [31].

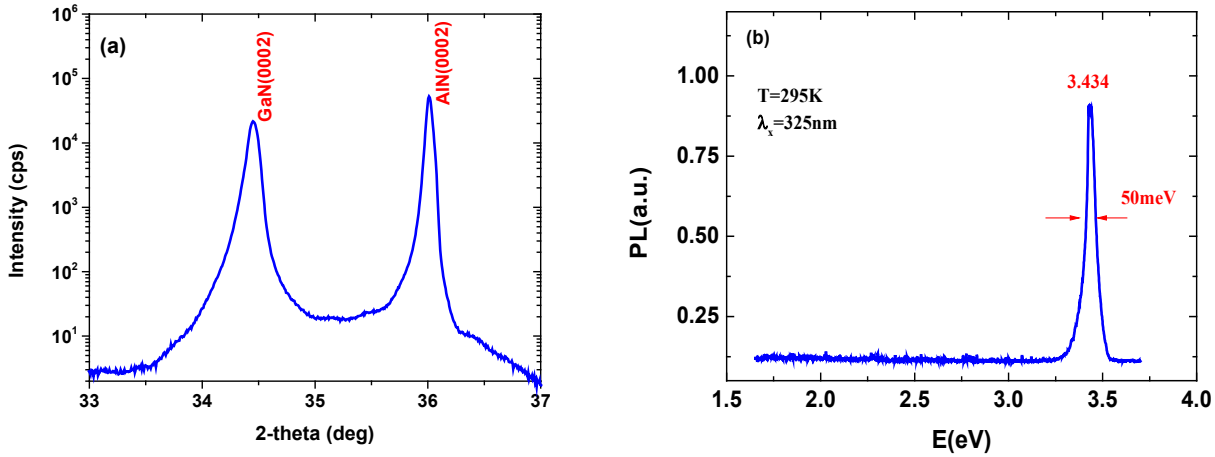


Figure 7.3: *Material characterization of the AlN/GaN/AlN heterostructure: (a) HR-XRD ω-2theta scan and (b) room temperature photoluminescence (PL) measurement using excitation at 325 nm.*

7.4 Device fabrication

Single-fin AlN/GaN/AlN MOS-FinHEMTs with fin widths (W_{fin}) of 200, 350, 500 and 650 nm, multi-fin (n= 70) AlN/GaN/AlN MOS-FinHEMTs with W_{fin}= 200 nm and conventional MOS-HEMTs with planar gate width W = 45 μm, were fabricated. The MOS gate dielectric was high quality Al_2O_3, deposited by atomic layer deposition (ALD). The schematic of Fig. 7.4(a) shows the overall configuration of the fabricated single-fin AlN/GaN/AlN MOS-FinFET and the corresponding gate structure is clarified in the device cross-section schematic of Fig. 7.4(b).

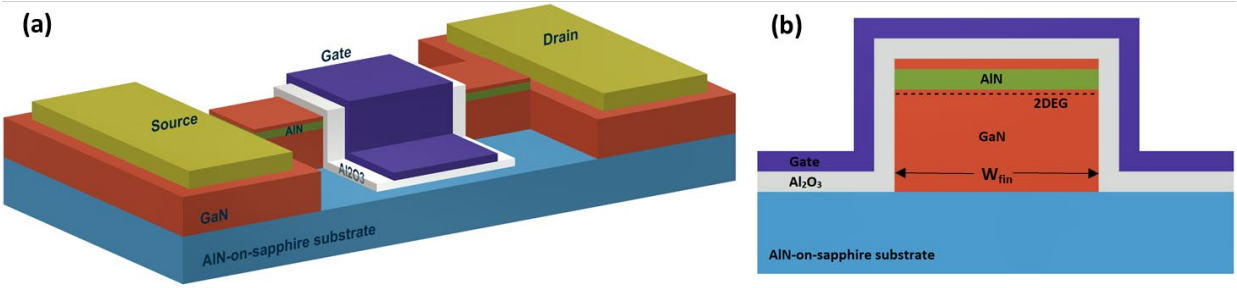


Figure 7.4: *Schematics showing: (a) the overall configuration of the fabricated single-fin AlN/GaN/AlN MOS-FinFET and (b) the MOS gate structure, in cross-sectional view of the device.*

The fabrication of devices started by patterning, using e-beam lithography and a lift-off process, a metal mask on the surface of the sample that covered the areas where the fins would be formed (metal stripes with the desired length and width of the fins). Then

photolithography was used to cover by photoresist the surface of the sample at the regions intended for formation of the Source (S) and Drain (D) Ohmic contacts, which were slightly extending towards the area of the fin (satisfying optical lithography rules to avoid misalignment errors) so that photoresist also covered the edges of the metal stripes of the fin mask. The metal and photoresist layers on the surface of the sample were used as a mask for the simultaneous formation of device mesas and fins by reactive ion etching (RIE), using a BCl_3/Cl_2 gas mixture [32]. The top layers of the HEMT structure were removed by RIE down to the AlN buffer layer, as confirmed by in-situ monitoring based on laser interferometry end-point detection [33]. Without removing the metal mask on the fins and the photoresist mask on the source and drain contact regions [34], additional wet etching was performed by dipping the samples into a commercial developer AZ 826 MIF (90°C for 15 min), which is a buffered Tetramethylammonium hydroxide (TMAH) solution [15, 16, 34]. The AZ 826 MIF treatment exhibits a strong anisotropy in the etching of GaN with minimal etching rate along the c-axis and is known to remove the plasma damage and to smoothen the lateral surface of the RIE-formed fins [15, 16, 34].

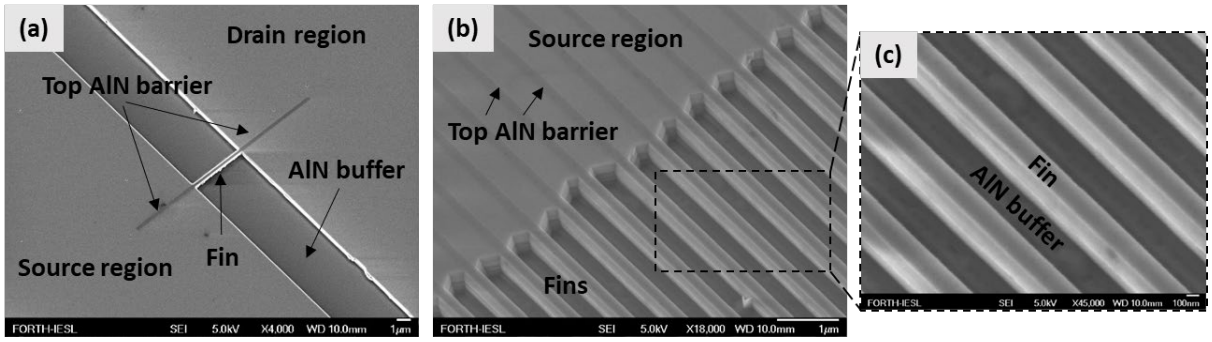


Figure 7.5: *SEM images, in tilted-view, showing the area of the sample near: (a) a single fin device structure and (b) a multi-fin device structure with (c) high magnification close to the region of the fins, after the formation of fins and device mesas by RIE, TMAH treatment and removal of the metal mask.*

Figure 7.5 illustrates SEM images of single-fin (Fig. 7.5(a)) and multi-fin (Figs. 7.5(b) and 7.5(c)) device structures, after the formation of fins and mesas by RIE, and after TMAH treatment and removal of the metal mask from the surface of the fins. Figure 7.5(c) shows with high magnification the area of the fins in the multi-fin (n= 70) device structure. The contrast difference in the extensions for approximately 6 μm of the fin (Fig. 7.5(a)) inside the source (S) and drain (D) contact regions is due to the presence of all epilayers, while in the rest of the S and D regions a top 7-9 nm layer (including AlN barrier) was removed during the TMAH treatment, according to measurements by Veeco DEKTAK 150 surface profilometer. This apparent difference is also observed in the S region of the multi-fin devices (Fig. 7.5(b)).

Ohmic contacts at the S and D regions were formed by Ti/Al/Ni/Au deposition by an electron-beam evaporator, followed by rapid thermal annealing (RTA) at 750 °C. This annealing temperature has been reported by Wang et al. [35] for a similar AlN/GaN heterostructure to provide the minimum specific contact resistivity (ρ_c) for Ohmic contact

formation directly on the GaN buffer layer, after removing the AlN barrier. Subsequently, 20-nm-thick Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD). Then, Ni/Au metal layers were deposited as the gate contact. The fabrication was completed with the formation of pads for all contacts, by Cr/Au metallization on the Al_2O_3 covered AlN buffer layer surface. The connection of the pads to the S/D Ohmic contacts was accomplished by the previous opening of windows in the Al_2O_3 film that covered the S/D contacts.

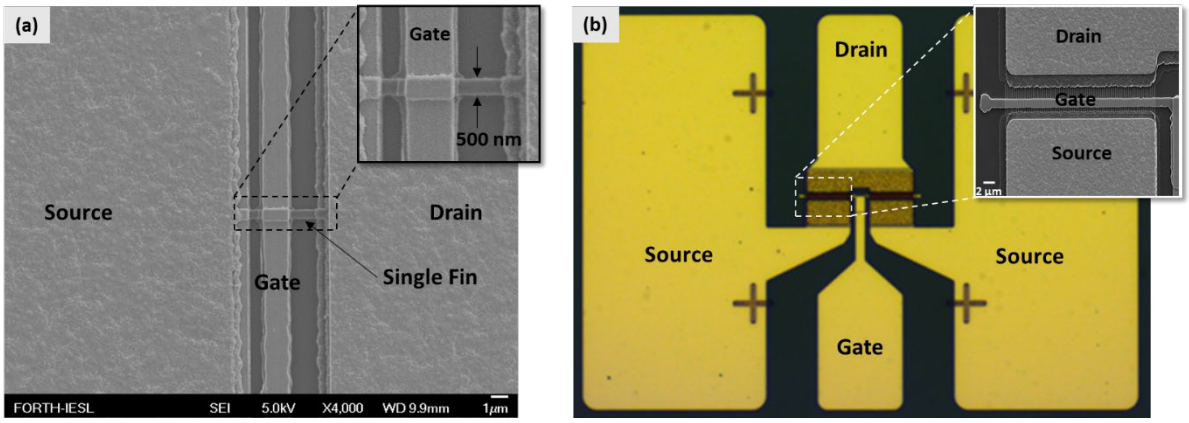


Figure 7.6: *(a) SEM image of a fully-processed single-fin MOS-FinHEMT device and (b) optical microscopy image of a multi-fin MOS-FinHEMT device. (The insets show SEM pictures of the fin and gate areas with high magnification).*

Single-fin MOS-FinHEMT devices were fabricated with fin width (W_{fin}) of 200, 350, 500 and 650 nm. Multi-fin MOS-FinHEMT devices with n = 70 fins of W_{fin} = 200 nm and conventional planar gate MOS-HEMTs, were also fabricated for comparison. Figure 7.6(a) shows the SEM image of a fully-processed single-fin MOS-FinFET device with W_{fin} = 500 nm and Fig. 7.6(b) shows the optical microscopy image of a fully-processed multi-fin device with W_{fin} = 200 nm. The insets in Figs. 7.6(a) and 7.6(b) are SEM images showing with high magnification the fin and gate area of the single-fin and multi-fin device, respectively. All devices were fabricated with gate length L_g = 1.5 μm, source-drain distance L_{sd} = 4 μm and gate-drain distance L_{gd} = 1.5 μm. The gate width in the case of planar MOS-HEMTs was W_g = 45 μm, while in case of single-fin MOS-FinFETs was considered equal to the top gate width that coincides with W_{fin}.

7.5 DC characterization of devices

The fabricated devices were characterized systematically by DC I-V measurements using a Keithley 4200 semiconductor characterization system.

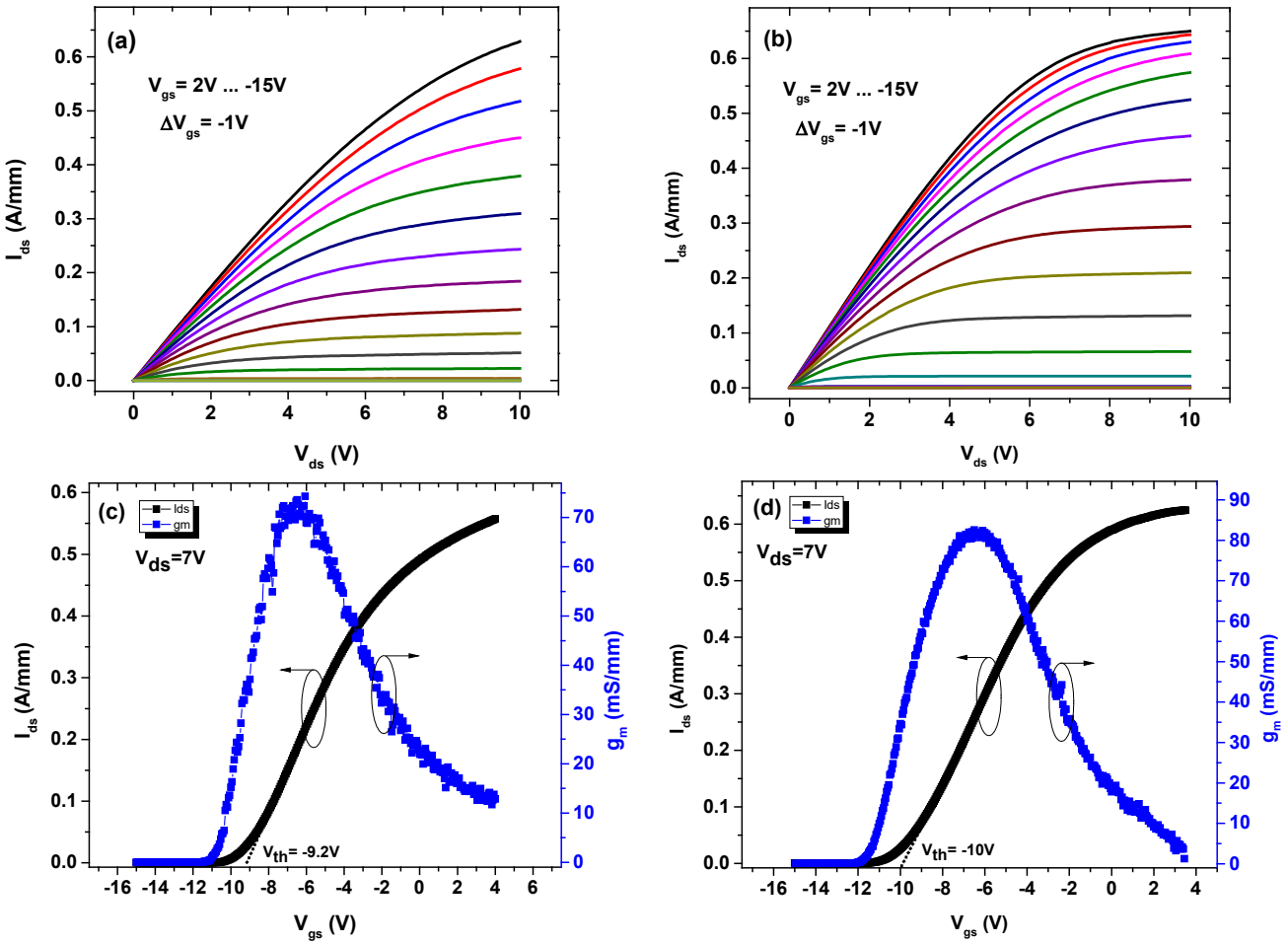


Figure 7.7: *DC characterization results for a MOS-FinHEMT with a single fin of W_{fin}= 650 nm and a planar MOS-HEMT with W_g = 45 µm, processed by the same AlN/GaN/AlN heterostructure: (a) Output (I_{ds}-V_{ds}) characteristics of MOS-FinHEMT, (b) Output (I_{ds}-V_{ds}) characteristics of MOS-HEMT, (c) Transfer (I_{ds}-V_{gs}) characteristics of MOS-FinHEMT and (d) Transfer (I_{ds}-V_{gs}) characteristics of MOS-HEMT. Both devices have L_g = 1.5 µm, L_{sd} = 4 µm and L_{gd} = 1.5 µm.*

Figure 7.7 reveals the experimental DC output (I_{ds}-V_{ds}) and transfer (I_{ds}-V_{gs}) characteristics of a single-fin MOS-FinHEMT with W_{fin} = 650 nm (the widest fin width within the investigated W_{fin} range) and a reference planar MOS-HEMT device, with I_{ds} normalized by the corresponding gate width (I_{ds}/W_g). According to the I_{ds}-V_{ds} output characteristics, the W_{fin} = 650 nm MOS-FinHEMTs reach $I_{ds,max}/W_g$ of 0.62 A/mm (Fig. 7.7(a)), compared to 0.65 A/mm (Fig. 7.7(b)) for the planar MOS-HEMTs. From I_{ds}-V_{gs} transfer characteristics at V_{ds} = 7 V, the W_{fin} = 650 nm MOS-FinHEMTs (Fig. 7.7(c)) and the planar MOS-HEMTs (Fig. 7.7(d)) exhibit maximum transconductance ($g_{m,max}$) of 73 mS/mm and 81 mS/mm, respectively. The threshold voltage (V_{th}) exhibits a positive shift from -10 V of the planar MOS-HEMT devices to -9.2 V of the W_{fin} = 650 nm MOS-FinHEMT devices. The V_{th} was defined as the gate bias intercept of the linear extrapolation of I_{ds} to 0 A.

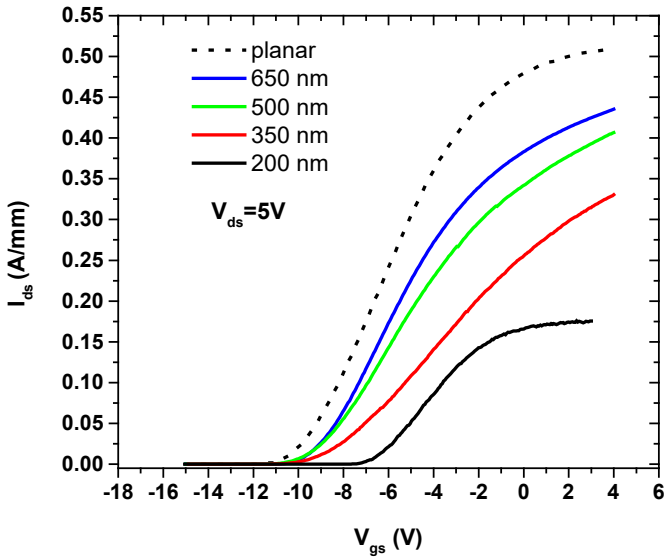


Figure 7.8: *Experimental DC transfer characteristics at V_{ds}= 5 V for single fin MOS-FinHEMTs with different W_{fin} (200, 350, 500 and 650 nm) and the reference planar MOS-HEMT.*

Figure 7.8 shows the experimental DC transfer characteristics of single-fin MOS-FinHEMTs with W_{fin} of 200, 350, 500 and 650 nm and the conventional planar MOS-HEMT, at V_{ds} = 5 V. In this comparative analysis, the choice of V_{ds} = 5 V was made in order to avoid thermal effects that may degrade narrow fin MOS-FinHEMTs at higher V_{ds}. Figure 7.8 reveals a dependence of V_{th} and $I_{ds,max}/W_g$ on the fin width. The V_{th} of the MOS-FinHEMT devices is positively shifted from the -10 V of the planar MOS-HEMT to -9.2 V for W_{fin} = 650 nm, -9.1 V for W_{fin} = 500 nm, -8.5 V for W_{fin} = 350 nm and -6.6 V for W_{fin} = 200 nm. A substantial reduction of $I_{ds,max}/W_g$ with decreasing W_{fin} is also observed (Fig. 7.8). The planar MOS-HEMT exhibits $I_{ds,max}/W_g$ = 0.5 A/mm at V_{ds}= 5V and V_{gs}= 4 V. The corresponding $I_{ds,max}/W_g$ of MOS-FinHEMTs is reduced to 0.43 A/mm for W_{fin} = 650 nm, 0.41 A/mm for W_{fin} = 500 nm, 0.33 A/mm for W_{fin} = 350 nm and 0.17 A/mm for W_{fin} = 200 nm. Qualitatively similar dependences of V_{th} [14–19] and $I_{ds,max}/W_g$ [16, 17, 19] on W_{fin} have been reported for AlGaN/GaN multi-fin FinHEMTs and their origins will be clarified in the following.

7.6 Simulations of devices

Comparative simulations of single-fin MOS-FinHEMT and planar MOS-HEMT devices, based on the AlN/GaN/AlN double barrier heterostructure, were performed using Silvaco Atlas software [36]. A 3D model was employing to predict the DC characteristics of the devices [36] with the material properties listed in Table 7.2 [28, 29, 37] and the nitride specific field dependent mobility model for free electrons, which is given by [36–37] :

$$\mu_n = \frac{\mu_{n0}(\mathrm{T,N}) + v_{sat}\dfrac{E^{n_1-1}}{E_C^{n_1}}}{1 + a\left(\dfrac{E}{E_C}\right)^{n_2} + \left(\dfrac{E}{E_C}\right)^{n_1}} \qquad (7.1)$$

where μ_{n0} *(T,N)* is the low field mobility, *E* is the electric field and V_{sat}, E_C, *a*, n_1, n_2 are model parameters with their values listed in Table 7.2 for GaN and AlN materials. The μ_{n0} (T,N) is given by [36–37] :

$$\mu_{n0}(\mathrm{T,N}) = \mu_{\min}\left(\frac{T}{300}\right)^{\beta_1} + \frac{(\mu_{\max} - \mu_{\min})\left(\dfrac{T}{300}\right)^{\beta_2}}{1 + \left[\dfrac{N}{N_{ref}\left(\dfrac{T}{300}\right)^{\beta_3}}\right]^{a_1(T/300)^{\beta_4}}} \qquad (7.2)$$

where *T* is the temperature, *N* is the total doping density and *a*, β_1, β_2, β_3, β_4, μ_{min}, μ_{max}, N_{ref} are model parameters with their values listed in Table 7.2 for GaN and AlN materials.

In addition, the donor concentrations of $N_D=10^{13}$ cm^{-3} for AlN and $N_D=10^{16}$ cm^{-3} for GaN, were assumed, considering the typical electron concentration of undoped GaN epilayers and the high resistivity exhibited by AlN epilayers. For the AlN/GaN heterojunction, a constant polarization scale factor [36] of 0.8 was used in order to calibrate the simulated with the experimental 2DEG density in corresponding structures of our previous work [11–12]. By using this polarization scale factor the total polarization charge density of 5.34 x 10^{13} cm^{-2} was assumed at the AlN/GaN heterojunction. The dielectric constant of 10.3 was used for the Al_2O_3 gate dielectric [38].

TABLE 7.2: Material properties (bandgap, effective electron masses in the growth and perpendicular to the growth direction, lattice constant and polarization parameters) and nitride field effect mobility parameters, used in the device simulations [Refs. 28, 29 and 37]

	GaN	*AlN*
E_g @300K (eV)	3.42	6.28
$m_{e,l}^*/m_0$	0.18	0.25
$m_{e,t}^*/m_0$	0.20	0.33
α_0 *(Å)*	3.189	3.112
e_{33} (C/m^2)	0.67	1.50
e_{31} (C/m^2)	-0.34	-0.53
P_{sp} (C/m^2)	-0.034	-0.09

V_{sat} (cm/s)	1.90 x 10^7	2.16 x 10^7
E_C (kV/cm)	220.8936	447.0339
n_1	7.2044	17.3681
n_2	0.7857	0.8554
α	6.1973	8.7253
μ_{min} (cm^2/Vs)	295	297.8
μ_{max} (cm^2/Vs)	1460.7	683.8
α_1	0.66	1.16
β_1	-1.02	-1.82
β_2	-3.84	-3.43
β_3	3.02	3.78
β_4	0.81	0.86
N_{ref}	10^{17}	10^{17}

7.6.1 Scaling the fin width

The MOS-FinHEMT device with W_{fin} = 650 nm fin was chosen as reference for these device simulations. This implies that we assumed a contact resistance R_c= 6.15 kΩ and an effective fixed positive charge Q_{if} = 4.4 x 10^{13} cm^{-2} at the AlN/Al_2O_3 MOS interface [39–40] to achieve I_{ds} and V_{th} similar to the experimental values of the W_{fin} = 650 nm MOS-FinHEMT (Figs. 7.7 and 7.8). The simulations assumed that the S/D contacts in all devices covered an orthogonal area limited to 650 nm width and 500 nm length, which corresponded to the use of a virtual "specific contact resistivity" (ρ_c) of 2 x 10^{-5} Ω cm^2 as an input parameter in the simulation software. For computational efficiency and focus on the comparative operation of different fin width devices, the 1-nm-thick GaN cap layer was not taken into account in the overall simulations, considering that its charge effects at the MOS interface could be effectively reflected in the calibrated value of Q_{if}.

Figure 7.9 shows the simulated DC output (I_{ds}-V_{ds}) characteristics (Fig. 7.9(a)) and the DC transfer (I_{ds}-V_{gs}) characteristics (Fig. 7.9(b)), at V_{ds} = 5 V, for the W_{fin} = 650 nm MOS-FinHEMT.

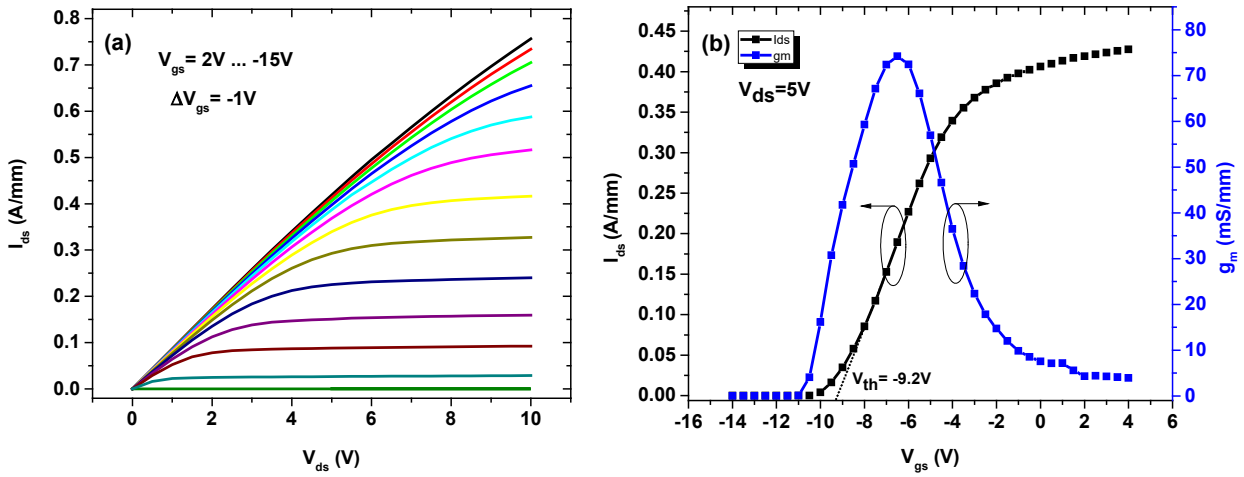


Figure 7.9: *Simulated (a) DC output (I_{ds}-V_{ds}) characteristics and (b) DC transfer (I_{ds}-V_{gs}) characteristics at V_{ds} = 5 V of the AlN/GaN/AlN MOS-FinHEMT with W_{fin} = 650 nm and L_g = 1.5 µm.*

Figure 7.10 illustrates the simulated DC transfer curves at V_{ds} = 5 V for MOS-FinHEMT devices with the different values of W_{fin} used in the experimental work. As shown in Fig. 7.10, the reduction of the W_{fin} of MOS-FinHEMTs is predicted to create a clear shift in positive direction of their threshold voltage, similarly to the experimental results (Fig. 7.8). However, for this range of W_{fin} (200-650 nm), $I_{ds,max}/W_g$ remains rather independent of W_{fin} and gate structure (tri-gate or planar), contrary to our experimental observations.

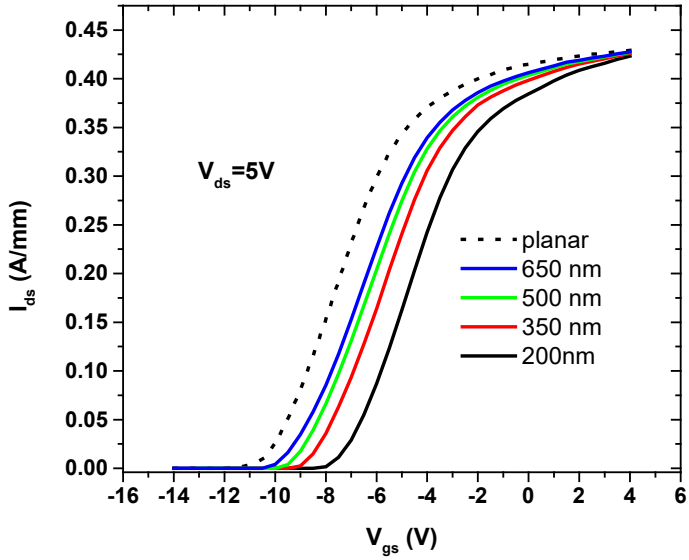


Figure 7.10: *Simulated DC transfer characteristics of AlN/GaN/AlN planar MOS-HEMT and MOS-FinHEMTs with different W_{fin} (200, 350, 500 and 650nm), at V_{ds} = 5 V.*

For the completeness of our study on the W_{fin} effects on V_{th} and $I_{ds,max}/W_g$, it is important also to address the potential strain relaxation of the top AlN barrier in the

narrow fin nanostructures. Following the description of Ren et al. [41] for fins with an AlGaN/GaN 2DEG heterojunction, the total polarization sheet charge density at the AlN/GaN interface within the area of the fin can be written as:

$$\sigma_{fin} = \sigma_{planar} - [P_{pz\_AlN} \cdot R(W_{fin})] \quad (7.3)$$

where σ_{fin} is the total polarization sheet charge density at the AlN/GaN heterojunction in the fin, σ_{planar} is the corresponding total polarization sheet charge density in a large area planar sample, P_{pz_AlN} is the piezoelectric polarization of a fully strained AlN-on-GaN layer and $R(W_{fin})$ gives the fraction of elastic strain relaxation (R) in the AlN HEMT barrier as a function of fin width (W_{fin}). The value of $R(W_{fin})$ could vary between zero (full strain) to one (full relaxation) and according to Ren et al. [41], an empirical formula to calculate R for AlGaN barrier in a fin of width W_{fin} is:

$$R(W_{fin}) = 39.813 \cdot (W_{fin} \cdot 10^{9})^{-0.962} \quad (7.4)$$

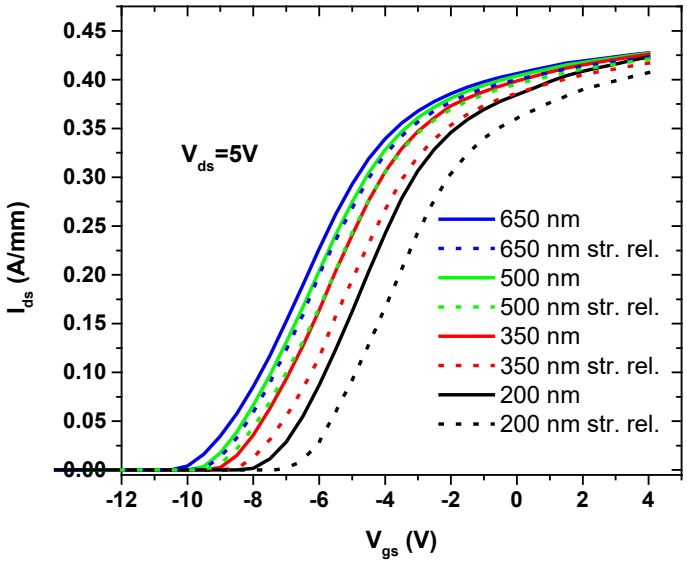


Figure 7.11: *Simulated transfer characteristics at V_{ds}= 5 V of AlN/GaN/AlN MOS-FinHEMTs with different W_{fin}, calculated by either assuming (dotted lines) or not assuming (continuous lines) a reduction of the polarization charge at the top AlN/GaN heterojunction due to partial elastic strain relaxation in the AlN layer that depends on W_{fin}.*

In order to investigate the effect of possible elastic strain relaxation in the top AlN barrier in the fins, we re-examined the previously described AlN/GaN/AlN MOS-FinHEMT simulations by modifying the polarization charge according to Eqs. 7.3 and 7.4. Figure 7.11 shows a comparison of the simulated DC transfer characteristics of AlN/GaN/AlN MOS-FinHEMTs for different fin widths, with or without the effect of AlN barrier strain relaxation on σ_{fin}, according to Eqs. 7.3 and 7.4. As illustrated in Fig. 7.11, the increasing

reduction of σ_{fin} compared to the planar device, as W_{fin} decreases, leads to an additional positive shift of V_{th} and to a slight decrease of $I_{ds,max}/W_g$ at V_{gs} = 4 V.

The positive shift of V_{th} may enable the fabrication of normally-off MOS-FinHEMTs, based on the AlN/GaN/AlN double heterostructure, by reduction of W_{fin} far below 200 nm. Figure 7.12 shows the simulated DC transfer characteristics of the AlN/GaN/AlN MOS-FinHEMTs with W_{fin} of 50, 20 and 10nm, for the two extreme cases of σ_{fin} corresponding to zero and full elastic strain relaxation in the top AlN barrier. The boundary condition for normally-off operation, i.e. V_{th}= 0 V, was determined for W_{fin} equal to 17 or 31 nm by assuming fully strained or fully relaxed AlN, respectively. Figure 7.12 also illustrates a significant reduction of $I_{ds,max}/W_g$ with the reduction of W_{fin}. Assuming zero strain relaxation in the top AlN barrier, the predicted $I_{ds,max}/W_g$ at V_{gs}= 4 V is 0.39 A/mm for W_{fin} = 50 nm, 0.35 A/mm for W_{fin} = 20 nm and 0.32 A/mm for W_{fin} = 10 nm. The corresponding $I_{ds,max}/W_g$ values for full strain relaxation in AlN would be 0.30 A/mm for W_{fin} = 50 nm, 0.25 A/mm for W_{fin} = 20 nm and 0.23 A/mm for W_{fin} = 10 nm.

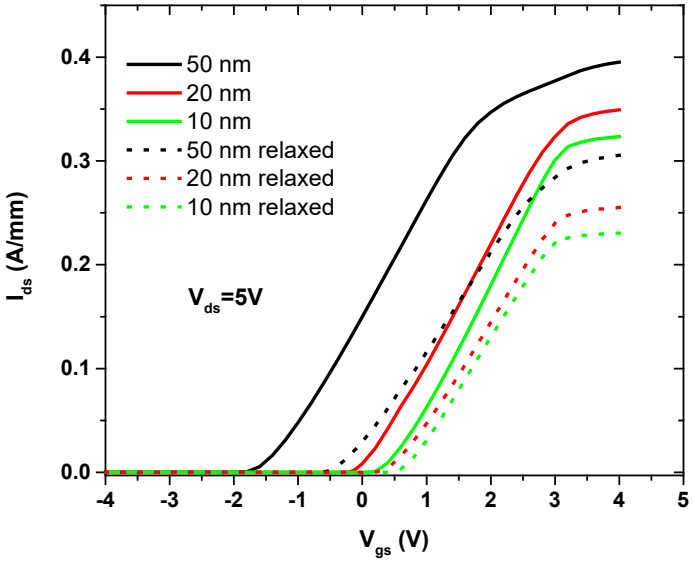


Figure 7.12: *Simulated transfer characteristics at V_{ds}= 5 V of AlN/GaN/AlN MOS-FinHEMTs with W_{fin} of 50, 20 and 10 nm, calculated by either assuming (dotted lines) or not assuming (continuous lines) full elastic strain relaxation in the top AlN barrier.*

7.6.2 Effect of S/D contact resistance

Previous simulations assumed the same contact resistance R_c= 6.15 kΩ for the S/D contacts of all devices, which corresponds to the same virtual "specific contact resistivity" (ρ_c) of 2 x 10^{-5} Ω cm^2 for the hypothetical 650 nm x 500 nm S/D contact areas of all devices. Figure 7.13 shows the schematic configuration with the three components of parasitic resistances: (a) metallization semiconductor resistance ($R_{m/s}$), (b) spreading resistance (R_{sp}) and (c) extension resistance (R_{ext}), in the S or D region of an AlN/GaN/AlN MOS-FinHEMT [42]. The $R_{s/m}$ refers to the resistance at the S/D metallization/semiconductor interface due to non-optimized ohmic contacts. The R_{ext} is the parasitic resistance in the

fin extension region (the area that is not covered by gate and S/D metallization) between S/D and gate region, and R_{sp} is the series resistance caused by the current spreading or current crowding from the S/D extension region into the S/D region [42]. The R_c induced in device simulations, physically includes the $R_{s/m}$ and R_{sp} resistances [42]. A series of simulations were carried out to determine the expected effect of different R_c on $I_{ds,max}$ of single-fin MOS-FinHEMT devices with different fin width (W_{fin}).

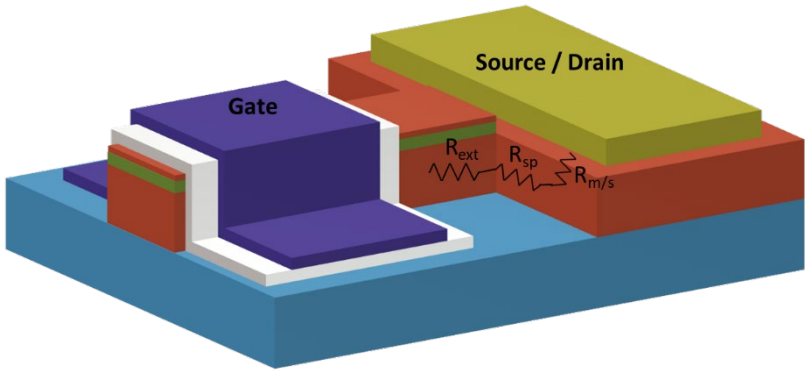


Figure 7.13: *The schematic shows the parasitic resistances in S/D region of an AlN/GaN/AlN MOS-FinHEMT, composed of three components: the metallization/ semiconductor resistance ($R_{m/s}$), the extension resistance (R_{ext}) and the spreading resistance (R_{sp}).*

Figure 7.14(a) shows the simulated $I_{ds,max}/W_g$ values, at V_{ds}= 5 V and V_{gs}= 4 V, as a function of fin width of AlN/GaN/AlN MOS-FinHEMTs for four different values of R_c (10^{-20}, 0.615, 6.15 and 61.5 kΩ) and with an effective fixed positive charge Q_{if} = 4.4 x 10^{13} cm^{-2} at the AlN/Al_2O_3 MOS interface (R_c= 10^{-20} kΩ is an approximation of R_c= 0 Ω, allowing to use the logarithmic axis in the plot of Fig. 7.14(b)). Figure 7.14(b) shows the same data, but $I_{ds,max}/W_g$ has been plotted versus R_c for the seven different values of W_{fin} (10, 20, 50, 200, 300, 500 and 650 nm). It is evident from both plots that the current driving capability of MOS-FinHEMTs should be insensitive to W_{fin} for fins wider than 200 nm and will differentiate only with the variation of R_c and, in general, the parasitic resistances. For constant R_c, a reduction of current with decreasing W_{fin} is expected only for the narrow fins, roughly for W_{fin} < 200 nm.

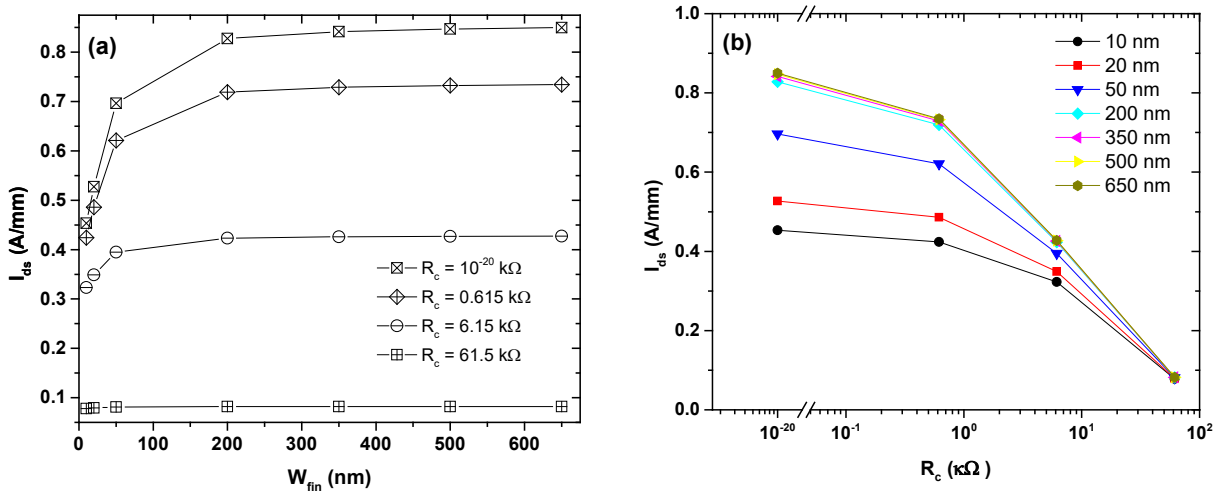
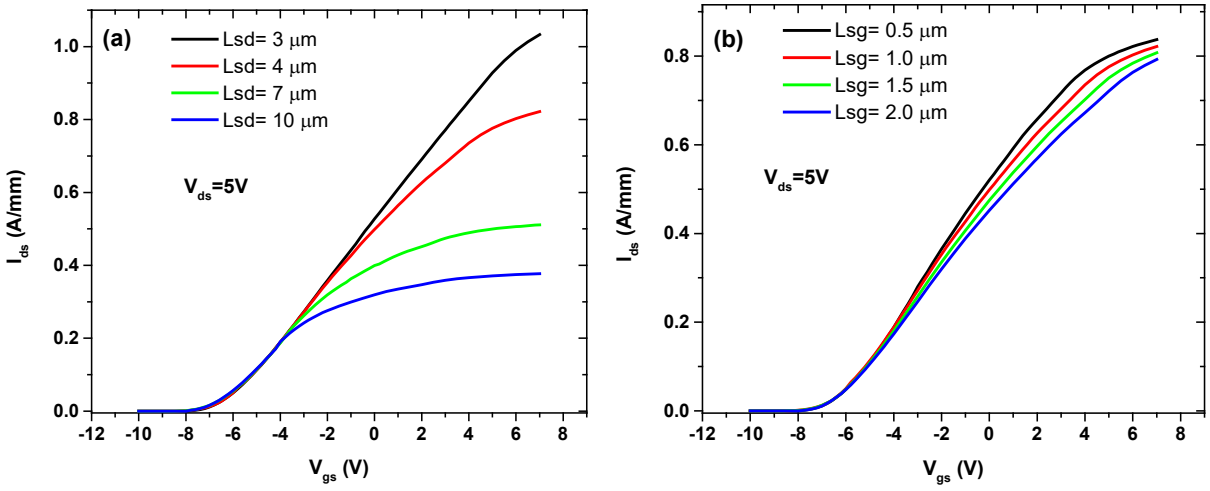


Figure 7.14: *Simulation results showing the effects of W_{fin} and R_c on $I_{ds,max}/W_g$ at V_{ds}= 5 V (V_{gs}= 4 V) of single-fin AlN/GaN/AlN MOS-FinHEMTs: (a) Plot of $I_{ds,max}/W_g$ versus W_{fin} for values of R_c equal to 10^{-20} (approximation of 0), or 0.615, or 6.15 or 61.5 kΩ, (b) Plot of $I_{ds,max}/W_g$ versus R_c for values of W_{fin} equal to 10, 20, 50, 200, 350, 500 and 650 nm.*

7.6.3 Effects of contact distances and oxide thickness

For the completeness of the theoretical analysis of single-fin MOS-FinHEMTs, based on the double AlN/GaN/AlN heterostructure, we also studied the dependence of the DC transfer (I_{ds}-V_{gs}) characteristics of the devices on the following device parameters: (a) the fin length, being equal with the distance between source and drain contacts (L_{sd}), (b) the source to gate distance (L_{sg}) for a fixed L_{sd}, and (c) the Al_2O_3 gate dielectric thickness (t_{ox}). These device simulations were carried out assuming R_c = 0 Ω for the S/D Ohmic contacts.



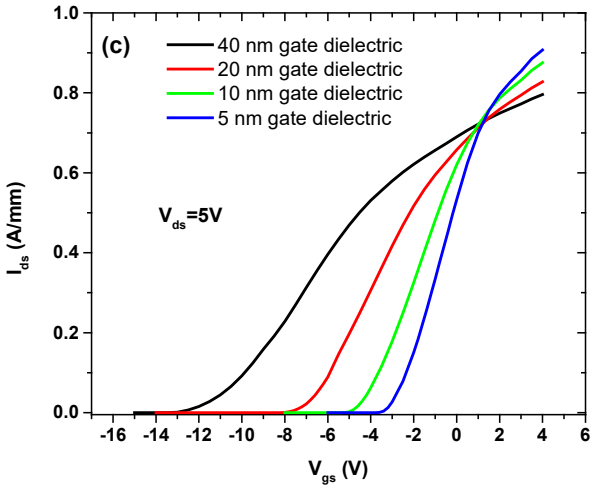


Figure 7.15: *Simulated DC transfer (I_{ds}-V_{gs}) characteristic at V_{ds} = 5 V of MOS-FinHEMTs with W_{fin} = 200 nm and L_g = 1.5 μm by varying: (a) the fin length between the source and drain contacts (L_{sd}), (b) the source to gate distance (L_{sg}) for L_{sd}= 4μm and (c) the Al_2O_3 gate dielectric thickness.*

Figure 7.15(a) illustrates the simulated I_{ds}-V_{gs} characteristics at V_{ds}= 5 V for a MOS-FinHEMT with W_{fin} = 200 nm, t_{ox}= 20 nm, L_g= 1.5 μm, L_{sg}= 1.5 μm and L_{sd} of 3, or 4, or 7 or 10 μm. The V_{th} is independent of the L_{sd} variation, while the $I_{ds,max}/W_g$ (V_{ds}= 5 V and V_{gs}= 7 V) increases by decreasing L_{sd}. The predicted $I_{ds,max}/W_g$ is 0.37 A/mm for L_{sd}= 10 μm and increases to 0.51 A/mm and 0.82 A/mm for L_{sd} of 7 μm and 4 μm, respectively. The maximum value of 1.05 A/mm corresponds to the minimum L_{sd}= 3 μm, from the investigated L_{sd} range.

Figure 7.15(b) shows the simulated I_{ds}-V_{gs} transfer characteristics at V_{ds}= 5 V for a MOS-FinHEMT with W_{fin} = 200 nm, t_{ox}= 20 nm, L_g= 1.5 μm, L_{sd}= 4 μm and L_{sg} of 0.5, or 1.0, or 1.5 or 2.0 μm. The V_{th} is independent of the L_{sg} variation, while the $I_{ds,max}/W_g$ (V_{ds}= 5 V and V_{gs}= 7 V) is slightly increasing by decreasing L_{sg}. The predicted $I_{ds,max}/W_g$ is 0.792 A/mm for L_{sg}= 2 μm and increases to 0.807 A/mm and 0.822 A/mm for L_{sg} of 1.5 and 1 μm, respectively. For the investigated L_{sg} range, the maximum value of 0.837 A/mm is reached for the L_{sg}= 0.5 μm MOS-FinHEMT.

Finally, Fig. 7.15 (c) depicts the simulated I_{ds}-V_{gs} characteristics at V_{ds}= 5 V for a MOS-FinHEMT with W_{fin} = 200 nm, L_g= 1.5 μm, L_{sg}= 1 μm, L_{sd}= 4 μm, and t_{ox} of 5, or 10, or 20, or 40 nm. The V_{th} is positively shifted by reducing the t_{ox}, being -11.4 V for t_{ox}= 40 nm, -7.2 V for t_{ox}= 20 nm, -4.5 V for t_{ox}= 10 nm and -2.8 V for t_{ox}= 5 nm. Therefore, t_{ox} is a critical parameter for fine tuning of normally off operation, since an accurate control of V_{th} can be achieved by varying it. The calculated $I_{ds,max}/W_g$ values at V_{ds}= 5 V and V_{gs}= 4 V are increasing by decreasing t_{ox}, from 0.79 A/mm for t_{ox}= 40 nm, to 0.82, 0.87 and 0.90 A/mm for t_{ox} of 20, 10 and 5 nm, respectively.

7.7 Comparative study and overall discussion

The experimental and device simulation results exhibited a very good agreement for the dependence of threshold voltage (V_{th}) on the fin width (W_{fin}) of single-fin MOS-FinHEMTs, based on the AlN/GaN/AlN double barrier heterostructure. This is evident in the plot of Fig. 7.16, which presents both the V_{th} values extracted from experimental DC transfer characteristics (Fig. 7.8) and the V_{th} values extracted from simulated DC transfer characteristics, assuming no strain relaxation in the top AlN barrier (Figs. 7.10 and 7.12). It should be noted that the W_{fin}= 650 nm MOS-FinHEMT was used as reference/calibration for the device simulations (section 7.6.1) and the simulated V_{th} was set to match the experimental one. As shown in Fig. 7.16, the V_{th} exhibits a positive shift from planar MOS-HEMT to MOS-FinHEMT devices that increases with the decrease of W_{fin}.

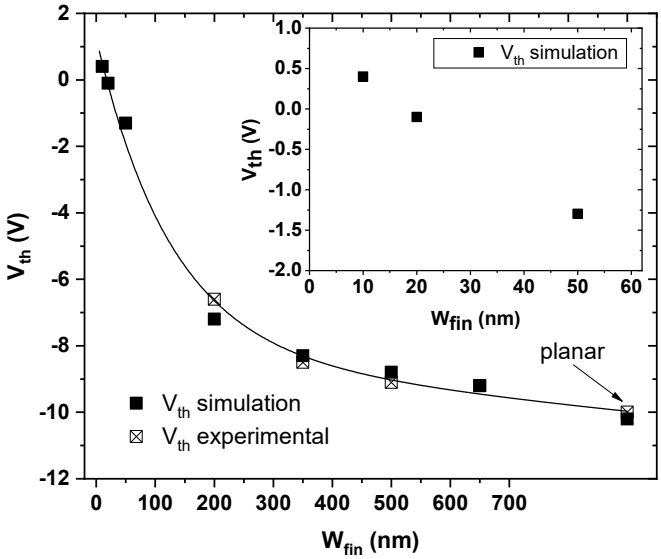


Figure 7.16: *Simulated and experimental V_{th} as a function of W_{fin} in MOS-FinHEMTs and planar MOS-HEMT, based on the double barrier AlN/GaN/AlN heterostructure. The simulations assumed no elastic strain relaxation in the top AlN barrier. The inset shows the simulation results for the narrow W_{fin} region.*

This behavior of V_{th} is understood considering the contribution to the depletion of the channel of the two sidewall gates in a MOS-FinHEMT device (Fig. 7.4(b)). Increasing the negative V_{gs} bias will induce a depletion region going inwards from the GaN sidewalls [14]. Consequently, under depletion bias conditions, in case of a conventional planar AlN/GaN/AlN MOS-HEMT, the width of the channel ($W_{ch/planar}$) would be equal to the width of the actual 2DEG channel (W_{2DEG}), while in case of a MOS-FinHEMT the width of the channel ($W_{ch/fin}$) would be equal to the width of the actual 2DEG channel (W_{2DEG}) reduced by the width of the two depletion zones ($2W_{dep}$) at the GaN sidewalls:

$$W_{\mathrm{ch/fin}} = W_{2DEG} - 2W_{dep} \quad (7.5)$$

For wide W_{fin} devices, the effect of the lateral gate contacts on the 2DEG channel, shown by the second term in Eq. (7.5), is almost negligible. However, for narrow W_{fin}

devices, the 2DEG channel will start to diminish at lower values of negative V_{gs}, as the depletion zones at GaN sidewalls become comparable to W_{fin}. This effect will shift V_{th} to less negative values, in agreement with our results.

Thus normally-off transistor operation can be achieved by the reduction of W_{fin} below a value that would depend on the degree of strain relaxation in the top AlN barrier. The large tensile strain in AlN may elastically relax due to the free lateral surfaces of the three-dimensional (3D) fin nanostructure, reducing the piezoelectric polarization component and the 2DEG density. The simulations indicate that V_{th}= 0 V would correspond to W_{fin}= 17 nm for zero strain relaxation and to W_{fin}= 31 nm for full strain relaxation in the top AlN barrier of the studied AlN/GaN/AlN heterostructure. The degree of AlN strain relaxation, for a given W_{fin} value, may be taken into account (Figs. 7.11 and 7.12) by an empirical formula such as Eq. 7.4 that was developed for AlGaN barrier FinHEMTs [41]. Figure 7.16 shows a difference of +0.6 V between the experimental and simulated V_{th} values for the W_{fin}= 200 nm MOS-FinHEMT, which may be related to AlN partial strain relaxation.

Contrary to V_{th}, the simulated and experimental data did not reveal the same effect of W_{fin} on the current driving capability of the MOS-FinHEMTs. The device simulations suggest that $I_{ds,max}/W_g$ should be independent of W_{fin} in the range of 200-650 nm (Fig. 7.10) or it might exhibit a negligible reduction if partial strain relaxation is assumed in the AlN barrier (Fig. 7.11). This is understood considering that the role of lateral electric fields related to the sidewall gates would be negligible for the operation of transistors with wide fin-channel. However, the experimental data (Fig. 7.8) present a clear reduction of $I_{ds,max}/W_g$ with decreasing W_{fin}. The $I_{ds,max}/W_g$ of the MOS-FinHEMT with W_{fin} = 200 nm is reduced 2.5 times compared to W_{fin} = 650 nm and almost 3 times compared to the planar MOS-HEMT, which exhibits the largest $I_{ds,max}/W_g$. The device simulations presented in sections 7.6.2 and 7.6.3 suggest that this behavior results from parasitic resistances due to the contacts and the S/D access regions. This explanation is also supported by DC I-V measurements to multi-fin (n= 70) test MOS-FinHEMTs, which revealed higher $I_{ds,max}/W_g$ values compared to that of the corresponding single fin devices.

For the test MOS-FinHEMT devices fabricated in the present work (Fig. 3), we analyzed with device simulations the potential variation of the S/D contact resistance (R_c) for different W_{fin}. The R_c is considered to physically include the resistance present at the metallization/semiconductor interface and any series resistance due to current spreading/crowding between the fin and the S/D contacts [42]. An assumption was that conduction at the S/D contacts might be dominated by the orthogonal areas of {~6 μm x W_{fin}} where the entire HEMT structure and 2DEG are present. These areas correspond to the geometrical extensions of the fin on the S/D contact regions for approximately 6 μm, as shown in Fig. 7.5. Assuming a constant specific resistivity ρ_c for these contact regions, then the contact resistance R_C would scale with W_{fin}, in comparison to the reference W_{fin}= 650 nm, according to:

$$R_C\left(W_{fin}\right)=\frac{650}{W_{fin}}R_C\left(650nm\right) \qquad (7.6)$$

The MOS-FinHEMT device simulations that were initially made for constant R_c (Fig. 7.10) were repeated for R_c varying with W_{fin} according to Eq. 7.6, and the results for the $I_{ds,max}/W_g$ values are presented, together with the experimental values, in Fig. 7.17 These simulations resulted to reduction of $I_{ds,max}/W_g$ with decreasing W_{fin}, in qualitative agreement with the experimental results. The actual device performance is more complex, but Fig. 7.17 clearly indicates the role of S/D contact resistance for the observed current variations in devices with W_{fin} between 200-650 nm. Furthermore, the results suggest that parasitic resistances should be the main cause of the significant inconsistencies in the comparative currents of FinHEMT and planar HEMT devices revealed from the overall literature reports on AlGaN/GaN structures. Optimized device design and processing requires large S/D contact areas in order to minimize the R_c. For a comparative study of device performances, the "active" S/D area should also be constant and independent of the W_{fin} and device geometry (planar or fin type).

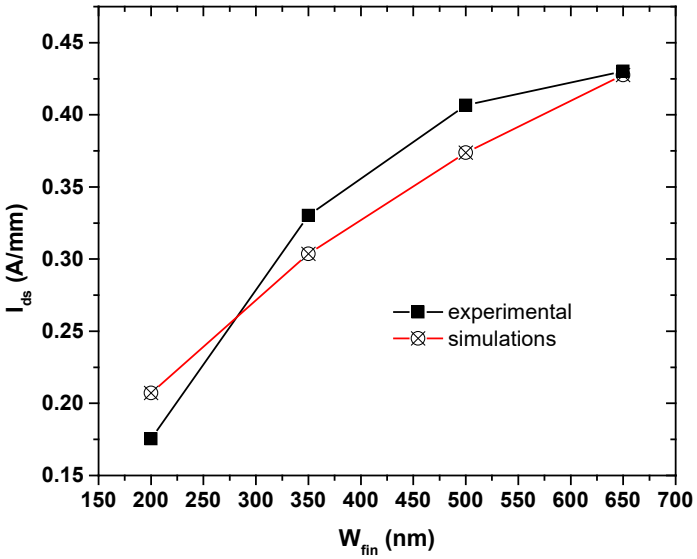


Figure 7.17: *Simulated and experimental $I_{ds,max}/W_g$ values at V_{ds}= 5 V and V_{gs}= 4 V as a function of fin width of AlN/GaN/AlN MOS-FinHEMTs. The device simulations were carried out by assuming dependence of the contact resistance on the W_{fin}, according to $R_C(W_{fin}) = \frac{650}{W_{fin}} R_C(650\ nm)$.*

According to the device simulations (Fig. 7.12), the AlN/GaN/AlN MOS-FinHEMTs with narrower fin widths, in the region of 10-50 nm, are expected to exhibit a reduction of $I_{ds,max}/W_g$ even assuming a constant R_C. This is understood as an effect of the three-dimensional electric field distribution due to the fin sidewall gates on the pinch-off of the channel at the drain side.

7.8 Conclusions

In conclusion, the application of an AlN/GaN/AlN double barrier heterostructure in the fabrication of single-fin MOS-FinHEMTs has been investigated by combining device simulations and experimental device fabrication and characterization. This work provides information for the variation of the DC I-V characteristics of MOS-FinHEMTs with the scaling of fin width. The threshold voltage shifts to positive direction with reduction of fin width, due to the lateral electric field of the sidewall gates. Normally-off transistor operation will become possible for fins with width less than 17 nm, if the tensile strain in the top AlN barrier is not relaxed. Elastic relaxation of the tensile strain in the AlN layer within the 3D fin nanostructure would reduce the 2DEG density and the achievable currents. Correspondingly, the minimum fin width for normally-off operation may be up to 31 nm, depending on the degree of strain relaxation. The achievable drain-source current density in the MOS-FinHEMTs is reduced in narrow fins approaching the dimensions of normally-off operation, due to the lateral fields of the gate structure. However, for sufficiently wide fins, such as in the region of 200-650 nm, a reduction of current density with decrease of fin width would result from increase of contact resistance. Overall, the research presented in this chapter contributes to the critical fundamental understanding of MOS-FinHEMTs based on AlN/GaN/AlN double barrier heterostructure while it can act as support for the design of GaN-based FinHEMTs for either low-power (digital, few fins) or high-power applications (multi fins).

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Chapter 8

Top-down GaN vertical NW MESFETs

8.1 Introduction and motivation

One-dimensional semiconductor nanostructures, such as nanowires (NWs), have gained significant interest as promising elemental building blocks in nanoelectronic and nanophotonic applications [1–3]. Their reduced dimensionality and high aspect ratio could enhance the miniaturization of devices and lead to high device density, decreased power consumption and high operation frequency [4–6]. Among them, nanowires of gallium nitride (GaN) have attracted much attention for the exploitation of the fundamental advantages of GaN material, such as wide direct band gap, high thermal conductivity and high breakdown voltage [7–10]. In particular, device simulations of Chowdhury et al. [10] predict that n-type GaN NW field-effect transistors (FETs) with gate length of 5 nm would outperform Si and other semiconductors, due to the higher electron effective mass and lower permittivity of GaN. This is attributed [10] to reduction of the source to drain direct tunneling by the relatively higher effective mass and better short-channel characteristics due to the lower permittivity of GaN. The all-around (wrap) gate in NW FETs offers better electrostatic control of the gate on the channel, in comparison to other gate designs, such as double- or tri-gate transistors [11].

The fabrication of GaN vertical NW transistors requires an accurate control of the position and dimensions of NWs. However, it is difficult to achieve these requirements by spontaneous or selective growth of GaN NWs, as reported analytically in chapter 5. For this reason, our interest shifted to a top-down approach for formation of vertical GaN NWs from GaN films by three processing steps: nanopatterning by electron-beam lithography (e-beam), reactive-ion etching (RIE) and anisotropic wet-chemical etching based on a Tetramethylammonium hydroxide (TMAH) solution [12]. According to literature reports, a Potassium hydroxide (KOH) solution can be also used, for the final wet-etching treatment [13].

There has been a limited amount of experimental work on top-down n-type GaN V-NW FETs [13–16], while there is no reference for bottom-up fabrication of GaN V-NW FETs, which indicates the overall difficulties in growth and processing of these structures. In all top-down fabricated transistors, a metal-insulator-semiconductor (MIS) gate has been used to fabricate FETs (MISFETs) from GaN NWs with diameter of either 120 nm [14,16], or 500 nm [13] or 800 nm [15] that were top-down processed from GaN epilayers grown by MOCVD. These works have shown the capability to realize both normally-off [13, 14, 16] and normally-on [15] GaN V-NW MISFET devices.

This chapter focuses on formation of top-down GaN V-NWs and fabrication of GaN V-NW FETs with Schottky barrier gate (V-NW MESFETs)[12]. A Cr Schottky-barrier gate was preferred, since MESFET devices can provide higher transconductance values compared to MISFETs. The GaN V-NW MESFET devices comprised an array of 900 (30x30)

NWs, with diameter of 100 nm. A nanofabrication process was developed and all fabrication steps were analyzed systematically, in order to understand the implication of fabrication aspects on the operation and performance of devices. The proposed GaN V-NW MESFET fabrication process is also applicable to selective area grown GaN V-NWs and it could be also adapted to V-NW MOSFET fabrication. It can be used for processing either single V-NW FETs as low power digital devices or multiple V-NW FETs as high power vertical GaN transistor switches. It establishes a technological platform that could be also extended to other semiconductors, especially of wide bandgap ones (e.g. exhibiting similar etching difficulties). High Resolution Transmission Electron Microscopy (HRTEM) studies were also performed to unintentionally doped top-down GaN V-NW structures to investigate the presence of threading dislocations along the formatted GaN V-NWs.

8.2 Formation of top-down GaN vertical NWs

Two epitaxial GaN structures were grown on sapphire (0001) substrates by PAMBE [17]. The first epitaxial structure consisted (from top to bottom) of 300-nm-thick Si-doped GaN layer (n^+-GaN) with doping concentration of 10^{19} cm^{-3}, 600-nm-thick unintentionally doped GaN layer (u-GaN) with electron concentration of approximately 10^{16} cm^{-3}, 500-nm-thick Si-doped GaN layer (n^+-GaN) with doping concentration of 10^{19} cm^{-3} and 30-nm-thick AlN layer and it was processed to form the vertical GaN NWs for the fabrication of GaN V-NW MESFETs (device structure). The second epitaxial structure consisted of 1500-nm-thick u-GaN with electron concentration of approximately 10^{16} cm^{-3} and 30-nm-thick AlN layer, and it was processed to form the vertical GaN NWs for HRTEM characterization (test structure).

In both structures, the formation of GaN NWs started by patterning, using e-beam lithography and a lift-off process, a Ni etch-mask on the surface of the sample that covered the areas where the nanowires should be formed. The diameter of the patterned circular Ni dots was 120 nm and 220 nm for the device structure and test structure, respectively, while the pitch was 1 μm in both cases. The Ni layer acted as a mask for GaN reactive ion etching (RIE), using a BCl_3/Cl_2 gas mixture [18]. Figure 8.1(a) shows the RIE-formed trapezoidal GaN device nanostructures with diameters of 120 nm to 650 nm from top to bottom and height of 1.15 μm, while Fig. 8.1(b) shows the corresponding test nanostructures with diameters of 220 nm to 700 nm from top to bottom and height of 1μm. Without removing the Ni mask, a wet etching treatment was then performed by dipping both samples into a commercial developer AZ 826 MIF (90 ^oC for 30 min), which is a buffered TMAH solution [14, 16, 19]. The TMAH treatment not only removes the plasma damage but also smooths the lateral surface of the RIE-formed NWs and further reduces their diameter [14, 16]. Due to its strong anisotropic behavior, with negligible etching along the c-axis [14, 16, 19], very steep and uniform GaN NWs of 100 nm diameter for the device nanostructures and 200 nm diameter for the test nanostructures, were obtained. Figures 8.1(c) and 8.1(d) illustrate the fabricated top-

down GaN NW array after removal of the Ni mask from the top surface of device GaN NW nanostructures and test GaN NW nanostructures, respectively.

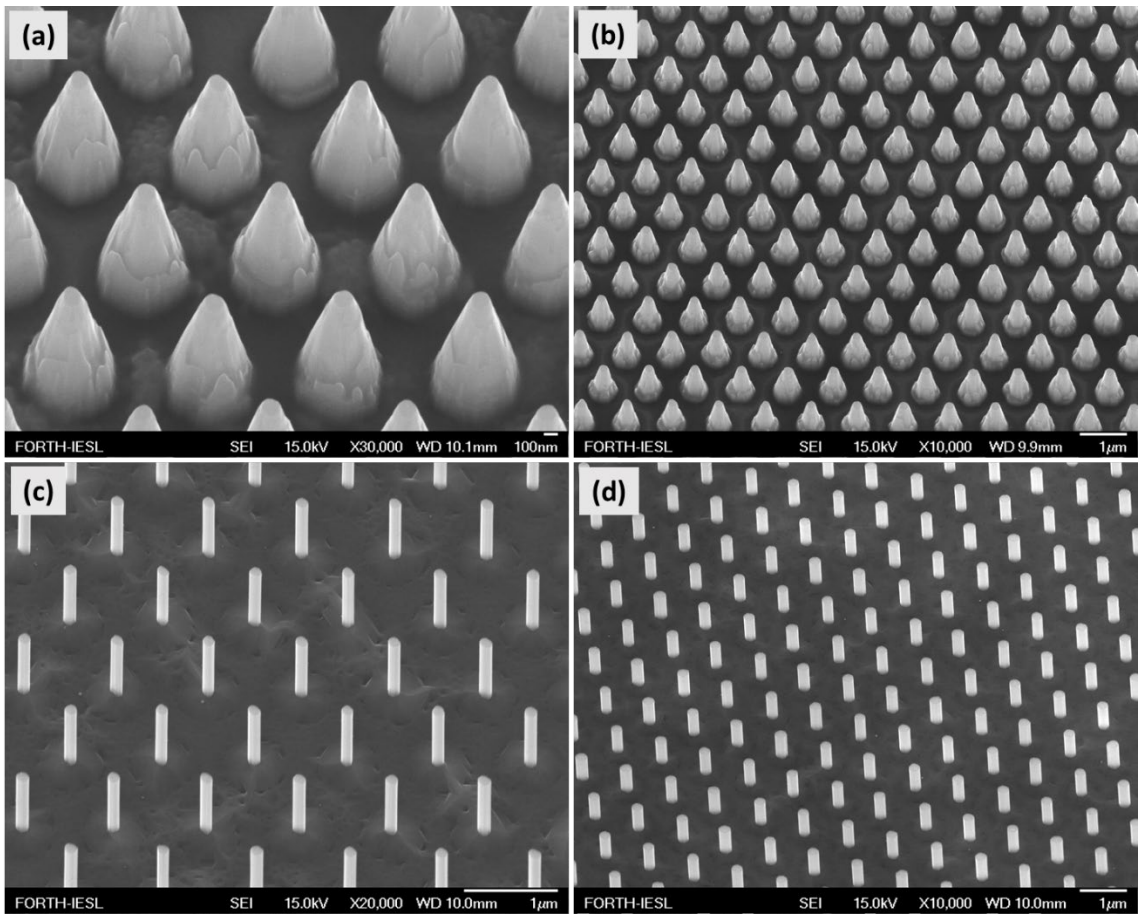


Figure 8.1: *SEM images in tilted-view of: (a) device nanostructures and (b) test nanostructures, consisting of trapezoidal GaN NW arrays after RIE of GaN film, and the final (c) device nanostructures and (d) test nanostructures, consisting of GaN NW arrays after RIE and anisotropic wet chemical etching in AZ 826 MIF developer.*

TMAH- or KOH-based anisotropic wet-etching treatment is widely used to remove the plasma damage and enhance the performance of nitride-based planar devices [19–21]. It is reported as an optimized pretreatment process for ohmic contact formation on p-type GaN [20] and for passivation of MOS-GaN capacitor devices [21], while there are also references to increase the maximum drain-source current and reduce the leakage current of Al_2O_3/GaN MOSFETs [19]. The exploitation of its properties in formation of top-down GaN-based NWs has recently gained significant attention by the first demonstration of GaN-based vertical NW FETs [14]. However, the etching mechanisms and kinetics are still not clear and further investigations for understanding this etching mechanism, are needed.

According to experimental insights of Yu et al. [22], a TMAH- or KOH-based wet etching treatment, after RIE of GaN film using a circular metal mask, results to the formation of hexagonal shape top-down GaN NWs, with smooth a-planes sidewalls. The

absence of metal mask on top of GaN NWs during this treatment, results to the formation of GaN NWs with irregular cross section and m-plane sidewalls [22]. In this case, the etching along the c-axis (vertical etching) is attributed to the high etch rate at the convex corners [23] between the top and sidewall planes [22]. The calculated temperature-dependent etch rate, when the metal mask is on the top of GaN NWs, is given by [22]:

$$R = R_o \exp\left(-\frac{E_a}{KT}\right) \quad (8.1)$$

where R is the etch rate at temperature T, K is the Boltzmann's constant, E_a is the activation energy of the chemical process, and R_o is a constant representing an attempt frequency for the reaction between OH^- ions and the GaN surface [24]. Therefore, according to Yu et al. [22] the etch rate is almost independent of NW diameter, while the estimated value of E_a (0.69 ± 0.02 eV) indicates that wet etching on a-plane sidewalls is a reaction-limited process, otherwise a value of E_a in the range of 0.04-026 eV would be expected for a diffusion limited process [25].

8.3 HRTEM characterization of GaN NW arrays

Vertical u-GaN NWs with diameter of 200 nm and height and pitch of 1μm (test structure), were systematically characterized using a JEOL 2010F and a JEM-2100 High Resolution Transmission Electron Microscopy (HRTEM) systems, by G. Martín, S. Estradé and Prof. F. Peiró at MIND-IN2UB, University of Barcelona.

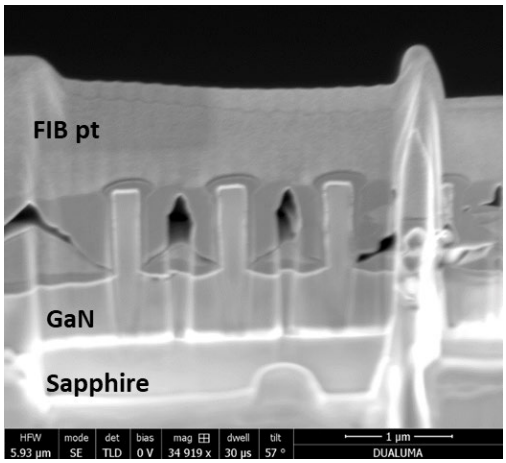


Figure 8.2: *SEM image of the HRTEM lamella preparation by FIB using the lift-out technique.*

HRTEM samples prepared using a focused-ion beam (FIB) lamella lift-out technique (Fig. 8.2) [26]. Initially, a platinum (Pt) protection layer was deposited at the site of interest, in order to obtain the lamella pattern. Afterwards, material was removed by ion milling above the target region and the underlying microstructure was revealed. Finally, a

micromanipulator used to place the lamella-sample to the e-chip for HRTEM investigation [26].

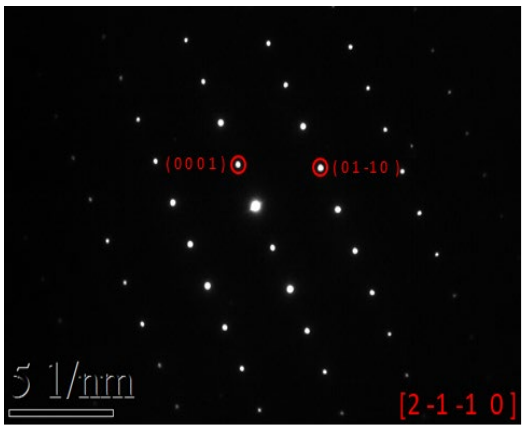


Figure 8.3: *Electron diffraction pattern of GaN NWs along the [2-1-10] zone axis.*

Figure 8.3 illustrates the electron diffraction pattern of GaN NWs along the [2-1-10] zone axis. The spotty aligned pattern of Fig. 8.3 reveals the good crystallinity and the hexagonal wurtzite structure of GaN NWs. Figure 8.4 shows in high magnification HRTEM images of the lateral sides of GaN NWs. Smooth and straight lateral edges are observed, resulting from the TMAH wet-etching treatment.

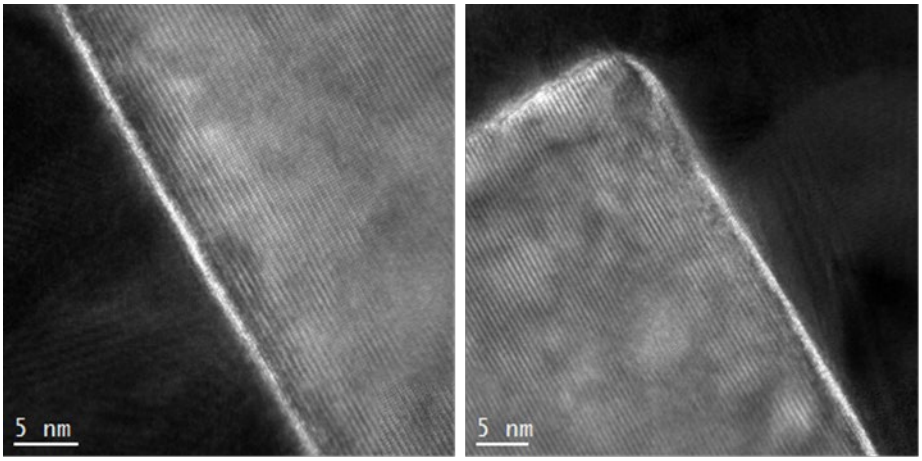


Figure 8.4: *HRTEM images of the lateral sides of top-down formatted u-GaN NWs.*

One major issue of the top-down GaN NWs is the presence of threading dislocations (TDs). HRTEM images of Fig. 8.5 indicate the presence of TDs along the formed GaN NWs in the corresponding areas of the planar epilayers. Figure 8.5(a) shows the interface between the GaN NW and the GaN film, with a TD starting from the GaN film and continuing along the GaN NW, while Fig. 8.5(b) shows a different GaN NW with a TD on its right lateral side.

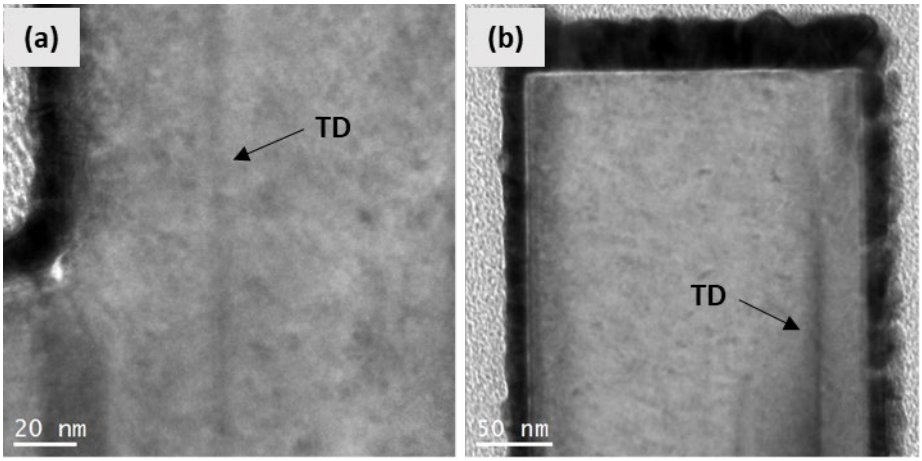


Figure 8.5: *HRTEM images showing the presence of threading dislocations (TDs): (a) at the interface between the GaN film and the GaN NW, and (b) on the lateral side of a GaN NW.*

The presence of TDs in top-down formed GaN NWs is probably the main disadvantage of the top-down method compared to spontaneously grown (bottom-up) defect free GaN NWs [27], [28]. The heteroepitaxial GaN (0001) layers on sapphire contain a high density of TDs that propagate almost vertically along the c-axis [29–30]. Thus, the top-down processed GaN NWs are expected to contain the TDs present in the corresponding areas of the planar epilayers, where each NW is formed, if there are no dislocation annihilation reactions. An estimation of the threading dislocation density (TDD) can be carried out by assuming that such GaN epilayers exhibit a TDD in the low 10^9 cm^{-2} range [29–30]. Considering that, each cylindrical NW with 200 nm diameter has a cross-sectional area of 3.14×10^{-10} cm^2 then we statistically expect that each GaN NW will contain at least one threading dislocation for TDD= 5×10^9 cm^{-2} [31] .

However, it may be also possible, using a proper treatment or epitaxial structure, for TDS to fully "escape" (by glide or climb) from the lateral NW sides due to their limited diameter. The movement of dislocations could be triggered by any stresses and it would be assisted by enhanced atomic diffusion at higher temperatures (e.g. annealing treatments). According to Conroy et al. [32] thermal annealing of RIE formed GaN NWs at 900 °C for 30 min can result to dislocation annihilation and recovery of the naturally occurred hexagonal non-polar facets of GaN NWs, without the use of a TMAH- or KOH-based wet etching treatment. Unfortunately, our laboratory equipment didn't support the application of so high temperatures for this time period. A rapid thermal annealing at 750 °C for 2 min was carried out, but HRTEM investigation of the samples didn't reveal a clear reduction of TDD of GaN NWs.

8.4 Fabrication of GaN Vertical-NW MESFETs

The V-NW arrays processed from the epitaxial device structure (300 nm n^+-GaN/600 nm u-GaN/500 nm n^+-GaN/30 nm AlN/ sapphire (0001)) were used for the fabrication of MESFET devices. GaN V-NW MESFET devices with channel comprising an

array of 900 (30 x 30) GaN NWs with 100 nm diameter and 1 μm pitch were fabricated. The schematic of Fig. 8.6(a) shows the overall configuration of the fabricated devices. Figure 8.6(b) illustrates a schematic for the lateral view of the device at source side, while Fig. 8.6(c) shows the corresponding schematic for the cross section of a single GaN NW.

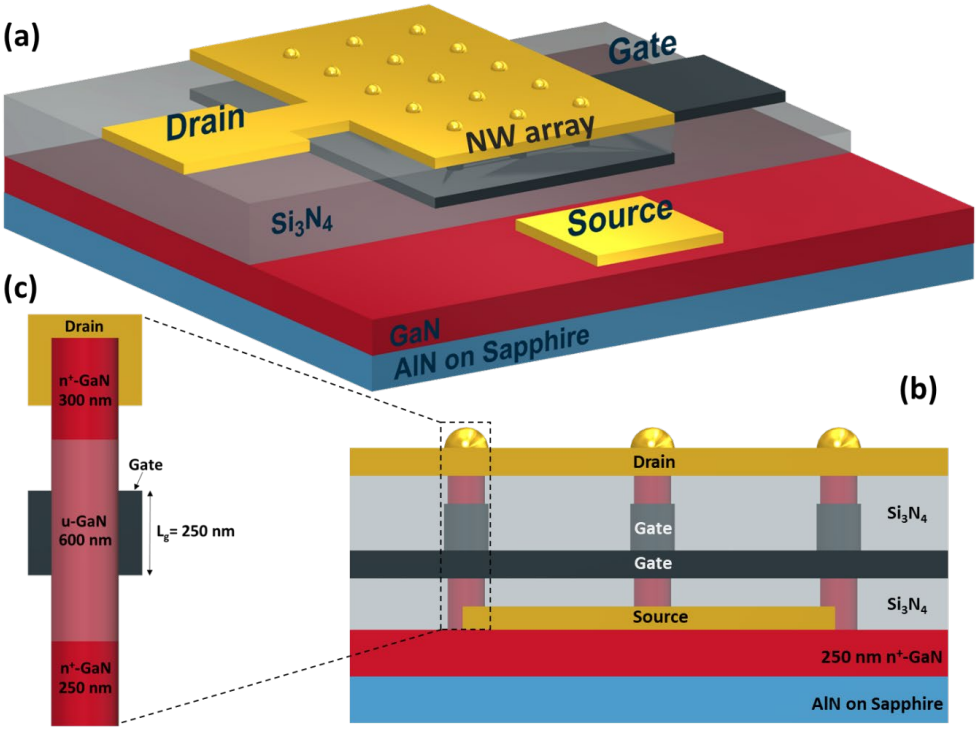
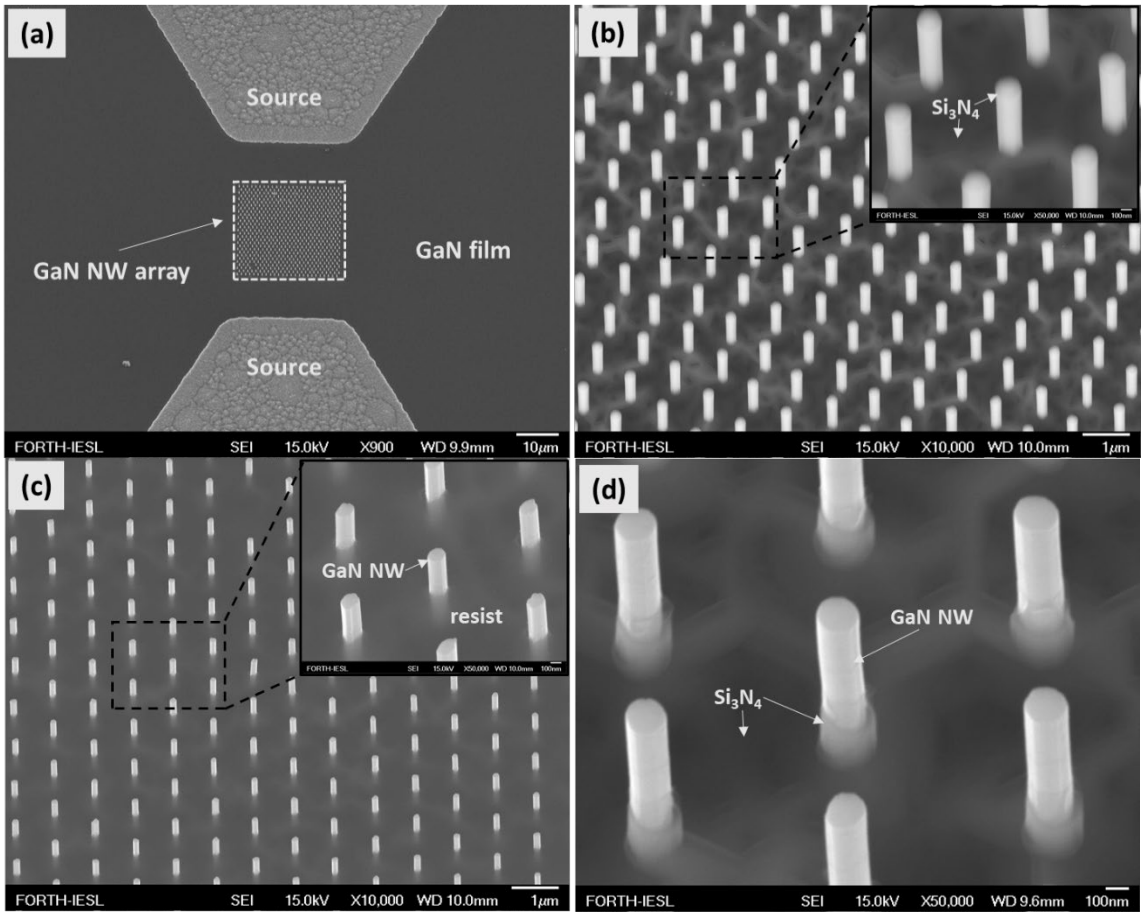


Figure 8.6: *Schematics showing: (a) The overall configuration of the fabricated GaN V-NW MESFET, (b) lateral view of the device at source side and (c) cross-sectional schematic of a single GaN NW after device fabrication.*

The fabrication of GaN V-NW MESFET devices started by formation of the Ti/Al/Ni/Au (30/170/30/70 nm) source contacts, using electron-beam evaporation, followed by rapid thermal annealing (RTA) at 750 °C (Fig. 8.7(a)). Afterwards, 100-nm thick Si_3N_4 was deposited by plasma-enhanced chemical vapor deposition (PECVD) as the source-gate insulating spacer (Fig. 8.7(b)).The Si_3N_4 film covered also the sidewalls of GaN NWs, as shown in high magnification at the inset of Fig. 8.7(b). In order to remove the Si_3N_4 from the upper part of GaN NWs, a positive resist with 1.5 μm thickness was spun to completely cover the NWs and an oxygen plasma treatment followed to etch back the resist to the desired thickness. The oxygen plasma was induced by application of 50 W power at pressure of 0.2 Torr, with 5 sccm oxygen flow and resulted to an etching rate of 3 nm/sec. After that, the sample was dipped into a buffered HF (BHF) solution with Si_3N_4 etch rate of 2 nm/sec and the resist served as the etch-stop mask to remove the Si_3N_4 only from the unprotected upper parts of GaN NWs (Fig. 8.7(c)). An acetone bath was then performed to completely remove the resist. Figure 8.7(d) shows the sample after resist removal and exhibits the Si_3N_4 shell that covers the sidewalls of GaN NWs up to a height of 350 nm.

Subsequently, in order to form the Schottky gate, 60-nm-thick Cr layer was initially deposited on the entire surface of the NWs by using electron-beam evaporation (Fig. 8.7(e)). In order to achieve uniform deposition of Cr metal layer, the sample during the evaporation was tilted at an angle of 30° and it was continuously rotated. The gate length (L_g) of 250 nm was set by removing the deposited Cr layer from the top 550 nm part of the NWs. This was accomplished by spinning a positive resist and thinning it down by oxygen plasma to the desired thickness. The Cr metal on the upper part of the GaN NWs that was not protected by resist was subsequently wet etched (Fig. 8.7(f)), using a commercial Cr etchant solution (Technic Chrome ETCH No1[33]). Afterwards, 150-nm-thick Si_3N_4 was deposited by PECVD as the gate-drain insulating spacer (Fig. 8.7(g)). By using a positive resist and BHF wet etching, as described earlier, the Si_3N_4 layer was removed from the top 200 nm part of GaN NWs (Fig. 8.7(h)) and Ti/Al/Ni/Au (15/85/15/20 nm) metals were deposited for drain contact formation by electron-beam evaporation (Fig. 8.7(i)). Finally, the fabrication was completed with the deposition of metal pads for all contacts by Cr/Au metallization. The pads were connected through windows of the Si_3N_4 film, previously opened at the source and gate contacts.

The final fully-processed GaN V-NW MESFET, consisting of an array of 900 (30 x 30) GaN NWs with 100 nm diameter, height of 1.15 μm, pitch of 1μm, channel length L_{ch}= 600 nm and gate length L_g = 250 nm, is illustrated in the SEM image of Fig. 8.7(j).



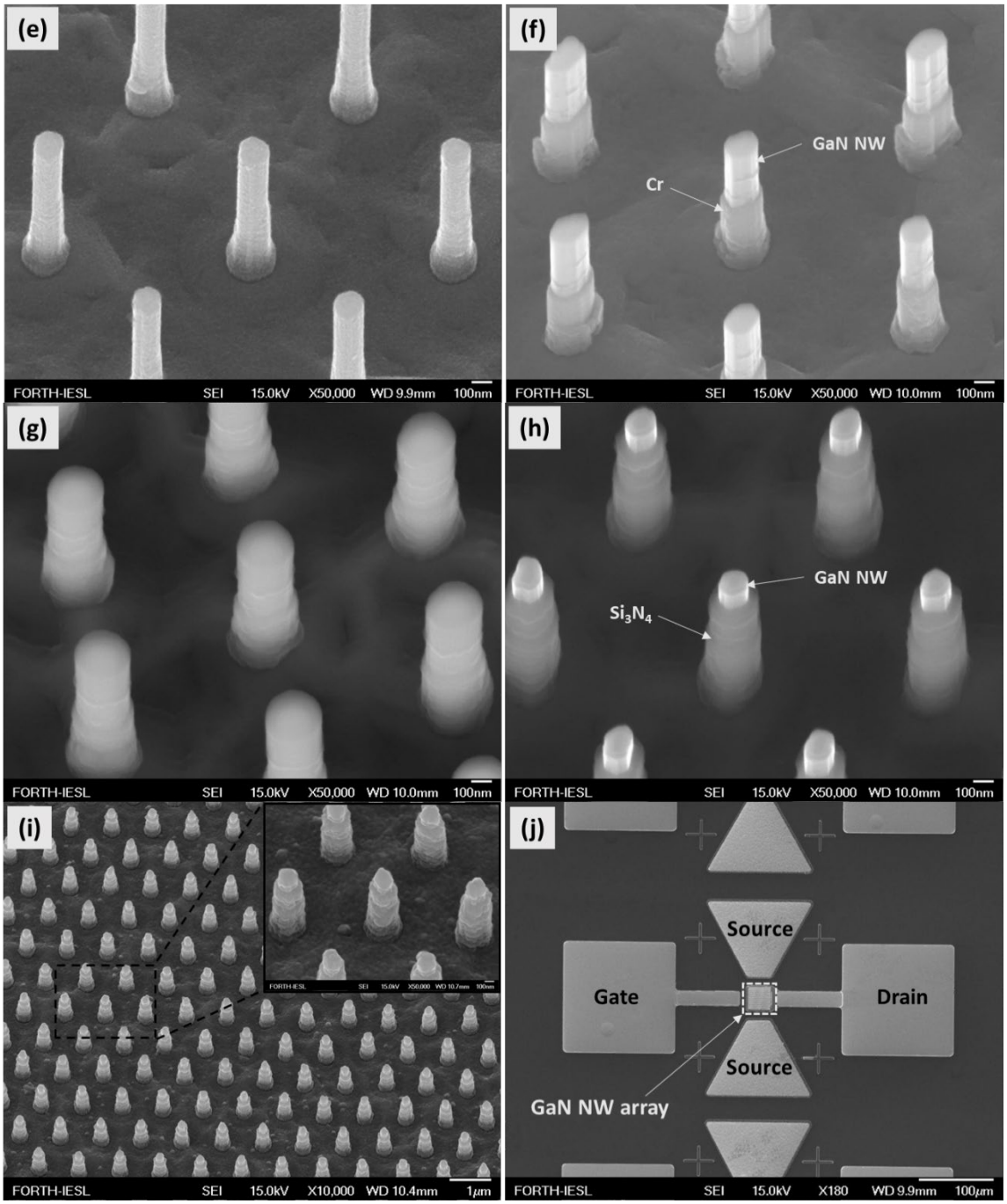


Figure 8.7: *SEM images in tilted-view showing the fabrication process flow for GaN V-NW MESFET after the following processing steps : (a) source Ti/Al/Ni/Au metals deposition and RTA at 750 °C, (b) PECVD deposition of 100-nm thick Si_3N_4 source-gate insulating spacer, (c) BHF wet etching of Si_3N_4 without removing the resist etch-stop mask, (d) removing the resist etch-stop mask, (e) electron-beam evaporation of 60-nm-thick Cr gate metal, (f) formation of gate with length L_g = 250 nm by a wet chemical treatment, (g) PECVD deposition of 150-nm thick Si_3N_4 gate-drain insulating spacer, (h) removal of Si_3N_4 from the 200 nm top part of GaN NWs, (i) drain Ti/Al/Ni/Au metals deposition and (j) the final fully-processed vertical GaN NW MESFET.*

8.5 Results and discussion

The fabricated devices were characterized by DC I-V measurements using a Keithley 4200 semiconductor characterization system. Figure 8.8 depicts the DC output (I_{ds}-V_{ds}) and transfer (I_{ds}-V_{gs}) characteristics of a fabricated GaN V-NW MESFET. The current density in Fig. 8.8 has been calculated using the formula:

$$J_{ds} = \frac{I_{ds}}{xS_{NW}} = \frac{4I_{ds}}{x\pi d^2} \quad (8.2)$$

where *x=900* is the total number of V-NWs, S_{NW} is the cross-sectional area and *d* the diameter of each one of the GaN V-NWs that comprise the V-NW MESFET channel.

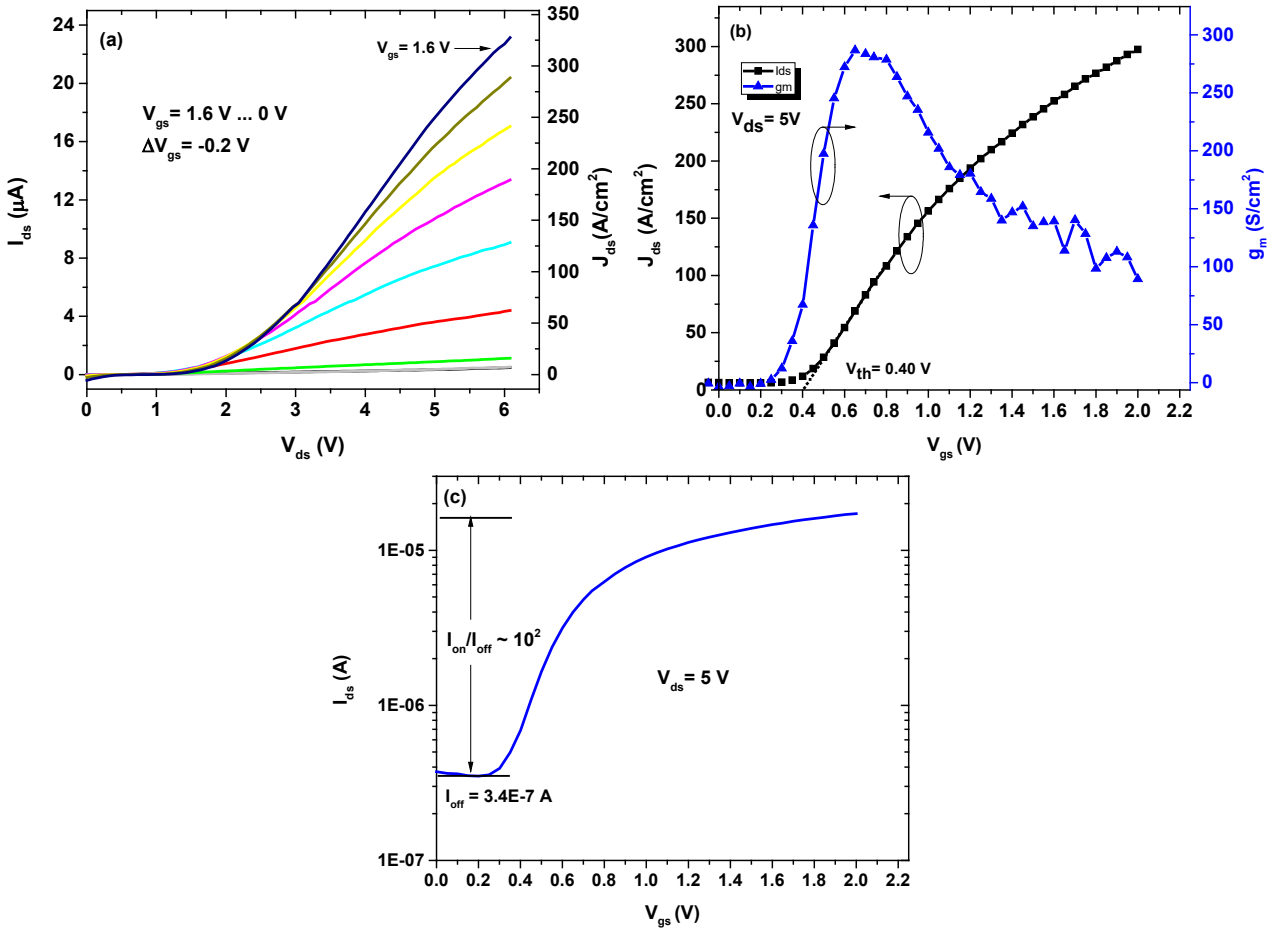


Figure 8.8: *DC characterization results for a GaN V-NW MESFET : (a) Output (I_{ds}-V_{ds}) characteristics, (b) Transfer (I_{ds}-V_{gs}) characteristics at V_{ds}= 5 V and (c) Transfer (I_{ds}-V_{gs}) characteristics in logarithmic scale at V_{ds}= 5 V.*

According to the I_{ds}-V_{ds} output characteristics (Fig. 8.8(a)), the GaN V-NW MESFETs exhibited a maximum drain-source current density ($J_{ds,max}$) of 330 A/cm^2. The I_{ds}-V_{gs} transfer characteristics at V_{ds} = 5 V (Fig. 8.8(b)) exhibited maximum transconductance ($g_{m,max}$) of 285 S/cm^2 and threshold voltage (V_{th}) of +0.4 V. The threshold voltage was defined as the gate bias intercept of the linear extrapolation of drain current to J_{ds}= 0 A.

The off-state current (I_{off}) was 4.3 x 10^{-7} A and the on/off current ratio was ~10^2, as shown in Fig. 8.8(c), which shows in current logarithmic scale the I_{ds}-V_{gs} characteristics. Two non-idealities present in the I_{ds}-V_{ds} characteristics of Fig. 8.8(a) are the large output conductance at high V_{ds} and the non-linear behavior at low V_{ds}. With the exception of the threshold voltage, the other performance figures of the GaN V-NW MESFETs are rather poor and could be significantly improved by further development of the technology in the future.

Better device performances have been reported in the literature for MOS-gate GaN V-NW FETs [13–15] , although a straightforward comparison is impossible due to the different type of gate contact (MOS) and GaN NW dimensions (diameter and length). On/off current ratios of 10^7-10^9 have been reported in Refs. [13, 14, 16], whilst the maximum current density of 219 kA/cm^2 has been achieved by Yu et al. [13] using NWs with 500 nm diameter. However, a much smaller current density of 2.75 kA/cm^2 has been reported in Ref. [15] using larger diameter (800 nm) NWs. These variations are rather indicative for the early stage of development also of the GaN V-NW MOSFET devices and suggest the need for improved fundamental understanding.

A major issue of the V-NW MESFET devices of the present work that consisted of 100 nm diameter NWs were the high source (R_s) and drain (R_d) series resistances, due to the fully depleted undoped GaN (u-GaN) NW regions (access regions) between the source and gate and the gate and drain electrodes (Fig. 8.6(c)). The carrier depletion inside the NW crystal, as discussed analytically in section 6.2, is induced by surface states on the free lateral sides of the GaN NW that pin the Fermi level and create a band bending along the radius of the NW (Fig. 6.1), as if a Schottky barrier contact was present on the surface [34]. The critical point is that the u-GaN region of the GaN NWs with 100 nm diameter and doping concentration of N_D= 10^{16} cm^{-3}, was fully depleted (Fig. 6.1(b)). The depleted source and drain access u-GaN regions were essentially insulating material and this was clearly the cause of the nonlinear I_{ds}-V_{ds} relation at low V_{ds} regime (Fig. 8.8(a)), where a quadratic dependence of current (I_{ds}) on voltage (V_{ds}) was observed that is characteristic of space charge limited (SCL) conduction [35–36].

Semiconductor NWs are particularly sensitive to conduction SCL effects [35–36] due to low intrinsic carrier concentration, poor screening of charge (characteristic in high-aspect ratio systems) and surface carrier depletion effects. It should be pointed out that the source contacts exhibited ohmic behavior with specific contact resistance of 3.7 x 10^{-5} Ω cm^2 in reference linear transmission line method (TLM) structures, which were fabricated on a planar part of the Si-doped n$^+$-GaN layer, simultaneously with the formation of the GaN NW source contacts. Although we could not measure directly the contact resistance of the drain contacts made also on an n$^+$-GaN layer, a similar ohmic behavior is expected. Thus, the rectifying I–V relationship at low V_{ds} regime (Fig. 8.8(a)) cannot be attributed to imperfect ohmic contacts at the source or drain region.

The V-NW MESFETs of this work consisted of d= 100 nm NWs and exhibited $V_{th}\approx$ 0.40 V. It should be pointed out that the analysis of surface depletion of GaN NWs (section 6.2) caused by Fermi level pinning at the surface, is also applicable by replacing the surface potential $q\Phi_B$ of Eqs. 6.1 to 6.5 with the barrier height induced by a Schottky

barrier metal contact, as in the gate region of the V-NW MESFETs. In this case, d_{crit} according to Eq. 6.2 or Eq. 6.3 is the NW diameter that would result to V-NW MESFETs with V_{th}= 0 V. Normally-off (V_{th}< 0) and normally-on (V_{th}≥ 0 V) devices would require d> d_{crit} and d ≤ d_{crit}, respectively. Therefore, the application of V_{gs}= V_{th} on the Schottky gate corresponds to the condition of W_{dep}= d/2= R_{NW}, where R_{NW} is the radius of the cylindrical shape GaN NW. Assuming that the Cr/GaN Schottky contact resulted to $q\Phi_B$= 0.55 eV [37–38], then a background electron concentration n= N_D-N_A ≈ 10^{16} cm^{-3} was estimated from the one-dimensional Eq. 6.1 for W_{dep}= d/2= 50 nm and $q\Phi_B$ replaced by $q\Phi_B$-qV_{th}≈ 0.15 eV. The electron concentration n≈ 10^{16} cm^{-3} is also typical for the undoped (non-intentionally doped) GaN epilayers grown in the same PAMBE system.

The high R_s and R_d and the nonlinear I_{ds}-V_{ds} behavior do not allow to extract electron mobility from the measured device output characteristics. However, the electron mobility is expected to be similar with the typical value of ~300 cm^2/Vs determined by Hall-effect measurements for u-GaN buffer layers on sapphire, grown in the same PAMBE system.

The I_{ds}-V_{ds} characteristics (Fig. 8.8(a)) of the fabricated GaN V-NW MESFET devices exhibited a difficulty to achieve I_{ds} saturation. This is not clearly understood and we could only speculate upon the contribution of various potential causes. A clear effect of the high R_s and R_d series resistances, due to carrier depletion in the source and drain access regions will be the shift of the required V_{ds} for current saturation to higher values. However, the increased V_{ds} was leading to catastrophic failure of GaN V-NW MESFETs, probably due to thermal effects, and prohibited to test higher V_{ds} voltages. A voltage drop $I_{ds}R_s$ would also limit the part of the positive V_{gs} that is actually applied between gate and channel to increase its conductance. Furthermore, the quadratic dependence of current on voltage at the source and drain access regions (SCL conduction mechanism) would vary the effective series resistances with increasing V_{ds}, which could have complicated the overall I_{ds}-V_{ds} characteristics. Leakage currents due to non-optimized processing could not be ruled out. Finally, short-channel effects, such as the channel length (L) modulation that takes place in devices with small channel length [39–41] may also have contributed.

The miniaturization of device technology could dominate short-channel effects in FET devices, resulting in significant deviations from ideal I-V behavior and may also affect the device performance [39–41]. In short channel devices, the subthreshold leakage is enhanced by the drain induced barrier lowering (DIBL) effect [39–41], while the threshold voltage and the off current are both modulated by the width of the transistor, giving also rise to leakage currents [39–41]. A FET device is considered to have "short-channel", when the channel length is comparable to the depletion layer width of the source ($W_{dep(S)}$) and drain ($W_{dep(d)}$) junction, even without any bias applied [39–41], as in case of fully depleted GaN NWs (section 6.2). An important characteristic of short-channel effects is the channel length (L) modulation that affects the saturation current of transistor. In the ideal case, I_{ds} in saturation region becomes independent of V_{ds} as the channel is pinched off at the drain end. Practically, the channel pinch-off point is moved slightly towards the source by an amount of ΔL. In large channel devices this effect is negligible, but for short

channel devices ΔL/L becomes important and in saturation region I_{ds} increases as V_{ds} increases [41].

The performance of the fabricated V-NW MESFET devices was also limited by the relatively low barrier height of the Cr/GaN Schottky contact that is disadvantageous for reducing leakage currents. A process optimization with a gate metal of higher workfunction (i.e. Nickel), possibly compatible with the other steps of the NW device fabrication, could significantly enhance the device characteristics in the future.

Another issue that should be discussed for the fabricated V-NW MESFETs concerns the presence of threading dislocations (TDs) in the GaN NWs, as described in section 8.3. The presence of a TD would deteriorate the electron transport along the NW-channel and may also degrade the Schottky barrier contact, resulting to high leakage current [42]. As it was discussed previously, on the average 40% of GaN NWs with 100 nm diameter, processed from a GaN epilayer with TDD ~5 x 10^9 cm^{-2} [31], would contain one TD in their volume. Thus, a variation of the electrical properties of the parallel connected NW-channels would occur in a V-NW MESFET device. This problem should have affected the devices fabricated in this work. In the future, it can be overcome by top-down processing of GaN NWs from homoepitaxial layers grown on free-standing GaN substrates or preferably by the bottom-up approach of spontaneous growth of GaN NWs by PAMBE [43–44]. The latter is technically challenging, especially concerning the proper control of selective area growth [45–47], but it is very promising as a low cost process that could provide high structural quality NWs that could be integrated on dissimilar substrates, such as Si.

The band bending along the NW radial axis due to surface states (section 6.2), results to a number of free electrons inside the NW not proportional to its cross sectional area but to its non-depleted part. An effective diameter (d_{eff}) could be defined, which contributes to conduction and is calculated by subtracting the value of the critical NW diameter (d_{crit}) from the whole NW diameter (d_{NW}). A sufficiently large NW diameter can result to almost negligible contribution of d_{crit} to d_{eff}, which allows high current density. Thus, an intrinsic problem of high access resistances appears for normally-off GaN V-NW MESFETs that should be optimized by improved doping profile and possible development of a self-aligned gate process technology. The development of proper passivation for the lateral NW surfaces is also important for the optimization of the devices. GaN NWs with core-shell structure, formed by the deposition of a wider bandgap layer such as AlN on their lateral sides, could improve the electron transport by limiting scattering from surface charges.

By controlling the diameter of GaN NWs, a wide range of applications can be achieved by GaN V-NW transistors. For a fixed N_D, different GaN NW diameters can provide both normally-off and normally-on transistors for low power (digital) logic applications. By increasing the number and the diameter of GaN NWs, transistors for high power applications may be fabricated, possibly in combination with more complex device geometries. The variation of diameters of GaN NWs can be easily achieved by top-down NW formation approaches.

8.6 Conclusions

The research presented in this chapter contributes to the development of GaN V-NW FETs, the optimization of nanofabrication processes and the understanding of implications of fabrication aspects on the operation and performance of devices. HRTEM investigation of u-GaN NWs, formed by a top-down fabrication process, indicated the existence of threading dislocations along the GaN NWs. A nanofabrication process with comprehensive description of all processing steps was proposed and validated with the demonstration of GaN V-NW MESFETs. The channel comprised an array of 900 (30x30) GaN NWs with diameter of 100 nm, processed from a GaN epilayer on sapphire (0001) substrate grown by PAMBE. Normally-off operation and threshold voltage of +0.4 V were observed in V-NW MESFETs with Cr all-around Schottky gate contacts with 250 nm length. A rather low maximum drain-source current density ($J_{ds,max}$) of 330 A/cm^2 and maximum transconductance ($g_{m,max}$) of 285 S/cm^2 were obtained for the fabricated devices. The I-V characteristics were dominated by the high source and drain access resistances resulting from electron depletion due to Fermi level pining by surface states at the lateral GaN NW sides. Optimization of the doping profile in the GaN epilayers, surface passivation and a self-aligned gate process technology could address this issue. Overall, a technological platform for fabrication of GaN V-NW MESFETs was developed, with exploitation potential for both low power (digital) and high power device applications, based on GaN and other relevant semiconductors.

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Chapter 9

Conclusions and future perspectives

9.1 Conclusions

The dissertation covered a wide range of fabrication aspects of GaN-based nanostructures and devices, as well as their realization, physical analysis and performance assessment. The research was focused on the processing and properties of field-effect transistors (FETs) based on nanofins of a GaN HEMT structure (FinHEMTs) and GaN vertical nanowires (V-NW FETs).

Bottom-up GaN nanowire devices

The electrical transport properties of unintentionally doped GaN NWs grown spontaneously or selectively by PAMBE (bottom-up processes) with diameters ranging from 30 to 140 nm and lengths ranging from 500 to 1900 nm were determined. The achievements and overall conclusions for bottom-up GaN NW devices are listed as follows:

- Individual GaN NW devices with multiple ohmic contacts per GaN NW were fabricated
- Surface states at the lateral sides of GaN NWs induce Fermi level pinning at the surface and corresponding carrier depletion (W_{dep}) inside the GaN NW crystal
- The estimated doping concentration of GaN NWs was in the range of 5.0 – 5.5 x 10^{17} cm^{-3}, assuming a barrier height of 0.55 eV at the GaN NW surface
- A critical GaN NW diameter of ~87 nm was estimated for full depletion of GaN NW
- The GaN NW resistivity of 0.01-0.03 Ωcm was calculated by assuming an effective GaN NW diameter
- Vertical p-Si/n-GaN NW heterojunction diodes were fabricated for the first time, to our knowledge, and the results exhibited a clear rectifying behavior
- The bottom-up GaN NWs could not provide the accuracy of the nanostructures that is required for fabrication of vertical NW FETs

AlN/GaN/AlN MOS-FinHEMTs

The exploitation of the two-dimensional electron gas (2DEG) channel of an AlN/GaN/AlN double barrier heterostructure in the fabrication of MOS-FinHEMTs has been investigated by combining experimental device fabrication and characterization with device simulations. AlN/GaN/AlN nanofins were formed by a top-down process using three processing steps: nanopatterning by electron-beam lithography (e-beam), reactive-ion etching (RIE) and anisotropic wet-chemical etching. The achievements and overall conclusions for AlN/GaN/AlN MOS-FinHEMTs are listed as follows:

- Single-fin AlN/GaN/AlN MOS-FinHEMTs with different fin widths (W_{fin}) of 200, 350, 500 and 650 nm were fabricated for the first time
- Experimental results and device simulations exhibited a positive shift of threshold voltage (V_{th}), in comparison to a reference planar-gate device, with reduction of W_{fin} due to the lateral electric field of the gate structure
- Device simulations of single-fin MOS-FinHEMTs indicated that normally-off operation will become possible for W_{fin} less than 17 nm for fully strained AlN barrier and W_{fin} less than 31 nm for fully relaxed AlN barrier
- A reduction of maximum drain-source current per top gate width ($I_{ds,max}/W_g$) with decreasing W_{fin} in the range of W_{fin}= 200–650 nm may result by increased ohmic contact resistance and in general, parasitic resistances
- Parasitic resistances should be the main cause of the significant inconsistencies in the comparative currents of FinHEMT and planar HEMT devices revealed from the overall literature reports on AlGaN/GaN structures
- For W_{fin} < 200 nm, $I_{ds,max}/W_g$ was predicted to decrease significantly with decreasing W_{fin}, due to lateral carrier depletion in the nanofins
- The effect of the source-gate and source-drain distances, as well as the gate oxide thichness, on the $I_{ds,max}/W_g$ and V_{th} were calculated

Top-down vertical GaN nanowire MESFETs

The development of GaN all-around (wrap) gate vertical nanowire (V-NW) FETs with Schottky barrier gate has been investigated. Vertical GaN NWs were formed by a top-down process using three processing steps: nanopatterning by electron-beam lithography (e-beam), reactive-ion etching (RIE) and anisotropic wet-chemical etching. The achievements and overall conclusions for vertical GaN nanowire MESFETs are listed as follows:

- A full device fabrication process was developed and GaN vertical NW FETs with a Schottky barrier gate (V-NW MESFETs) were fabricated for the first time. They consisted of an array of 900 (30 × 30) GaN NWs with the narrowest reported diameter of 100 nm and all-around gate length of 250 nm
- The devices exhibited normally-off operation and threshold voltage of +0.4 V
- A maximum drain-source current density ($J_{ds,max}$) of 330 Acm^{-2} and a maximum transconductance ($g_{m,max}$) of 285 Scm^{-2} was observed
- The I–V characteristics were dominated by the high source and drain access resistances, resulting from electron depletion, induced by the band bending toward the lateral sides of the GaN NWs
- Optimization of the doping profile, surface passivation and possible development of a self-aligned gate process technology could address the high access resistances

9.2 Future perspectives

According to the predictions of the 2018 "International Roadmap for Devices and Systems (IRDS)" for low power device applications [1–2], vertical NW Gate-All-Around (GAA) technology is expected to succeed FinFET technology and will dominate until 2034. Advanced materials are expected to replace Si, while III-V NWs are anticipated to be used for n-channel MOSFETs from 2022, together with strained Si and Ge [1–2]. The transition to high power devices can be easily achieved by increasing the number of NWs or nanofins. The results, obtained in this work, pointed out the great potentials of FETs based on GaN nanofins and vertical NWs, but also indicated that further systematic studies are needed to improve the understanding of the structures and to optimize the design and performance of devices.

Primarily, the use of high quality PAMBE grown (bottom-up) III-V semiconductor nanostructure materials may enhance the performance of fabricated devices. Therefore, the ongoing systematic studies of the growth of GaN-based NWs and nanofins should be continued. The selective area growth (SAG) of GaN NWs and nanofins at selected substrate sites by PAMBE may offer this high quality nanostructure material. Thus, it is of high priority to intensity the research efforts for optimizing the SAG processes. Otherwise, significant effort is needed to improve the quality of the top-down formed GaN NWs and nanofins. The presence of threading dislocations (TDs) in these structures is attributed to the corresponding TDs present in the areas of the planar epilayer, where each NW is formed. However, it may be possible for TDs to fully "escape" (by glide or climb) from the lateral NW sides due to their limited diameter. The movement of dislocations could be triggered by any stresses and it would be assisted by enhanced atomic diffusion at higher temperatures (e.g. annealing treatments)[3]. According to Conroy et al. [3] thermal annealing of RIE formed GaN NWs at 900 °C for 30 min can result to dislocation annihilation, as well as of recovery of the naturally occurred hexagonal non-polar facets of GaN NWs, without the use of a TMAH- or KOH-based wet etching treatment (GaN at the lateral NW sides is decomposed and Ga, N atoms are evaporated).

The exploitation of the two-dimensional electron gas (2DEG) channel of an AlN/GaN/AlN double barrier heterostructure for MOS-FinHEMT devices has been investigated by combining fabrication, DC I-V measurements and simulations of single-fin MOS-FinHEMT devices. The bottom GaN/AlN interface induces a strong electric field within the GaN buffer layer and thus a large barrier (back barrier) for electron motion toward the substrate, which is expected to reduce leakage currents and enhance the performance of devices [4]. However, modeling insights indicated the critical role of parasitic resistances and device characteristics (fin length, source to gate distance and dielectric thickness) for the performance of MOS-FinHEMTs. Optimized device design and processing require large source-drain contact areas in order to minimize the contact resistance, reduced fin length and source to gate distance, while the dielectric thickness is a critical parameter for fine tuning of normally off operation, since an accurate control of threshold voltage can be achieved by varying it. In this work, the MOS gate dielectric

was Al_2O_3, deposited by atomic layer deposition (ALD). ALD is the optimum method for depositing Al_2O_3. However, a critical issue at insulator/semiconductor interface concerns the presence of interface states that could result to any performance irreproducibility, create current instabilities and deteriorate the RF performance of devices. The overall reported results [5–8] have revealed significant inconsistency in the preferable pretreatment surface preparation of GaN before deposition of Al_2O_3, in order to reduce the interface trap density (D_{it}). A different dielectric material with enhanced dielectric properties [9] or a dielectric stack [10–11] may also be used, while the influence of processing steps of top-down approaches on the GaN semiconductor surface has to be investigated, as it may induce process-related defects and contaminants. A selective area grown MOS-FinHEMT device with in-situ deposition of the gate dielectric is probably the ultimate option.

Regarding vertical NW GAA technology, GaN V-NW MESFET devices with channel consisting of an array of 900 (30×30) GaN NWs with 100 nm diameter were fabricated. The I–V characteristics were dominated by the high source and drain access resistances resulting from electron depletion due to Fermi level pinning by surface states at the lateral GaN NW sides. Optimization of the doping profile in the GaN epilayers, surface passivation and a self-aligned gate process technology could address this issue. A gate metal of higher workfunction (i.e. Ni) instead of Cr could also significantly enhance the device characteristics; otherwise, a MOS gate may be preferred in terms of reduction of leakage current and increased operational voltage. The critical parameters of FinHEMT devices and the previously discussed ways for FinHEMT device optimization are also applicable to this technology. A selective area grown vertical GaN NW transistor with optimized process and in situ gate dielectric deposition is expected to overcome most of the aforementioned issues.

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Appendix: Publications

A.1 PUBLICATIONS IN JOURNALS

1. ***Nanofabrication of normally-off GaN vertical nanowire MESFETs***
   G. Doundoulakis, A. Adikimenakis, A. Stavrinidis, K. Tsagaraki, M. Androulidaki , F. Iacovella, G. Deligeorgis , G. Konstantinidis and A. Georgakilas
   NANOTECHNOLOGY 30, 285304 (2019)
2. ***Experimental and modeling insight for fin-shaped transistors based on AlN/GaN/AlN double barrier heterostructure***
   G. Doundoulakis, A. Adikimenakis, A. Stavrinidis, K. Tsagaraki, M. Androulidaki, G. Deligeorgis , G. Konstantinidis and A. Georgakilas
   SOLID STATE ELECTRONICS 158, 1 (2019)
3. ***Bandgap, electrical and structural properties of thick InN (0001) films grown under optimal conditions***
   A. Adikimenakis, M. Androulidaki, E. Foundoulaki Salhin, K. Tsagaraki, G. Doundoulakis, J. Kuzmik and A. Georgakilas
   JOURNAL OF PHYSICS: CONF. SERIES 1190, 012010 (2019)
4. ***Multimodal microscopy test standard for scanning microwave, electron, force and optical microscopy***
   O.C. Haenssler, M. F. Wieghaus, A. Kostopoulos, G. Doundoulakis, E. Aperathitis, S. Fatikow and G. Kiriakidis
   JOURNAL OF MICRO-BIO ROBOTICS 14, 51 (2018)
5. ***Selective-area growth of GaN nanowires on SiO_2-masked Si (111) substrates by molecular beam epitaxy***
   J.E. Kruse, L. Lymperakis, S. Eftychis, A. Adikimenakis, G. Doundoulakis, K. Tsagaraki, M. Androulidaki, A. Olziersky, P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand, T. Koukoula, Th. Kehagias, Ph. Komninou, G. Konstantinidis and A. Georgakilas
   JOURNAL OF APPLIED PHYSICS 119, 224305 (2016)

A.2 PUBLICATIONS IN PROCEEDINGS OF INTERNATIONAL CONFERENCES

1. ***Test standard for Light, Electron and Microwave Microscopy to enable robotic processes***
   O. C. Haenssler, A. Kostopoulos, G. Doundoulakis, E. Aperathitis, S. Fatikow and G. Kiriakidis
   MARSS 2017 proceedings, International Conference on Manipulation, Automation and Robotics at Small Scales, Montreal, Canada (IEEE 2017)
2. ***A study on the fabrication of devices and the characterization of GaN nanowires and the GaN/Si heterojunction***
   G. Doundoulakis, A. Bairamis, E. Tsikritsaki, A. Stavrinidis, Ch. Zervos, G. Konstantinidis, M. Kayampaki, S. Eftychis, J. Kruse, A. Adikimenakis and A. Georgakilas
   38th WOCSDICE proceedings, Workshop on Compound Semiconductor Devices and Integrated Circuits, 15-18 June 2014, Delphi, Greece, pp. 129-130 (book of extended abstracts)
3. ***Nanopatterning of Si (111) substrates for selective growth of III-nitride nano-wires by plasma-assisted molecular beam epitaxy***
   P. Dimitrakis, A. Olziersky, V. Ioannou-Sougleridis, P. Normand, J. E. Kruse, S. Eftychis, G. Doundoulakis, K. Tsagaraki, M. Androulidaki, G. Konstantinidis and A. Georgakilas
   38th WOCSDICE proceedings, Workshop on Compound Semiconductor Devices and Integrated Circuits, 15-18 June 2014, Delphi, Greece, pp. 131-132 (book of extended abstracts)
4. ***Importance of substrate temperature in one-step or two-step process of spontaneous GaN nanowire growth by plasma-assisted molecular beam epitaxy***
   S. Eftychis, J. Kruse, L. Lymperakis, K. Tsagaraki, G. Doundoulakis, M. Androulidaki, T. Koukoula, Th. Kehagias, Ph. Komninou and A. Georgakilas
   38th WOCSDICE proceedings, Workshop on Compound Semiconductor Devices and Integrated Circuits, 15-18 June 2014, Delphi, Greece, pp. 173-174 (book of extended abstracts)

A.3 PRESENTATIONS IN INTERNATIONAL CONFERENCES

1. ***Study of the fabrication of vertical GaN nanowire transistors***
   G. Doundoulakis, A. Adikimenakis, A. Stavrinidis, K. Tsagaraki, M. Androulidaki , F. Iacovella, G. Deligeorgis , G. Konstantinidis and A. Georgakilas
   45th MNE, International Conference on Micro & Nano Engineering, 23 – 26 September, Rodos Palace Hotel, Rhodes, Greece (2019)
2. ***Experimental and modeling study of FinHEMT transistors based on AlN/GaN/AlN heterostructure***
   G. Doundoulakis, A. Adikimenakis, A. Stavrinidis, K. Tsagaraki, M. Androulidaki, G. Deligeorgis , G. Konstantinidis and A. Georgakilas
   45th MNE, International Conference on Micro & Nano Engineering, 23 – 26 September, Rodos Palace Hotel, Rhodes, Greece (2019)
3. ***Substrate effects in selective area growth of GaN nanowires by plasma-assisted molecular beam epitaxy***
   A. Adikimenakis, G. Doundoulakis, S. Eftychis, K. Tsagaraki, M. Androulidaki and A. Georgakilas
   45th MNE, International Conference on Micro & Nano Engineering, 23 – 26 September, Rodos Palace Hotel, Rhodes, Greece (2019)
4. ***Transferrable dielectric DBR membranes for versatile GaN-based polariton and VCSEL technology***
   E.A. Amargianitakis, S. Kazazis, G. Doundoulakis, G. Stavrinidis, G. Konstantinidis, E. Delamadeleine, E. Monroy and N.T. Pelekanos
   45th MNE, International Conference on Micro & Nano Engineering, 23 – 26 September, Rodos Palace Hotel, Rhodes, Greece (2019)
5. ***Test standard for Light, Electron and Microwave Microscopy to enable robotic processes***
   O.C. Haenssler, A. Kostopoulos, G. Doundoulakis, E. Aperathitis, S. Fatikow and G. Kiriakidis
   MARSS 2017, International Conference on Manipulation, Automation and Robotics at Small Scales, Montreal, Canada (2017)
6. ***Evaluation and understanding of size effects on the conductivity of spontaneously grown GaN nanowires***
   G. Doundoulakis, A. Stavrinidis, S. Eftychis, M. Androulidaki, K. Tsagaraki, M. Kayambaki, G. Konstantinidis and A. Georgakilas
   EUROMAT 2017, European Congress and Exhibition on Advanced Materials and Processes, 17-22 September, Thessaloniki, Greece (2017)
7. ***SiO_2-mask patterns for selective-area growth of GaN nanowires on Si(111) substrates***
   J. Kruse, S. Eftychis, A. Adikimenakis, G. Doundoulakis, K. Tsagaraki, M. Androulidaki, A. Olziersky, P. Dimitrakis,V. I.-Sougleridis, P. Normand, T. Koukoula, T. Kehagias, Ph. Komninou and A. Georgakilas

EMRS 2015, European Materials Research Society 2015 fall meeting, 15 -18 September, Warsaw, Poland (2015)

8. ***Electrical characterization of individual GaN Nanopillars synthesized by Plasma assisted Molecular Beam Epitaxy***
   G. Doundoulakis, A.Stavrinidis, S. Eftychis, J. Kruse, M. Androulidaki, K. Tsagaraki, M. Kayambaki, G. Konstantinidis, P. Normand, K. Zekentes and A. Georgakilas
   ICNS-11, International Conference on Nitride Semiconductors, 30 August – 4 September, Pekino, China (2015)

9. ***Effectivity of SiO_2-Mask Patterns for Selective-Area Growth of GaN Nanowires on Si(111) Substrates***
   J. E. Kruse, S. Eftychis, L. Lymperakis, A. Adikimenakis, G. Doundoulakis, K. Tsagkaraki, M. Androulidaki, E. Iliopoulos, P. Tzanetakis, A. Olziersky, P. Dimitrakis, V. Ioannou-Sougleridis, P. Normad, T. Koukoula, Th. Kehagias, Ph. Komninou and A. Georgakilas
   ICNS-11, International Conference on Nitride Semiconductors, 30 August – 4 September, Pekino, China (2015)

10. ***Selective Growth of GaN Nanowires on SiO_2-masked Si(111) Substrates***
    J. E. Kruse, S. Eftychis, G. Doundoulakis, K. Tsagkaraki, M. Androulidaki, P. Dimitrakis, A. Olziersky, P. Normad and A. Georgakilas
    MBE 2014, 18th International Conference on Molecular Beam Epitaxy, 7-12 September, Flagstaff, Arizona (2014)

11. ***Temperature effects on GaN nanowire growth by PAMBE***
    J.E. Kruse, K. Tsagkaraki, M. Androulidaki, A. Adikimenakis, G. Doundoulakis and A. Georgakilas
    MBE 2014, 18th International Conference on Molecular Beam Epitaxy, 7-12 September, Flagstaff, Arizona (2014)

12. ***Selective Growth of GaN Nanopillars on patterned Si (111) substrates***
    J.E. Kruse, S. Eftychis, G. Doundoulakis, K. Tsagaraki, M. Androulidaki, A. Olziersky, P. Normand and A. Georgakilas
    IWN 2014, International Workshop on Nitride Semiconductors, 24-29 August, Wroclaw, Polland (2014)

13. ***A study on the fabrication of devices and the characterization of GaN nanowires and the GaN/Si heterojunction***
    G. Doundoulakis, A. Bairamis, E. Tsikritsaki, A. Stavrinidis, Ch. Zervos, G. Konstantinidis, M. Kayampaki, S. Eftychis, J. Kruse, A. Adikimenakis and A. Georgakilas
    38th WOCSDICE, Workshop on Compound Semiconductor Devices and Integrated Circuits, 15-18 June, Delphi, Greece (2014)

14. ***Nanopatterning of Si (111) substrates for selective growth of III-nitride nanowires by plasma-assisted molecular beam epitaxy***
    P. Dimitrakis, A. Olziersky, V. Ioannou-Sougleridis, P. Normand, J. E. Kruse, S. Eftychis, G. Doundoulakis, K. Tsagaraki, M. Androulidaki, G. Konstantinidis and A. Georgakilas
    38th WOCSDICE, Workshop on Compound Semiconductor Devices and Integrated Circuits, 15-18 June, Delphi, Greece (2014)
15. ***Importance of substrate temperature in one-step or two-step process of spontaneous GaN nanowire growth by plasma-assisted molecular beam epitaxy***
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    38th WOCSDICE, Workshop on Compound Semiconductor Devices and Integrated Circuits, 15-18 June, Delphi, Greece (2014)
16. ***Spontaneous growth of III-V semiconductor nanopillars by molecular beam epitaxy for nanoelectronic, photonic and sensor applications (invited)***
    A. Georgakilas, A. Adikimenakis, S. Eftychis, J. Kruse, K. Tsagaraki, M. Androulidaki, E. Iliopoulos, Z. Hatzopoulos, P. Tzanetakis, Ph. Komninou, T. Koukoula, Th. Kehagias, G. P. Dimitrakopulos, J. Kioseoglou, A. Lotsari, Th. Karakostas, G. Konstantinidis, G. Doundoulakis, K. Zekentes, P. Dimitrakis, V. Ioannou-Sougleridis, A. Olziersky and P. Normand
    4th IC4N-2013, Workshop on Nanowires and Nanostructures: Fabrication, Characterization, Applications, 16-20 June, Corfu, Greece (2013)