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Development of technology for improved nitride-based optoelectronic devices

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Αφιερώνεται στους γονείς μου,

Γιώργο και Ειρήνη,

στη Γιάννα

και γενικά σε όσους δεν το βάζουν εύκολα κάτω

Abstract

The main objective of this thesis is the development of the device fabrication technology for nitrides, towards establishing a technology platform, which can serve as a benchmark for the realization of Nitride-based optoelectronic devices and beyond. In this light, research was focused on basic fabrication procedures, which are not yet detrimental for nitrides and restrain realization of novel optoelectronic devices that are costly and reliable as well. Such procedures are dry-etching, ohmic contact formation to p-GaN and optimization of active region of laser structures.

The formation of optical cavity is one of the main issues in fabricating a semiconductor laser and it can be achieved, either by cleaving the semiconductor or by etching its surface in order to form mesas with vertical and smooth sidewalls. Our study resulted in obtaining mesas with mirror-like facets, having a slope of 90^{o} and a roughness of less than 100 nm, using a conventional Reactive Ion Etching (RIE) reactor with chlorine-based chemistry and photoresist AZ 5214 as the etch mask. These results were obtained after thorough optimization of lithography and RIE processes. For enhanced material protection during plasma etching, we have developed an alternative lithography procedure with a double photoresist layer, which ensures that photoresist etch-mask is sufficiently thick throughout the etching process.

Next, a study aiming in forming low resistance ohmic contacts to p-GaN followed. The influence of several pre-deposition surface treatments and different contact metals to the electrical properties of metal/p-GaN contacts was studied. A low resistance as-deposited ohmic contact was achieved, with the use of boiling aqua regia (AR) as the surface treatment, and Cr/Au as the contact scheme. The ohmic resistance of contacts with 50 μm interspacing was found to be 50 Ω. The results of X-ray Photoelectron Spectroscopy (XPS) characterization of p-GaN might be able to explain formation of this low resistance contact scheme. Towards this end, a formation mechanism is proposed, based on the appropriate preparation of p-GaN surface by boiling AR, and on covalent-type of bonding between Cr and semiconductor atoms, as evidenced by the short-range epitaxial character of Cr layer on p-GaN, ascertained by HRTEM and the Ga-Cr intermetallic phase formed at the interface without heat treating the contacts, ascertained by XPS.

Concerning active region of laser structures, a series of InAlGaN (QN) thin films and InAlGaN/GaN QWs of various In and Al compositions were grown and characterized. For the $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs, a reduction of internal-fields by a factor of 4 as compared to equivalent GaN/AlGaN QWs was estimated after fitting of our experimental results with theoretically calculated curves indicating that an internal-field of 0.265 MV/cm exists inside QN

QWs. Following the same procedure, the corresponding internal-field value for $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs was estimated to be essentially zero as expected from theoretical calculations, which predict zero internal-field in case of In/Al composition ratio close to ½. The reduced internal-fields inside the QN QWs are also indicated by temperature-, power-dependent and time-resolved PL characterization, with the latter yielding radiative recombination times of few hundreds of ps. Moreover, optical pumping experiments on laser structures composed of QN QWs in the active region show reduced power threshold values as compared to equivalent GaN/AlGaN structures.

Finally, by employing the optimized dry-etching and the novel, as deposited p-GaN contact scheme, violet EL was readily observed. The latter suggests that the as deposited Cr/Au contacts are good candidates for serving as the p-electrode in nitride-based optoelectronics. Furthermore, a novel nitride-based sensor, monolithically integrating an LED and a HEMT, is designed and realized. A study concerning process flow optimization resulted in achieving operation of both LED and HEMT parts of the devices in a satisfying level, with the first showing good performance and intense light emission, while the second needs further optimization. Considering the complexity of the structure and the multi-step nature of process flow, the fact that both parts of the devices satisfyingly operate and can be individually controlled, is very inspiring and opens the way for our novel, integrated sensor device to be tested in actual sensing experiments and, depending on the results, to be patented and commercialized.

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• 2010, ICO Micro & Nano, Athens, Greece, Effect of boiling aqua regia on MOVCD and MBE p-type GaN surfaces and Cr/p-GaN interfaces F. G. Kalaitzakis, G. Konstantinidis, L. Sygellou, S. Kennou, S. Ladas and N. T. Pelekanos
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CHAPTER 1

Nitride-based Optoelectronic Devices

1.1 Introduction

III-Nitrides constitute a family of wide, direct band gap semiconductors, with their special features originating from the hexagonal wurtzite structure they usually crystallize. Such features are the increased mechanical, chemical and thermal stability, the high electron saturation velocity, short carrier response times under external field application and others. The light emitted from the binary (GaN, AlN, InN), ternary (AlGaN, InGaN, InAlN) and quaternary (InAlGaN) compounds cover a wide range of wavelengths, spanning from near-UV to near-IR spectral region (250 nm - 1.5 μm) due to the wide range of band gap values (~ 0.8 eV for InN and ~ 6.2 eV for AlN) of these materials as can be seen in fig. 1.1, where the band gap values of binary, ternary and quaternary compounds are plotted versus their in-plane lattice constants. Moreover, by utilizing the modern Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) crystal growth methods there is the feasibility of growing alloys of various compositions in Al, In and Ga, controlling in this way their lattice constants and energy band gap values as shown in fig. 1.1. With the feasibility of accurate composition and layer thickness control provided by these crystal growth methods, multi-layered heterostructures can be engineered and

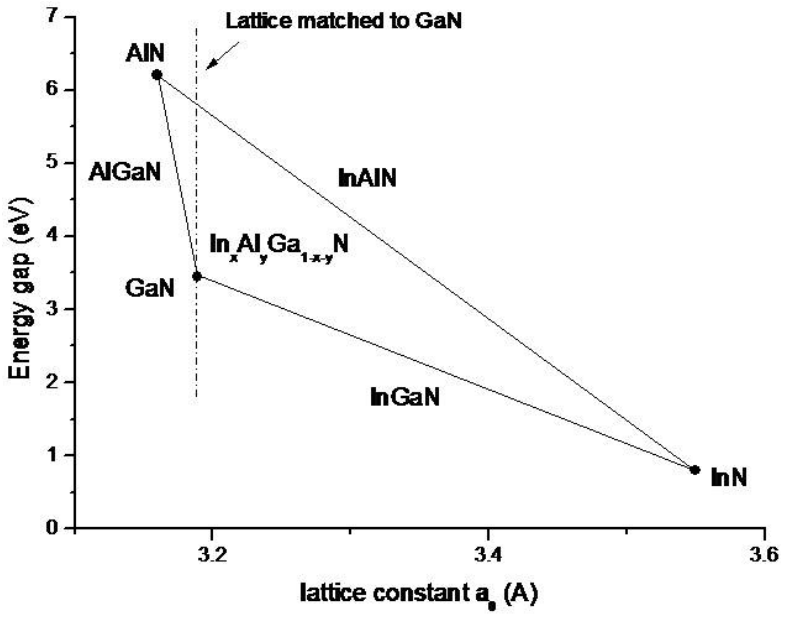

Fig. 1.1 *Energy band gap versus in-plane lattice constant of the III-N compounds.*

grown permitting realization of p-n and p-i-n structures, which are the basis of modern optoelectronic devices. As such are considered the devices through which electrical signals can be transformed into optical ones and vice versa. Light-Emitting Diodes (LEDs), Laser Diodes (LDs), photovoltaic devices (PVs), and others are the main types of optoelectronic devices, with nitride-based ones being the most important applicants for use in a variety of applications, like dense optical data storage, white and traffic lighting, photovoltaics, detectors and many others.

A schematic of typical nitride-based device geometry, commonly utilized in LEDs and LDs, is shown in fig. 1.1[1,2]. As can be seen in the schematic, the p-i-n structure that the device is based on, is grown on a sapphire substrate and is comprised of the bottom n- and the top p-GaN contact layers, with the i-region (active region) in between, where radiative carrier recombination takes place and is usually comprised of multiple-quantum well (MQW) structures, i.e. multi-layered -Barrier-QW-Barrier- structures. The electrical and optical properties of the heterostructure are mainly determined by layer composition, thickness and sequence and a careful design of the structure is needed for optimized device performance to be obtained. The n- and p-electrodes of the device are also shown in the schematic, while a mesa has to be formed in order for the active area of the device to be defined and the n-layer to be revealed and contacted. Such device geometry is imperative in nitrides, since sapphire, which is the costlier and most commonly used substrate for nitrides growth, is insulating and does not permit a full-area backside n-electrode,

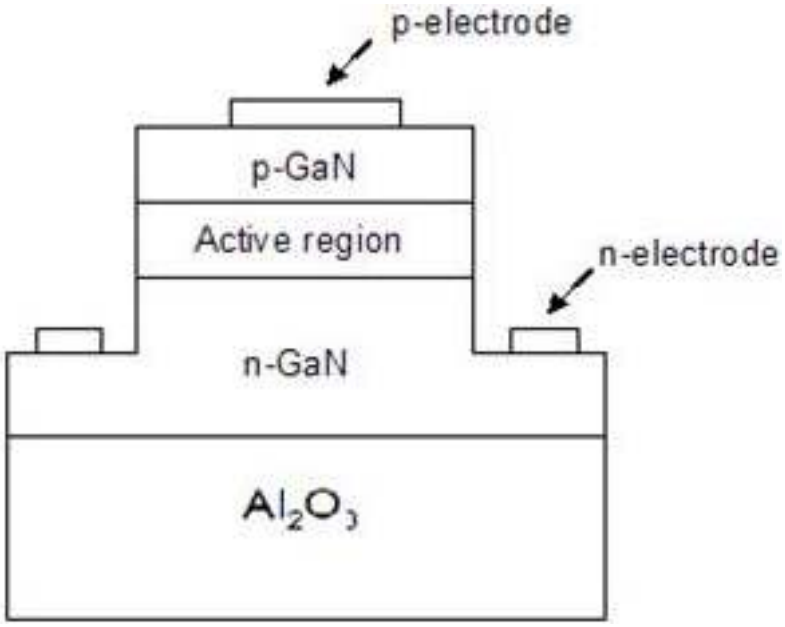

Fig. 1.2 *Schematic of a typical nitride-based p-i-n LED structure, which also applies in edge-emitting LDs.*

with such a geometry design favoring device performance through more uniform current injection in the active region and reduced serial resistance due to the increased contact areas of both electrodes. This is the case for arsenide-based optoelectronic devices, where p-i-n structures are grown on thick GaAs substrates, as opposed to nitride-based devices where such thick, free-standing GaN substrates are not available.

Heteroepitaxy of nitrides on sapphire substrates is the origin of many issues inhibiting performance of nitride-based optoelectronic, and not only, devices. As can be seen in fig. 1.3, there is a lattice mismatch between GaN and sapphire along (0001) plane, with strain-induced crystal defects being always present, despite the many year research and growth optimization of the thin AlN buffer layers. Moreover, GaN lattice is rotated by 30° in respect to the sapphire one, **making cleaving almost impossible**. This has an impact on LD realization, since cleaving can yield atomically-smooth surfaces, which in the case of edge-emitting LDs can be the mirrors of the Fabry-Perrot cavity, necessary for laser action to be achieved. Lasing is also dependent on the non-optical losses occurring inside the layers of the structure, with the high turn-on voltages obtained in nitride-based LDs being partly attributed to the **high crystal defect density** inside the layers of the structure.

However, moderate crystal quality of nitride-based structures grown on sapphire is not the only reason for the obtained device performance. The lack of symmetry along the [0001] direction (c-axis) that characterizes wurtzite structure, induces spontaneous polarization fields, which

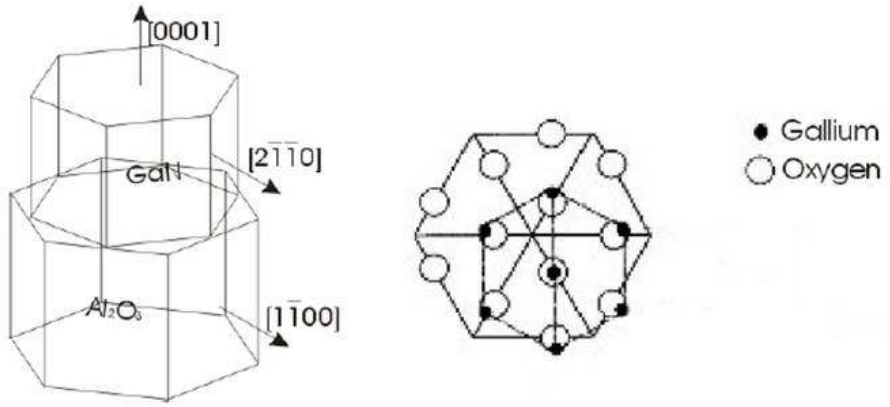

Fig. 1.3 *Schematic of sapphire and GaN unit cells; a lattice mismatch can be observed, as well as GaN lattice rotation along [0001] direction by 30°.*

along with the piezoelectric polarization induced by strain is responsible for the existence of **internal electric fields** inside the active region's layers. Such internal electric fields can have a devastating effect on optical recombination rates, in turn affecting LED and LD performance. Moreover, **p-type doping of GaN** is still an issue, since low solubility of dopand atoms in the GaN matrix is responsible for the even worse crystal quality of p-GaN as compared to unintentionally or n-doped GaN and the relatively low doping levels commonly obtained. Both features of p-GaN inhibit the realization of low resistance ohmic contacts to p-GaN, which is of major importance due to the voltage drop and heat originated from the large potential barriers present at the p-GaN/electrode interface.

The above mentioned issues are the main ones responsible for the somehow problematic performance of nitride-based optoelectronic devices still obtained. Most of them are growth-related, in the sense that better crystal quality resulting from growth on GaN and/or growth along other crystal directions (for example along a-axis) can finally improve device performance. However, if one wants to improve nitride-based optoelectronic devices based on the most common c-axis grown structures on sapphire substrates, optimization of the fabrication and design parts of the device realization procedure is needed. These are the main objectives of this work, where the results of our efforts to provide solutions for improved nitride-based optoelectronic devices are presented and discussed.

This work begins with a short introduction to semiconductor processing, which is necessary for device realization (**chapter 2**). A short presentation of the main characterization techniques employed in this work follows in **chapter 3**. The issue of optical cavity formation in nitrides by using Reactive Ion Etching is treated in **chapter 4**, where an improved procedure yield-

ing vertical sidewalls with roughness of < 100 nm has been developed, with special care given to material damage minimization during etching. The important issue of forming low resistance ohmic contacts to p-GaN is the topic of **chapter 5**, where a low resistance, as deposited contact scheme is presented, while exploitation of its formation mechanism is attempted. In **chapter 6**, internal-field minimization in the active region of optoelectronic devices is considered, where incorporation of quaternary nitrides in the design of the active region has proved to improve optical properties of the structures characterized. LEDs are fabricated in **chapter 7**, as well as a novel sensor device, which monolithically integrates a High-Electron Mobility Transistor (HEMT) with an LED for potential chemical or biological sensing applications. Finally, the main results and accomplishments of this work are summarized in chapter 8.

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CHAPTER 2

Device processing

2.1 A short introduction to semiconductor processing

After design and growth of a device structure, a number of processes are necessary for the realization of operating devices, i.e. devices that can be driven electrically by an external circuit. The processes beginning immediately after the growth of the structure and end up with the operating devices form what is called semiconductor processing or just processing, which can be very demanding and often determines the feasibility of a device's design. Furthermore, processing gives feedback to the design and growth procedures, in order for more realistic approaches to be adopted and/or growth to be optimized when is needed. The rest of this section is dedicated to giving a short introduction to semiconductor processing in general, while a more detailed presentation of the methods used for nitride processing in particular is given in the rest of this chapter.

The delivered semiconductor samples delivered for processing usually have the form of thin, circular-shaped plates called wafers. The wafer size can vary from 1 inch diameter, usually intended for basic/academic research, up to 12 inches for industrial applications, with the 2'' and 3'' diameter wafers being the most widely used. Depending on the device and its purpose of use,

the size of it can vary from hundreds of μm^2 to tens of cm^2. Consequently, the number of devices fabricated on top of every wafer can vary from 1 device/wafer (solar cells) up to approximately 10^{11} devices/wafer[1] (Intel's transistor density on a 12'' wafer). Moreover, there is usually the need of fabricating different kinds of devices, active or passive, on the same wafer. By active devices, are denoted the devices that perform a certain action (diodes, transistors), while by the term passive devices, are denoted the devices that are intended for, either the determination of material properties, like Van der Pauw geometry patterns for Hall effect characterization, or testing the quality of processes, like ohmic contact formation with Transmission Line Model (TLM) patterns, both to be discussed in chapter 3. No matter if the whole wafer or a part of it to be processed, the sample must usually be subjected to several successive and parallel processes in order for all devices to be fabricated in parallel on top of the sample undergoing the same processing steps.

Processing includes definition of the device in given shape and dimensions, spatial and electrical isolation of each device, Ohmic or Schottky contact formation on specific layers of the structure, doping, environmental protection, packaging and others. For most of the above mentioned processes, several techniques are utilized, with the most basic and important being lithography, etching (wet and dry), metal deposition and annealing. These four techniques are usually sufficient to yield devices for testing and characterization, especially in the case of academic/basic research. Apart from operation characteristics optimization, issues like cost, aging and environmental protection should be addressed as well when commercializing a device. The device characteristics can be optimized by improving both the structure of the device (design and growth related) and the processing quality. In this context, a significant part of the present work is focused in understanding, controlling and optimizing these four basic processes in nitrides in order to point out the way to solutions for improved performance nitride-based optoelectronic devices. Due to their importance, these processes will be discussed in detail below.

The processes, as well as their sequence, needed for the realization of a device is called process flow. Usually for the completion of a device, different process flows are possible; finding the optimum one can be very crucial for the device operation and operation characteristics.

2.2 Nitride processing for optoelectronic devices

Process flow is mainly defined by the semiconductor material that the structure consists of. Nitrides have unique properties, which have to be taken into consideration during their processing. Moreover, each process may be affecting the others, and in this light, their sequence might be important. From the short discussion in the previous chapter concerning the nitride-related issues affecting optoelectronic devices performance, it becomes clear that almost all of them are material related, i.e. a higher quality material would finally give better devices. For a given material quality though, finding solutions through processing can be very challenging and the only way to improve device performance.

Despite the fact that nitrides belong to III-V compound semiconductor family, their peculiarities make their processing substantially different from III-Arsenides, which have a well developed device technology and the commercially grown material is of high quality. Among these special features of nitrides are their increased chemical inertness, the resultant unavailability of wet chemical etchants and large defect density. Moreover, it should not be forgotten the fact that nitrides are heteroepitaxially grown on foreign substrates, with most common being Al_2O_3 (sapphire), SiC and Si.

In the case of etching, there has not yet been found any aqueous solution to etch nitrides of both polarities (Ga- and N- polarity), with an exception probably being the case of AlN, the low and reaction-limited etch rates of which being attributed to its lower crystal quality[2]. Therefore, if one does not wish to employ complicated and time consuming techniques, like photo-enhanced (assisted) chemical etching, the only way to form mesas on nitrides is through dry etching, i.e. use of ion beam (sputtering) or plasma techniques. Moreover, the enhanced mechanical and chemical stability of nitrides makes dry etching a procedure that needs careful optimization due to low etch rate, long etching runs and insufficient material protection from the usual photoresist etch masks. With quality of mesas often playing an important role in device performance due to surface states caused by etching, optimization of this procedure is of great importance.

N vacancies on the other hand, are present in epitaxial nitride films and are considered responsible for the unintentional background n-type doping usually observed. This has a negative effect on producing high resistivity epitaxial layers and furthermore hinders the already problematic p-type doping of nitrides. Therefore, the lack of N atoms in the crystal and the ease that surface N atoms are extracted from the surface during etching or annealing have to be taken into

consideration during such processes. These two processes by the way, are well known to improve ohmic contact formation to semiconductors; etching can increase surface roughness providing larger area for metal contacting, while annealing can promote reactions between atoms of the crystal and metal atoms, leading to conductive phases at the metal/ semiconductor interface. These processes however, cannot be applied in the case of p-GaN in this straightforward way, as will become apparent in chapter 5. Moreover, ohmic contact formation to p-GaN is also affected by presence of H atoms in the crystal, caused by Mg doping in the most widely used MOCVD grown samples. H atoms (in the form of Mg-H and other complexes) act as hole compensating centers, with their removal from the interface or near-interface region being crucial in the contact quality. This issue will be scrutinized in chapter 5. In the rest of this chapter, the basic techniques used in this work for nitride processing will be presented.

2.3 Processing Techniques for nitrides

Almost all processing techniques require advanced and specialized machinery for their implementation. Moreover, if one considers the dimensions of most devices, contact of dust particles or other contamination with the sample surface must be avoided, including human secretion, like sweat and hand grease. Consequently, people who do processing wear special clothes, shoes and gloves, while sample handling is performed with special tools, the tweezers. Furthermore, light, temperature and humidity conditions should be well controlled for reasons that will be apparent below. Semiconductor processing therefore takes place in special laboratories, the clean rooms.

As the name denotes, the amounts of dirt and dust inside clean rooms are well controlled. Dirt and dust are actually particles that travel through air. The air concentration in particles greater than a specified size (0.5 μm) is used to classify clean rooms. The air inside the clean room of MRG, used for all experiments in this work, has a maximum concentration of 1,000 particles greater than 0.5 μm in a cubic feet of air, and that makes it a class 1,000 clean room. Those that are used for LSI or VLSI circuit fabrication for instance, are usually of class 100 or less, while in class 10 clean rooms human presence is prohibited in order for such low number of particles to be preserved. On the other hand, a typical room is of class 100,000 or more. The need for having

controlled environmental conditions inside clean rooms is expanded to temperature, humidity and lighting conditions also. Typical values are: 20-21°C of temperature, 45% of air humidity, while lighting is yellow. The reason for the above specifications will be discussed in the photolithography subsection below.

Etching, lithography, metal deposition, annealing and other processes are usually performed inside clean rooms in order for 'dirty' air exposure of the sample in-between of successive processes to be avoided. The rest of this section is devoted to presenting the basic processes for device processing and it begins with a very important process, which is surface cleaning.

2.3.1 Surface Cleaning

A sample after growth must usually undergo structural, optical or electrical characterization (XRD, AFM, SEM, PL, Hall effect), in order to ascertain its properties and quality. During characterization, contact of the sample with human skin, dust, glue, metal contacts is possible. Surface cleaning aims at removing any such contamination from the sample surface, in order for processing to begin. This is a very important procedure, which can affect the whole processing and device performance. There are two types of contamination, organic and inorganic.

Organic contamination is usually caused by human contact with the sample. It may be grease, sweat from hands, saliva or particles that are sprayed out during expiration. They can be removed with sequential use of acetone, isopropanol and de-ionized (Di) water. The mechanism is the following: grease is removed by the more active acetone, the remainings of which are removed by isopropanol. Di-water can then remove the remainings of isopropanol and leave a hydrated surface[3]. Actually isopropanol is used for this reason, i.e. its ability to remove acetone and to be removed by water. Usually, an ultrasonic bath is used in order for this procedure to be more efficient, while there is also the ability of heating the chemicals. Heating is used, either in addition with ultrasonics for very intense contamination, or alone when ultrasonics cannot be used, like in the case of GaAs where ultrasonics can damage a 3" wafer. Nitrides on the other hand, due to both increased mechanical stability and the fact that they are grown on sapphire substrates, do not suffer from similar problems. This whole procedure is called organic degreasing and is also effective in removing other organic compounds, such as photoresist. It is also used for silver epoxy removal, commonly used in PL measurements for sample mounting. The organic degreas-

ing results are controlled via optical methods, and if not satisfying, the whole procedure is repeated from the beginning.

By inorganic contamination is usually meant native oxide formed on the crystal surface, when sample is exposed to air after growth. The presence of oxides can be more intense if the sample is subjected to any thermal annealing after growth, like in the case of MOCVD grown p-type GaN. Inorganic contamination is usually removed by inorganic acid solutions, like HCl, HF, HNO_3, H_3PO_4, H_2SO_4 or combination of these, while there is again the ability of heating the solutions on a hot plate. In the Si and GaAs cases, some of the above acids can be etchants, therefore the choice of acid(s) used and the procedure must be performed very carefully. This is not the case for nitrides as mentioned previously, where etching by any aqueous solution has not yet been widely observed (apart from monolayer removal occurring with N-face crystals in melted KOH). In nitrides though, other issues must be considered as well, such as efficient native oxide removal with minimum N removal during such processes, which in the case of p-type GaN can be detrimental as will be discussed in chapter 5. Inorganic chemicals can usually etch and remove metals from the sample surface, like Ga droplets usually found on nitrides or, less often, sintered In contacts made for Hall effect measurements.

If one wants to be certain of the cleaning process results then the painstaking method of RCA cleaning should be employed. It is a multi-step procedure employing both organic and inorganic chemistry in sequence, with the mechanism being similar to the organic degreasing one: the next chemical removes remaining of the previous one and so on, with the remainings of the last chemical being removed by Di-H_2O. It is well known that contact of the basic acetone and propanol with acids should be avoided, therefore dedicated hoods for each kind of chemicals is used. Due to its complexity, RCA cleaning is used only in heavily contaminated samples. The necessity of having well controlled chemical composition on the sample surface prior to photolithography will become obvious below.

2.3.2 Optical Lithography

The optical lithography technique is based on the area selective illumination of a chemical substance and subsequent removal of either the exposed or the non exposed areas for patterns to be formed on the light sensitive substance. These patterns can then be transferred on the substrate

with use of etching and/or deposition processes. In contrast to using light, a beam of electrons (e-beam) can also be used, leading to another type of lithography, the e-beam lithography. The latter is used for nanometer scale pattern formation.

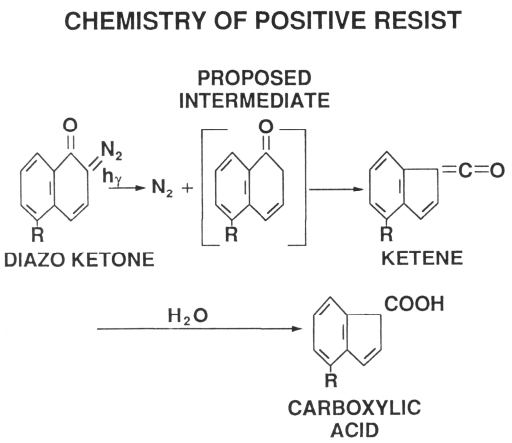

Fig 2.1 *Chemistry of a typical positive photoresist. The product of light-induced chemical reaction is shown as well.*

The light sensitive substance used in optical lithography is a polymeric material called photoresist (PR) or just resist. Depending on the light wavelength, type of lithography and purpose, different resists can be used. There are two main PR categories: the positive and the negative ones. In positive PRs, the areas that are removed are the exposed ones, while in the negative PRs the areas that are removed are the non-exposed. Figure 2.1 shows the chemical reactions occurring during illumination in the case of a positive PR. Such PRs contain photo-active elements, which absorb light. The absorbed energy is responsible for breaking the bond with nitrogen, leading to ketene formation. Ketene reacts with moisture, either found inside the PR or in the atmosphere (this also explains the necessity of well controlled environmental conditions in clean rooms), to form carboxylic acid, which is easily removed by a basic alkaline solution. The abovementioned reactions do not occur in the non-exposed areas of the positive PR and altogether constitute the basic patterning mechanism. Negative PRs on the other hand, become insoluble in basic alkaline solutions when they absorb light. In any case, the ‘‘contrast’’ in the chemical composition of the exposed and non-exposed areas of the PR is responsible for its selective removal and patterning.

The photolithography procedure for most resists includes the following basic steps: **spin-coating**, **soft-bake**, **exposure**, **development** and **post-bake**. In order to understand the mechanism of optical lithography, each step will be discussed shortly.

First, the PR should cover the sample’s surface uniformly, in the form of a thin layer. This is achieved with the method of **spin-coating**, with rounds/ minute and spinning duration being the parameters that control thickness and uniformity. For PR AZ 5214, spinning at 4,000 rpm for 25 sec yields a layer thickness of ~ 1.2 μm, while 3,000 rpm for 30 sec yield ~ 1.8 μm. There is a low limit in spinning velocity and duration, for which uniformity of the resist layer is lost, with these limit values depending on the resist used. Thickness uniformity of the resist layer is a prerequisite in every lithographic procedure. One can experiment with spinning velocity in order for

better uniformity to be achieved, with this effort being almost mandatory for small sized samples (less than 1x1 cm^2), where edge effects are more pronounced. By edge effects is meant the edge bead built-up during spinning due to greater attraction forces between the surface and the PR at the sample edges (see fig. 2.2).

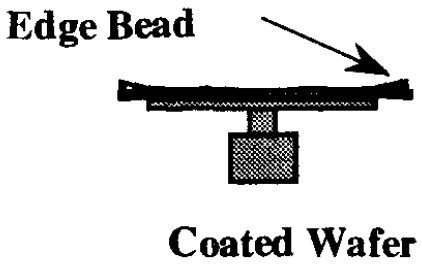

Fig. 2.2 *Schematic illustration of edge bead effect; photoresist layer is thicker at the edges of the sample.*

Next, **soft-bake** of the PR takes place. This step is necessary for moisture and solvent removal in order for the PR film to acquire the desired mechanical stability for proper handling and lithography completion. As the term implies, this step does not completely remove moisture from the resist film, so that the aforementioned necessary reactions to take place during exposure. In this point, the necessity of having well controlled temperature and humidity conditions inside clean rooms becomes evident. Usual bake conditions in our lab for AZ 5214 are: ~ 85°C for 20 min in an oven, or alternatively, ~ 95°C for 90 sec on a hot plate, although bake in an oven offers better uniformity and is preferred for demanding lithographies.

Selective modification of the PR chemical composition is achieved during the **exposure** step. The PR mainly used in this work is the AZ 5214 of Clariant. This resist is positive, meaning that it follows the mechanism described in fig. 2.1. In fig. 2.3 one can see the transmission spectrum for exposed and non-exposed AZ 5214. One can notice, that this PR absorbs significantly up to wavelength values of ~450 nm. Therefore, if the exposure wavelength is below this value the absorption in the exposed areas will be significant and the photo-induced reactions described above will take place. The usual exposure wavelength for this resist is i-line of Hg emission spectrum (356 nm), while the necessity of having yellow lighting inside clean rooms now becomes clear; white lighting would result in significant absorption of the shorter wavelengths of the visible spectrum in the whole PR volume, making pattern-

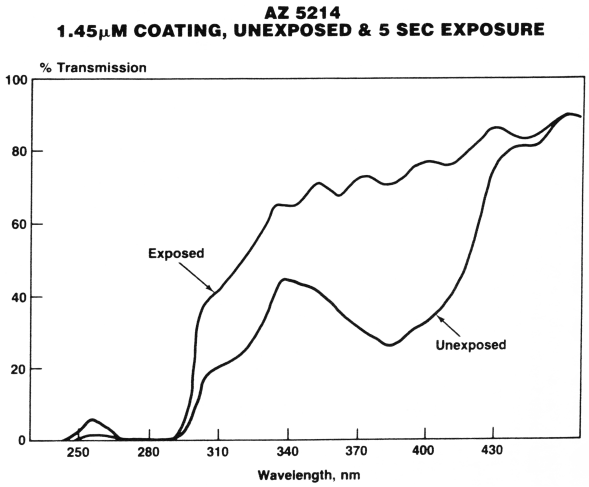

Fig. 2.3 *Transmission spectra of exposed and non-exposed PR AZ-521. Strong absorption above 290 nm is observed in both cases.*

ing impossible.

The selective irradiation of the resist film is achieved with the use of photomasks, i.e. transparent plates with opaque areas, altogether forming the pattern. These masks are usually made out of boron silicate or quartz (SiO_2) with opaque metal oxide (usually CrO_x) patterns formed on it. Basically, what one has to do is to bring the sample, with the PR layer on top of it, in contact with the mask and irradiate for some time in order for light to go through the transparent areas of the mask, while blocked from the opaque patterns. This optical lithography mode is called contact lithography, in contrast to projection lithography, where the sample has a distance from the mask and the pattern is projected, through special optical systems, on the resist film. With an important feature of optical lithography being edge definition, i.e. the accuracy that the borderline between transparent-opaque areas is transferred to the resist film, the intimate contact between the resist film and the mask becomes of great importance due to necessity of suppressing the undesired, although present, effect of light diffraction at the SiO_2-CrO_x edges. Moreover, light should form a beam of uniform radial intensity, impinging normally to the sample surface. Furthermore, placement of the sample relatively to the mask is very important, especially if one wants to form patterns relatively to already existing patterns on the sample surface. The exposure procedure, therefore, is achieved with use of a dedicated system, called mask-aligner like the one shown in fig. 2.4. This mask-aligner is the MA 6 of Karl Suss and is the one mainly used in this work. In such a mask-aligner, one can find state-of-the-art optical systems for the uniform irradiation of the resist film with a normal to the surface impinging beam, while there are systems for submicron X, Y and Θ translation of the sample for accurate control of its position, necessary for alignment of forthcoming patterns, as well as optical microscope and camera for monitoring the sample. Intimate contact between the sample and the mask is achieved by vacuum pumping the air between them, with thickness uniformity and edge bead of the resist film being crucial at this point. By optimizing exposure time, for a given exposure wavelength and beam intensity, one can give sufficient dose of photons for the photo-assisted chemical reactions to occur throughout the whole PR film thickness, while mi-

Fig. 2.4 *The MA-6 mask-aligner of Karl Suss.*

nimizing the impact of diffraction effect. The latter along with the fact that the minimum spot size of a light beam cannot be less than its wavelength λ, set the limits of optical lithography.

After the exposure, next comes the resist **development** step. A basic solution (developer) is employed during this step, which selectively etches either the exposed (positive PR) or the non exposed (negative PR) areas of the PR. The developer used for AZ 5214 is a KOH based solution (AZ 400K), diluted with Di-H_2O at a volume ratio of 1:4 (usually 5ml AZ 400K: 20 ml Di-H_2O for small samples). Dilution offers lower etch rate, therefore, better control of the development step, with development time, i.e. the time that the sample is dipped into the developer, being an important parameter. Development time generally depends on the PR layer thickness, exposure time and application, with its minimum value determined by the minimum time needed for pattern to appear and complete removal of the exposed or non-exposed areas of resist from the surface of the sample to occur. After this point, further development will result in improved sidewall roughness if the additional development time is up to 25% more than the minimum one. This can be explained by removal of additional exposed (positive) resist from the sidewall, which absorbed a smaller light dose due to diffraction effects and needed longer exposure to the developer. Even further development will lead to increased sidewall roughness of the resist patterns, due to removal of non exposed areas in this case, which had some light dose by diffracted rays, while even more time in the developer will lead to lost of pattern dimensions and failure of the lithography (overdevelopment). Control of this step is performed with optical microscope. Clearly, development time is affected by the previous lithography steps and a number of experiments are needed for calibrating the whole procedure for a specific application.

Up to this point, patterns are formed and this can be the end of the lithography if increased mechanical stability of the resist patterns is not a requirement for the specific application. But if hardening of the PR film is required, an additional heating step is needed and this takes place during the last step of the lithography, the **post-bake** of the PR. Heating, during this step, has to take place at higher temperature than the soft-bake step and aims at complete moisture and/or solvent removal, with increased mechanical stability achieved mainly through reflow of the resist and cross-linking of the polymeric chains inside PR's volume. Typical post bake conditions for AZ 5214 is 110°C in an oven for 30 min or 90 sec on a hot plate. Actually, the duration of post bake depends upon the application, as will become apparent in chapter 4.

These were the basic steps of optical lithography and are, more or less, the same for the majority of the PRs used. From the above discussion, it is evident that many parameters control the final properties of the obtained PR patterns and a lot of work is needed for adjustment of li-

thography to the specific application. After PR pattern formation, sample is ready for either etching or deposition of metal or dielectric to be performed for pattern transport from the resist to the sample surface. For completion of a device, many processing steps are usually required; for a light emitting diode for instance the minimum required steps are: one etching, two metal depositions and at least one thermal annealing step. For each etching and metal or dielectric deposition step, a different lithography step is needed, each having a different pattern, with all of them needed to be aligned in order for a device to be fabricated. Alignment of each pattern with patterns formed during previous steps is performed with use of the mask-aligner, as described above. Without the photolithography technique, patterning of samples would not be possible, at least in the well controlled way it is now.

2.3.3 Dry Etching using Reactive Ion etching

Etching is a process involving removing of material from the sample surface. Material can be uniformly removed from the whole surface of the sample or it can be selectively removed if the surface is patterned. Patterns can be made using PR, metal or dielectric, acting as the etch mask, i.e. the covered areas of the sample surface will be protected and won't be etched, while the uncovered areas will be removed. The resulting features on the sample surface are called mesas due to the resemblance in shape with the trapezoidally-shaped, flat top mountains. As mentioned, nitrides cannot be wet etched, especially the most common Ga-polarity films. But even if they were, wet etching is not very appropriate if pattern's dimensions are critical. In nitrides therefore, dry etching techniques are utilized.

Dry etching usually employs ion/ atom beams or plasma to remove material from the surface. If ions or atoms do not chemically interact with the semiconductor, etching is performed solely by mechanical removal of surface atoms by impinging kinetic ions, a process also called sputtering. On the other hand, plasma etching employs randomly moving ions to etch the semiconductor, based mainly on the chemical interaction of the kinetic ions and the semiconductor surface atoms. If the active, kinetic plasma species all move towards one direction, usually normal to the semiconductor surface, the technique is called Reactive Ion Etching[4] (RIE) and is the one mainly used in this work. A short presentation of the RIE technique, the system used in this

work and the parameters controlling the procedure, will be helpful to better understand dry etching of nitrides.

Plasma is an excited matter state, obtained when sufficient energy is provided to a gas or gas mixture in order for some gas atoms or molecules to ionize[5]. This distinct matter state is characterized by the coexistence of ions (electrons and positive radicals), atoms and molecules. Practically, in order for plasma to be obtained, one needs a vacuum chamber, the gases and a voltage source for the excitation. In order for voltage (direct or alternating) to be applied, gases should be confined in-between two electrodes, usually being the top and bottom walls of a vacuum chamber. Some of the plasma electrons, since they are more kinetic than the positive ions, move towards the electrode and build-up a negative potential, making the plasma to be quasi neutral in its volume. As electrodes become more and more negatively charged other plasma electrons are repulsed from the electrodes, forming a narrow area depleted of electrons next to the electrodes, called the plasma sheath. Across the sheath is obtained a voltage drop accelerating the positive ions towards the electrode. Sheath's small thickness (0.1-1 cm), as compared to the chamber's dimensions, makes the electric field there to be homogeneous and vertical to the electrodes. As a result, plasma's positive ions are attracted towards the electrodes. A steady state is finally achieved, where equal number of electrons and positive ions impinge on the electrodes per unit area and time. If a sample is placed on the bottom electrode, positive ions will impinge on the sample surface removing material from the uncovered areas of the surface through mechanisms to be discussed below. In this way, dry etching occurs and mesas are formed on the sample surface.

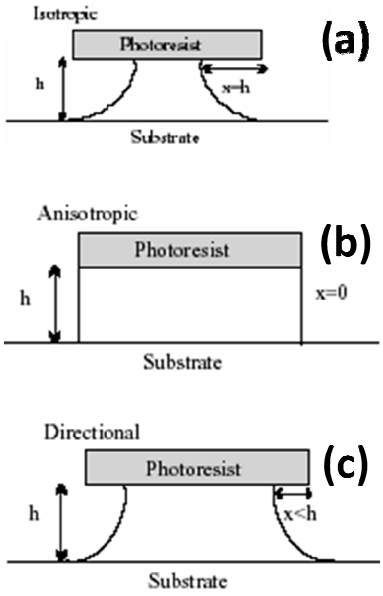

Fig. 2.5 *The three dry- etching mechanisms employed in RIE: (a) chemical, (b) physical and (c) kinetically-assisted chemical*

The sheath accelerated ions that hit sample's surface (and electrode) remove material through two distinct mechanisms (physical and chemical), leading to three etching modes: **chemical**, **physical** and **kinetically assisted chemical** modes. A very useful figure used to categorize its modes is the etching anisotropy coefficient, defined as the ratio of etch rate in a direction parallel to the surface over the etch rate vertical to the surface. In **chemical mode** the two etch rates are equal, lending to etching a fully isotropic character, resembling the fully isotropic character of wet etching. This etching mode results in large undercuts, as seen in fig. 2.5 (a) and

can be used when pattern's dimensions are not critical. This etching mode however, results in smoother mesas sidewalls. In **physical mode** of etching on the other hand, plasma ions do not chemically interact with the semiconductor. Any material removal in this case, occurs through surface bombardment by the kinetic ions, which move perpedicular to the surface due to the plasma sheath. Therefore, etch rate parallel to the surface is zero, giving to etching a fully anisotropic character, as seen in fig. 2.5 (b). This mode is also called sputtering. This etch mode can lead to deep mesas with vertical sidewalls and is ideal if pattern's dimensions are critical. In contrast to chemical mode, this mode usually leads to increased roughness of mesas sidewalls. The **kinetically assisted chemical** etching mode, as name denotes, is a mixture of the above two modes and is the one employed in RIE. Here, ions are both kinetic and chemically reactive with the semiconductor, removing material in a combined way. Kinetic ions, impinging on the surface, either brake atoms' bonds directly or chemically react with them to form by-products that are, either removed by the pumping system directly or by bombardment of forthcoming kinetic ions of the plasma. This mode is not fully anisotropic and can be characterized as directional, as can be seen in fig. 2.5 (c). Depending on the pattern requirements and application, one can either enhance chemical or physical component of the combined etching mode employed in RIE, affecting the anisotropy coefficient. This is practically achieved by controlling some parameters to be discussed below.

The RIE system used in all dry etching experiments in this work is a conventional RIE system of Vacutec AB, employing a 13.56 MHz RF-source for plasma ionization, a schematic of which being shown in fig. 2.6. The base of the cylindrical shaped, aluminum chamber is the one electrode, where samples are placed, and the rest of the chamber is the other electrode, which is grounded. With all bias applied, therefore, to the bottom electrode, sheath is only formed over this electrode. Consequently, the direct electric field that accelerates positive ions towards the electrode and the sample is highly directional and, to a good approximation, homogeneous. A mechanical-turbo pump combination is employed for pumping the chamber, with vacuum being ~

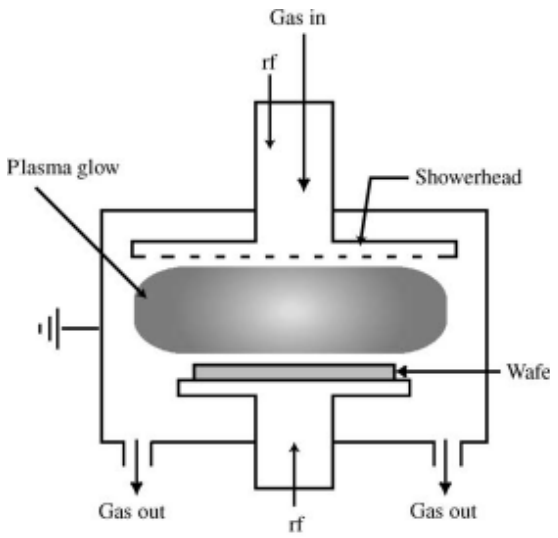

Fig. 2.6 *Schematic of the RIE system used.*

$5x10^{-6}$ mbar after overnight pumping. Gases are introduced into the chamber from the top side, with each gas flow being accurately controlled by mass flow controllers. The chamber pressure during the etch run can be controlled via a throttle valve of 0.1° angular step, connected to the pumping system. In order to avoid heating of the sample from plasma electrons, temperature of the bottom electrode is controlled by a closed-circuit cooling system. Progress of etching is in situ monitored with use of a laser interferometry system. Gases to be excited into plasma, their flows (partial and total), chamber pressure during run, RF-source power and dc-bias are the parameters that control the process.

Gas chemistry has to be chosen in light of both high reactivity with the semiconductor and the volatility of etch by-products. Adding an inert gas, like Ar, or an active one, like Cl_2, can enhance physical or chemical component of etching respectively, while ratio of the gases used can be controlled by their flows through the mass flow controllers. **Chamber pressure** value during run can also affect isotropic or anisotropic character of etching through the mean free paths for electrons and ions, leading to enhancement of the chemical component of etching if the chamber pressure is increased. These values typically range from 8 mTorr to 100 mTorr. Next, **RF-source power** is the power offered to gases in order for plasma to be achieved. A higher power value will ionize more molecules, at the same time resulting in more energetic electrons, which will transfer their energy to molecules or ions during collisions. As a consequence, ions that are directed towards the sample are more energetic increasing the etch rate. Last but not least, the **dc-bias** reflects the kinetic energy of ions impinging on the electrode and on the sample surface and, for a given semiconductor, is the result of all the other parameters, such as the gases used, source power and chamber pressure, and in the RIE case is usually of the order of hundreds of Volts. For constant power and pressure, dc-bias increases throughout the etch run reaching a maximum value after some time, with this fact being most probably related to the number of ions impinging on the electrode surface per unit time and the fact that this number saturates over time. Practically, dc-bias is controlled indirectly through control of rf-source power and chamber pressure, which as seen above, affect the kinetic energy of ions. Higher dc-bias values results in higher etch rates and enhancement of anisotropic etching, which may lead to increased roughness in the mesas' sidewalls. Therefore, in many cases a compromise between the etch rate and the mesa roughness has to be made.

In conclusion, RIE is a fundamental technique in semiconductor processing in order to obtain good quality mesas and its multiple parameters need careful optimization in any device undertaking. The RIE results concerning nitride dry-etching is the topic of chapter 4.

2.3.4 Metal deposition

Metal deposition is the process involved when ohmic or Schottky contact formation is required. The objective in this process is to deposit a thin metal film on the semiconductor surface, either covering the whole sample, or some specific areas following a pattern. It belongs to the more general process of thin film deposition, where deposition of dielectrics is also included. While there are many physical and chemical deposition techniques for metals, the one mainly employed in this work is **electron-beam thermal evaporation**. A detailed presentation of the experimental procedure for metal deposition and patterning follows.

Thermal evaporation, as the name denotes, is a process where energy is provided to heat and evaporate the material to be deposited (source material), in order for vapors' condensation to occur on the sample surface. If an electron beam is used for heating the source, the technique is called e-beam evaporation, as opposed to resistive evaporation for example, where heating is achieved through the Joule effect. Vacuum ensures a long mean free path for vapors to reach the sample surface instead of colliding with air particles and, depending on the source material, the vapors can have atomic, molecular or ionic nature. If a metal source is heated above its melting point, metal atoms will leave the source volume, ascribing an atomic nature to metal vapors. In other words, metal deposition occurs through energetic metal atoms impinging on the sample surface. Moreover, metal atoms' movement is considered ballistic accentuating issues with step or sidewall coverage. Considering the large in-plane lattice constant differences of semiconductors and metals used, along with the fact that sample is not usually heated during metal deposition, the polycrystalline nature of the deposited film, routinely observed with XRD and TEM, can be explained. The metal film is considered to be bonded to the semiconductor through electrostatic interactions of Van der Waals nature, forming in the general case an abrupt interface. A more de-

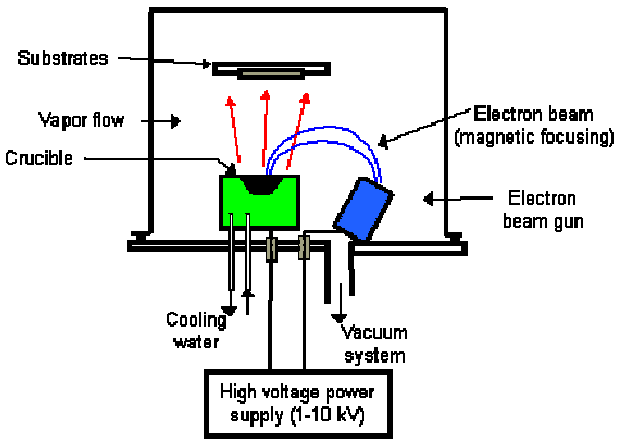

Fig. 2.6 *Schematic of a typical e-beam deposition system.*

tailed discussion on the nature of bonding between metal and a semiconductor will be conducted in chapter 5. A schematic of the technique is shown in fig. 2.6.

While applications that need full surface coverage are very few, the majority of applications require metal deposition on specific areas of the sample surface. The basic technique for this to be achieved is the **lift-off** technique. In this technique, the sample is first patterned with PR, with the corresponding photo-mask creating openings in the areas that the metal should finally remain (fig. 2.7 (a)). Metal deposition will cover the whole sample surface, i.e. both the bare sample surface and the top of the PR patterns, as seen in fig. 2.7 (b). Subsequent sample immersion in acetone will remove the PR patterns along with the metal that has been deposited on top of PR, leaving behind the metal deposited directly on the sample surface (fig. 2.7 (c)). The ballistic movement of metal atoms ensures that the PR patterns' sidewalls are not covered by metal and along with the fact that the deposited metal thicknesses are usually much less than 1 μm, and thus the PR patterns are not submerged in the metal (fig. 2.7 (b)), there are always exposed PR surfaces for acetone to come in contact with PR and remove it. In very dense patterns however, with small openings for metal deposition, the PR contact with acetone becomes problematic. In such cases, special openings should be incorporated in the photo-mask design for this purpose. Another issue that might emerge is the non verticality of the sidewalls of PR patterns, which can lead to full metal coverage of sidewalls leaving no exposed PR surfaces for lift-off. Slope of PR patterns' sidewalls can be controlled during photolithography, offering the ability to overcome such issues, as will be better explained in chapter 4.

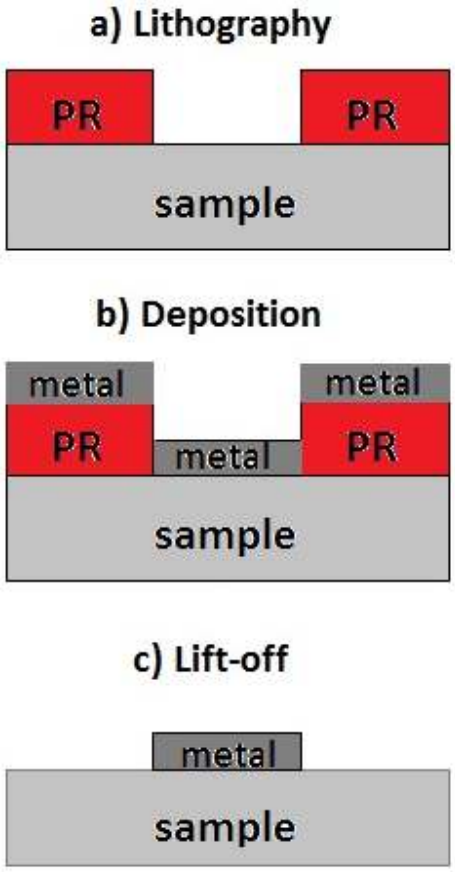

Fig. 2.7 *Schematic of lift-off technique.*

Apart from the positive slope of the PR patterns' sidewalls, there are some other PR-related issues that might emerge during metal deposition procedure. For instance, if the difference in thermal expansion coefficients of semiconductor and metal are large, sample heating during evaporation can be a way to promote metal adhesion and avoid cracks on the metal film, which

are observed if no heating is used. For already patterned samples the sample temperature should not exceed 110°C, as is the post-bake temperature, or else failure of lift-off is very possible due to inability of acetone to remove the hardened PR. If unintentional heating of the sample due to the hot metal vapors, which is always present and can raise sample's temperature by > 50°C depending on the metal, is taken into consideration, a lift-off failure is very possible. Moreover, there are cases where surface treatment prior to metal deposition is needed, like in the case of p-GaN, in order for oxide and/or other contamination to be removed. This is usually performed by sample immersion in an acid or base solution and in order for the surface not to be re-contaminated, this step should be performed after lithography and before sample's loading inside the vacuum chamber of the e-beam evaporator. The fact that the sample is PR patterned when immersed inside a solution limits the choice of chemicals that can be employed for surface treatment due to possible PR etching by some of them, while restrains immersion times and solution temperature . An alternative approach for metal patterning able to overcome the above mentioned issues is metal **etch-back**. In this approach, the metal film is first deposited on the entire, bare sample surface and then patterning of the metal film with PR follows, as shown in fig. 2.8 (a) and (b). The aim of this procedure is finding a chemical that etches the deposited metal without attacking PR, which acts as the etch-mask, or else, PR will be removed completely and metal patterning won't be possible. The lithography in this case should create PR patterns wherever metal should finally remain, i.e. the opposite than is in the lift-off technique. This is achieved by, either designing a photo-mask directly for that purpose or by employing a negative PR if the same photo-mask as in the lift-off technique is used. With PR AZ 5214 however, there is the ability of easily transforming it into negative, following a modified lithography procedure called **image reversal**. Nevertheless, when metal from the uncovered with PR areas is etched away, PR can be removed by acetone and the metal patterns can be finally obtained, as seen in fig. 2.8 (d). Special attention should be paid during optimization however, as well as execution of this procedure, concerning the duration and temperature, in order for patterns dimensions not to be lost due to the isotropic nature of wet etching. Conclusively, metal etch-back offers more freedom degrees concerning sample's surface treatment prior to metal deposition and sample temperature during deposition, however not generally applicable since the prerequisite of finding a metal etchant without affecting the PR pattern cannot be easily satisfied. Furthermore, the quality of the obtained metal patterns using etch-back is always inferior as compared to this of the lift-off. Therefore, in cases where surface treatment and/or sample heating during deposition do not affect the PR of patterned samples, the lift-off technique is preferred.

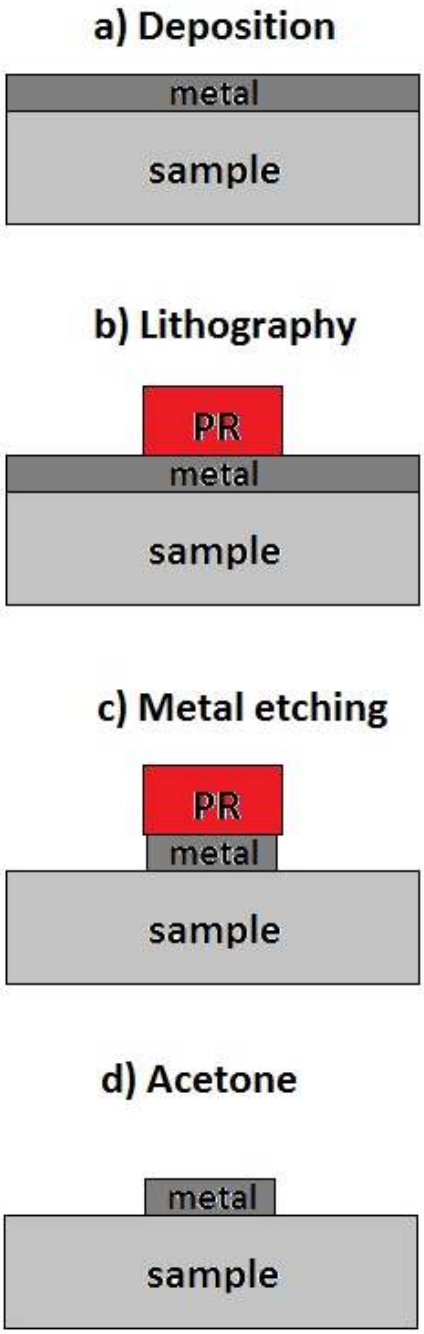

Fig. 2.8 *Steps of the metal etch-back approach.*

The e-beam evaporation system used in this work is a Temescal BJD 1700 of Airco Coating Technology. For achieving low pressures inside the chamber a cryogenic pump is utilized, reaching vacuum values of 10^{-7} Torr after overnight pumping. The electron beam is accelerated in a potential of maximum value of 20 kVolts and can be controlled either automatically or manually. Source materials are placed inside special containers, called crucibles, which exhibit higher melting points than that of the material to be evaporated, while there is the ability of having 6 different crucibles, each one containing different source materials, for multi-layered structures to be obtained. The exposure of the sample's surface to vapors can be controlled via a shutter, which is placed in between the source and the sample. Thickness of the deposited metal film can be in-situ monitored and controlled with utilization of a piezoelectric crystal, which is placed close to the sample.

2.3.5 Thermal annealing

Thermal annealing is a well known process in metallurgy and is involved in many processes in semiconductor technology. In this process, thermal energy is provided to the atoms of the semiconductor, which results into increase of their kinetic energy, in turn enabling their diffusion and/or redistribution in the crystal if inhomogeneous composition is the case. Moreover, partial recovery of crystal periodicity can be achieved by thermal annealing in case of crystal defects introduced, by non-optimized growth of the crystal and/or deformations induced by surface bombardment and/or implantation of ions or atoms in the crystal. Thermal annealing of metal layers deposited on a semiconductor can lead to the formation of polycrystalline alloys, containing some or all of the different metals that were deposited, and in most cases atoms from

the semiconductor's surface or near surface region. However, it must be thermodynamically allowed for reactions to take place during thermal annealing, with temperature, ambient and duration affecting reaction kinetics for given semiconductor/ metal systems.

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CHAPTER 3

Characterization techniques

3.1 Introduction

Since a large part of this thesis is related to ohmic contact formation and device realization, electrical characterization (I-V, TLM) of contacts and devices is imperative. Moreover, optical characterization (PL, EL, optical pumping, time-resolved PL) of thin films and laser structures is necessary for exploring basic material properties, which can enable the design and growth of laser structures with reduced or even eliminated internal electric fields, which can ultimately boost performance of nitride-based optoelectronic devices. Finally, surface and interface characterization techniques (SEM, AFM, XPS) provide the means for obtaining surface morphology and electronic properties of the samples used, which is very important in the whole device fabrication procedure.

3.2 Electrical Characterization

3.2.1 I-V

I-V characterization is probably the most fundamental type of electrical characterization in the field of electronics. The electrical behavior and the function executed by a device are mostly determined by its characteristic I-V curve, and more specifically, from its shape and the values of quantities that are extracted by it. This curve can be obtained with current-voltage measurements, where the current flowing through the electrodes of the device is measured for each voltage applied and can be done either by employing ammeters and voltmeters if suitably connected to the device or by employing a curve tracer. This is the case in this thesis, where a curve tracer of Tektronix (model A370) was employed. The test device I-V curve is readily obtained in the curve tracer's screen, while there is the ability of extracting the I-V set of measurements in the form of ASCII files through a PC and a GPIB card, which is always advantageous for the data analysis procedure.

For the purposes of this thesis, I-V measurements were commonly employed for the characterization of metal/semiconductor (M/S) contacts, Light Emitting Diodes (LEDs) and few electrolyte-gate High Electron Mobility Transistors (HEMTs). Characteristic I-V curves of three different metal/semiconductor (M/S) contacts are shown in fig. 3.1. The exact geometry of the test pattern will be discussed below in more details when the TLM method is presented. Never-

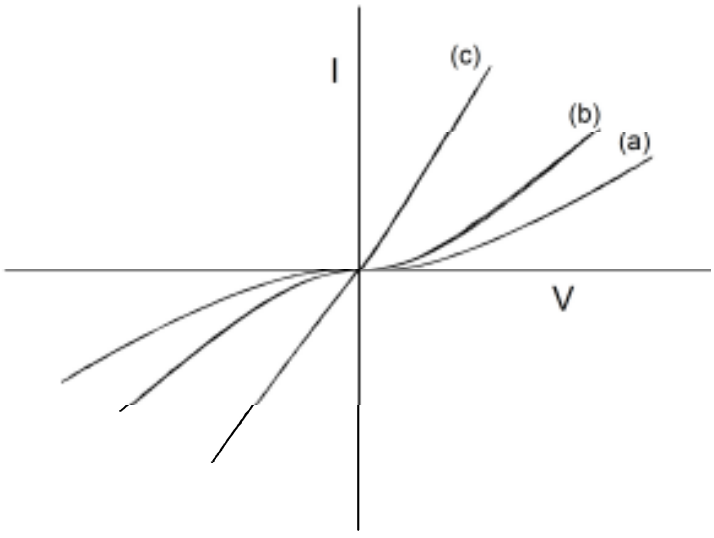

Fig. 3.1 *I-V curves of adjacent metal contacts from a TLM pattern. (a) and (b) are not ohmic and (c) is.*

theless, comparison of the curves shown in fig. 3.1 indicates that conductivity of contacts improves when going from case (a) to (b) and (c), while case (c) is the only that can be characterized as ohmic. The voltage dependence of serial resistance (dV/dI) in the other two cases implies that a potential barrier inhibiting carrier movement is formed at the M/S interface, with the barrier being more intense in case (a) than in (b). Despite the fact that the interface barrier's height and width values cannot be determined from these curves, the above qualitative analysis is feasible, which enables for useful conclusions to be formed. As will be seen in chapter 5, I-V characterization of M/S contacts can prove to be a very powerful tool in the ohmic contact formation procedure. The same holds for the electrical characterization of fabricated devices as will be seen in chapter 7, where quantities like turn-on and breakdown voltages, in the case of LEDs, and saturation current in the case of electrolyte-gate HEMTs can be directly determined from the corresponding I-V curves of the devices.

3.2.2 TLM

As can be easily understood, the current that will flow between two contact pads under an applied bias depends on the contact dimensions and the length of the current path inside the semiconductor. This is the reason why another feature is used to characterize ohmic contacts on semiconductors, since the resistance value obtained from I-V characterization depends on the size of the contacts and the geometry of the test pattern. This feature is the specific contact resistance ρ_c value, which is measured in Ωcm^2. In a simple vertical contact configuration, where the semiconductor layer is sandwiched between two contact layers, ρ_c would just be the product of the contact resistance times the area of the contact. In most devices however current flows laterally, in which case the above simplified relation for ρ_c is insufficient. The most widely used method to determine the specific contact resistance is the Transmission Line Model (TLM) first introduced by Shockley[1] and developed by others later on[2,3]. The situation according to the TLM is schematically illustrated in fig. 3.2, where the cross section of two adjacent con-

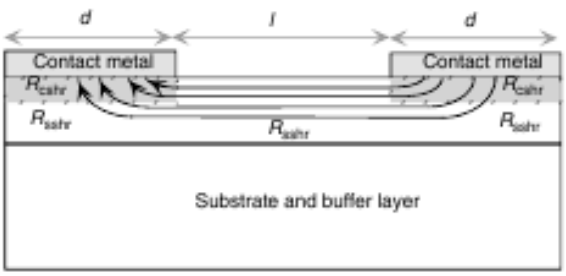

Fig. 3.2 *Cross-sectional schematic of two adjacent contacts in linear TLM.*

tacts and the structure beneath are shown[4]. The two contact pads of length d are separated by a distance l, which is almost equal to the length of the carrier's path through the semiconductor. Here, R_{sshr} and R_{cshr} are the semiconductor sheet resistance values in the bulk and at the region directly beneath the contact respectively. These two values are different (usually $R_{cshr} << R_{sshr}$) in the case of sintered/ alloyed contacts, where alloying of the semiconductor and the contact's material atoms results in metallic and/or intermetallic compounds formation beneath the contact region. In the case of as-deposited contacts, as is the case for contacts to p-type GaN studied in this thesis, sheet resistance is not expected to be different in the two regions, hence $R_{sshr}=R_{cshr}$. In this special case, the total resistance measured between the contacts of fig. 3.2 is simply:

$$R_T = 2R_C + \frac{lR_{sshr}}{Z},$$

where Rc is the contact resistance, Z is the contact width, l is the spacing between the contacts and R_{sshr} is the semiconductor sheet resistance. If a linear array of contacts as the one shown in fig. 3.3 (a) is fabricated, a set of R versus spacing l measurements can be obtained and if plotted together, the TLM plot (R vs. l), like the one shown in fig. 3.3 (b), is realized. The data points can be linearly fitted in case of ohmic contacts, with the slope S and y-intercept Y being equal to:

$$S = {R_{sshr}}/{Z} \text{ and } Y = 2R_C = \frac{2R_{sshr}L_T}{Z} = 2SL_T,$$

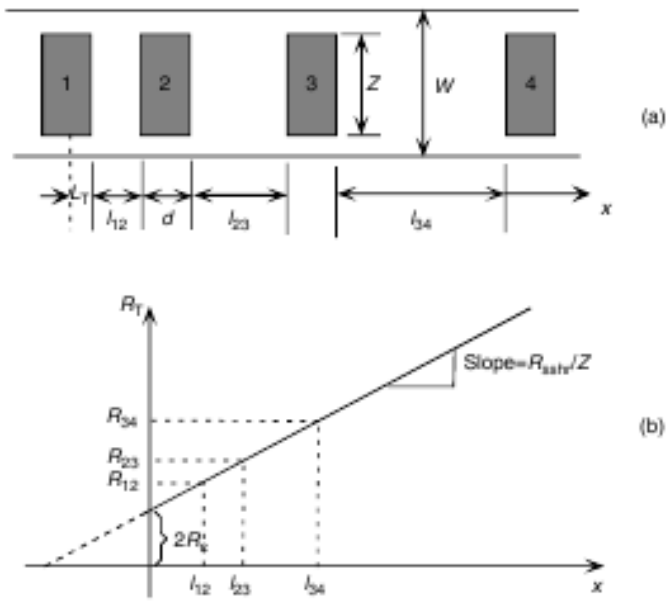

Fig. 3.3 *(a) Top view schematic of a linear TLM pattern. (b)From the linear relationship between measured resistance and spacing the specific contact resistance value the TLM plot is obtained.*

where L_T is the transfer length, defined as the 1/e distance of the potential curve inside the contact region measuring from the edge of the contact in the l direction. Actually, L_T expresses the length, which if multiplied with the contact width equals the area that most of carriers pass through. Therefore, from the slope and y-intercept of the TLM plot the sheet resistance and transfer length can be determined, leading to specific contact resistance determination from the relation:

$$\rho_c = R_{sshr}L_T^2$$

expressed in Ωcm^2. It has to be noted that transfer length is a measure of the validity of the calculations made to extract the ρ_c value, since a main assumption of the model ($4L_T<d$) should be valid for our values. The linear TLM pattern used in this work has square contact pads (left of fig. 3.4) of side Z=d=250 μm and spacing l of 5, 10, 20, 30, 40, 50, 100 and 200 μm.

In the linear TLM pattern geometry, contact pads should be formed on an etched stripe in order to eliminate current side effects. Consequently, mesas should be formed on the semiconductor before the contact material is deposited to form the contact pads (see section 2.3.4). Instead, if the circular TLM geometry is used, patterns do not need to be mesa isolated. This is favorable due to the one less step employed in the fabrication procedure and mainly due to the fact that all RIE-related contamination and/or damaging of the surface are avoided. The circular TLM pattern used here is the ring geometry one shown in the right microscope image of fig. 3.4, which enables the ρ_c determination by using a formulation similar to that of linear TLM[5]:

$$R_T = \frac{R_S L_T}{2\pi}\left(\frac{1}{r_{out}} - \frac{1}{r_{out}-d}\right) + \frac{R_S}{2\pi}\left(\ln\frac{r_{out}}{r_{out}-d}\right),$$

where R_T is the measured resistance for the i-th contact, R_S is the sheet resistance, r_{out} is the outer radius of the i-th contact, d is the corresponding spacing and L_T is again the transfer length. Note that for the last formula to be obtained, the assumption $4L_T<r_{out}-d$ has been made. Provided that the pattern has been designed so that $\left(\frac{1}{r_{out}} - \frac{1}{r_{out}-d}\right)$ is about constant for all contacts, a TLM graph can be obtained if R_T vs. $\ln\frac{r_{out}}{r_{out}-d}$ is plotted. In case of ohmic contacts, a straight line is the outcome, with slope and y-intercept Y being equal to:

$$S = \frac{R_S}{2\pi} \text{ and } Y = \frac{R_S L_T}{2\pi}\left(\frac{1}{r_{out}} - \frac{1}{r_{out}-d}\right).$$

Therefore, R_S and L_T can be determined by slope and y-intercept respectively, with specific contact resistance being given again by:

$$\rho_c = R_{sshr} L_T^2.$$

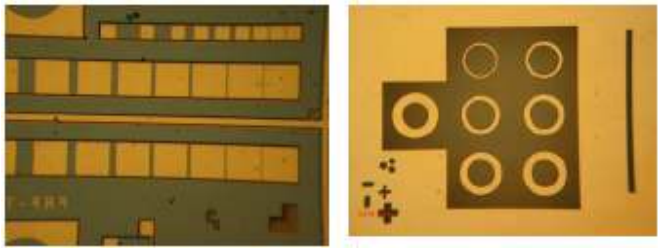

Fig. 3.4 *The linear (left) and circular (right)TLM patterns used.*

Table 3.1 *Dimensions of the contacts of the c-TLM pattern*

No	D_1 (μm)	D_2 (μm)	L (μm)
1	198	218	10
2	190	226	18
3	185	237	26
4	180	248	34
5	173	257	42
6	168	268	50
7	163	279	58

In table 3.1 are shown the dimension of the circular TLM pattern of fig. 3.4. Here, D_1 and D_2 are the inner and outer cycles diameters respectively and L is d, the spacing of each contact. Note that the quantity $\left(\frac{1}{r_{out}} - \frac{1}{r_{out}-d}\right)$ is around 0.02 μm^{-1} for all contacts.

3.3 Optical Characterization (PL, EL, Optical pumping)

Photoluminescence (**PL**) is a fundamental characterization technique for semiconductors, since it is based on the detection and recording of optical transitions occurring in a crystal after its carriers have been excited with light. A laser is usually employed as the light source, with its photons energy ≥ energy gap of the test semiconductor layer. In case of a multilayer structure, the requirement for the excitation photons' energy is to be ≥ than the smaller energy gap of the structure. Same holds for transitions occurring inside quantum wells (QWs), where the excitation photons energy should be ≥ $E_{e1\rightarrow h1}$ (energy difference of electron, hole ground states in the QW). The carriers that are excited far from the band edges are rapidly thermalized via phonons at states near the band edges, where they recombine with simultaneous photon emission[6]. This optical transition corresponds to a peak in the PL spectrum with energy position equal to the energy gap of the semiconductor. This peak is widened if there is a spatial variation in the energy gap along the crystal due to defects, impurities, clusters or any other crystal deformation. Therefore, conclusions concerning the quality of the test layer can be formed from this peak's FWHM. Same conclusions can be formed concerning the quality of a QW structure, since QW thickness variation or other effects can widen the corresponding PL peak's FWHM[7]. Another type of optical transitions are the ones mediated by states corresponding to donors and/or acceptors. Finally, exciton-related transitions can be detected , especially at low temperatures. The exciton corresponding PL peaks are narrower than the band-edge recombination one and are at lower energy in a PL spectrum. Moreover, temperature- and power-dependent PL can give valuable information about the quality of the test layer or structure, distinguish the type of each transition, estimate electric fields present in the QWs of the structure and many others. A more detailed presentation of PL can be found in many textbooks[6,7,8]. A schematic of the PL set-up is shown in fig. 3.5.

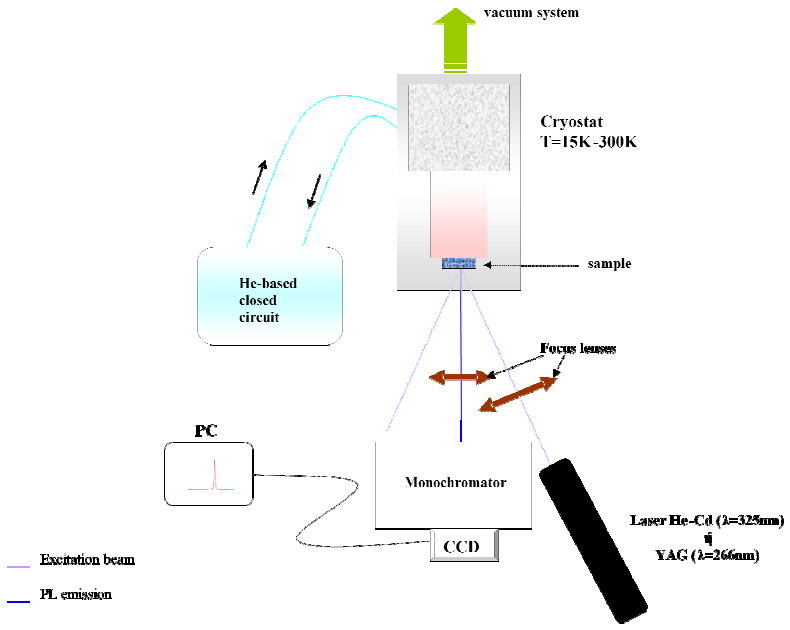

Fig. 35 *The PL set-up used.*

Electroluminescence (**EL**) is based on the effect of radiative recombination of electron-hole pairs that have been excited by the presence of a large electric field or under current flow. This effect is more pronounced in p-n or p-i-n junctions, which are the structures that all optoelectronic devices are based on. Actually, EL is the technique used for the optical characterization of optoelectronic devices, such as LEDs, LDs. In order for structures to be characterized with EL, current must flow through ohmic contacts therefore devices must have been fabricated and packaged in advance. The latter is a prerequisite if low temperature characterization is the objective, since the device must be placed inside a cryostat and at the same time be connected with the external electric circuit. For the excitation, either a voltage or a current source can be utilized, however special care has to be taken in the circuitry in order to avoid destruction of the device. Furthermore, in order to avoid heating of the device, pulsed excitation sources can be used.

Optical pumping refers to optical excitation of laser structures in order for laser action to be obtained. It is used for exploitation of basic properties of laser structures, such as laser threshold power densities and is not as demanding as electrical pumping of LDs concerning the design of the laser structure and the fabrication of the test pattern. For example, a laser structure to be optically pumped does not require p-type layers, which especially in nitrides is not so trivial (even if good quality p-GaN layers can be grown, the p-AlGaN case will still be an issue). The experimental set-up for optical pumping experiments is almost identical with that of PL (fig. 3.5) with the exception that special care has to be given both in focusing the excitation beam on a cavity formed on the sample surface (chapter 4) and collecting the emission from the cavity sidewall, where an optical fiber was used.

3.4 Surface/Interface Characterization (SEM, AFM, XPS)

3.4.1 SEM, AFM

Scanning Electron Microscopy (SEM) is a technique used for a high-definition visualization of the morphology of surfaces. It is based on the detection of secondary electrons and their projection on a screen in a way that produces an actual picture of the surface. Secondary are the electrons originating from the sample surface after it has been irradiated by the microscope's scanning electron beam. The transformation of the electron beam into an optical image roughly follows the operation principles of CRT TVs; higher electron energies correspond to brighter spots on the screen. The escape energy of a secondary electron depends on the material that it escapes from and the surface morphology. For example, two secondary electrons coming from the same material will have different energies if one comes from an edge and the other from a ditch, while two electrons coming from different materials on a flat surface will also have different energies. SEM is a powerful tool in microelectronics since surface observation is necessary for the overall evaluation of the processing procedure, especially after etching and metallization processes. This will become more apparent in chapter 4.

Atomic Force Microscopy (AFM) is a surface characterization technique used for imaging of surface morphology of solid samples in the atomic scale, as well as for determination of surface roughness. Its operation is based on atom-atom electrostatic interactions between atoms of the surface and the cantilever used. The latter is made of a material with low elasticity modulus as compared to that of the surface under investigation, which ensures that it is the cantilever that will be bent due to the repulsive forces between the atoms of the cantilever and the atoms of the surface and not the surface. For semiconductor surfaces characterization, aluminum cantilevers are usually employed, with Al ensuring that there will be a significant atom displacement in the cantilever (cantilever bending) even for weak repulsive forces. Therefore, by monitoring the cantilever bending, the surface hypsometric variations are monitored and with use of a computer, two- or three-dimensional images of the surface can be obtained.

3.4.2 XPS

X-ray Photoelectron Spectroscopy (XPS) is based on the photoelectric effect first discovered by Hertz and completely explained by Einstein in 1905. According to this effect, electrons can be extracted out of a material when it is irradiated with electromagnetic radiation of sufficient photon energy. The XPS technique was developed during the 60's, when progress in vacuum systems and electronics has permitted photoemission measurements. A schematic of the technique is shown in fig. 3.6: when a photon of energy hν enters the material is absorbed by a core electron of binding energy E_1. The electron then escapes the material with kinetic energy: $E_{kin.}=h\nu-E_B-(E_{vac.}-E_{Fermi})=h\nu-E_B-e\Phi$, where $e\Phi$ is the work function of the material, i.e. the minimum of energy required for an electron to escape from the material with zero kinetic energy (vacuum level). In a first approximation, the photoelectrons distribution corresponds to the one of the core electrons, although the picture is more complicated if one considers that not all states have the same probability to absorb a photon, while other effects that take place after the photo-ionization also complicate the picture. After the photoelectrons have escaped the material, they are collected by an energy analyzer, where their number and kinetic energy are recorded. For a known analyzer and the potential applied to it (necessary for the electrons to be able to pass the potential difference between the work functions of the sample and the analyzer), the binding energy of each photoelectron can be determined, with this energy value being characteristic of the original atom that was photo-ionized. In this way, in an XP spectrum there will be peaks in binding energy values characteristic of the target material. Moreover, binding energy of photoelectrons shifts according to the chemical state of the atoms of the target material, if for example these atoms chemically react with other species. Considering the fact that photoelectrons that contribute to XPS peaks (from 10 to 1500 eV energy range) come from a maximum depth of 1-6 monolayers normally to surface in order not to have been non-elastically scattered before they escape the material/air interface, XPS can be characterized as a surface characterization technique since this depth cannot exceed 12 nm in any case. Therefore, XPS can yield information about the kind of atoms present at the surface, their chemical

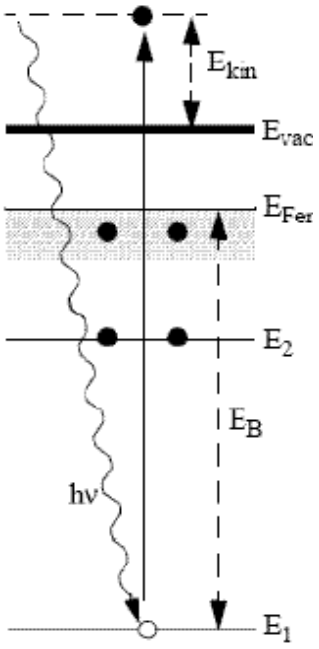

Fig. 3.6 *Schematic of the XPS technique's operational principle.*

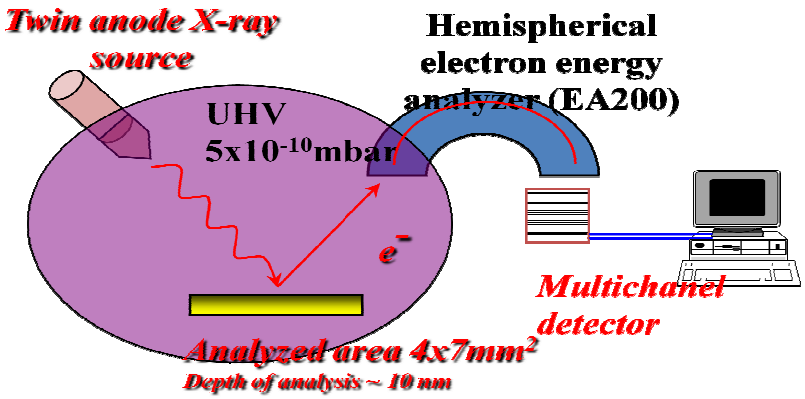

Fig. 3.7*The experimental set-up of the XPS technique (Surface Science Lab, Chemical Eng. Dept., University of Patras).*

state and their stoichiometry. The latter is feasible due to the fact that the area of an XPS peak is proportional to the number of photoelectrons with the corresponding binding energy of the peak. A schematic of the experimental set-up is shown in fig. 3.7.

Apart from the stoichiometry of surfaces, XPS can detect whether adsorbed species have chemically reacted with surface atoms to form a new compound or if they are just electrostatically attached to the surface. Moreover, with XPS measurements at an energy regime near the band edges, the energy distance between the Fermi level and the valence band maximum can be estimated. The importance of the information that XPS can provide will become apparent in chapter 5, where the mechanism of forming low resistance, as-deposited ohmic contacts to p-type GaN is under investigation.

5, where the mechanism of forming low resistance ohmic contacts to p-type GaN is investigated.

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CHAPTER 4

Nitrides Dry Etching

4.1 Importance of mesa quality

Semiconductor etching is one of the most important processes in device fabrication. The most cost and time efficient way to define device geometry is to employ dry etching techniques, such as RIE. The features formed on the sample surface after etching are called mesas and practically define the device (see subsection 2.3.3). With ideal devices assuming, in their majority, regular shapes, it is straightforward to understand that any variations in shape and morphology of the device can affect its performance. Such deviations from shape regularity are usually described by slope and roughness of mesa sidewalls. Ideally, a mesa is considered of good quality if sidewall slope is close to vertical, while sidewalls should be smooth on the atomic scale for crystal periodicity to remain unperturbed. The effect of mesa quality on the device characteristics is not the same for all materials and devices. An understanding of the mesa quality requirements in the case of optoelectronic devices, will be attempted in the rest of this section.

Mesa quality can have an effect on both electrical and optical characteristics of optoelectronic devices. Electrical characteristics of most devices rely upon bulk properties, while surface transport effects are usually neglected in the ideal case. As seen in chapter 1 for the case of p-i-n light emitting diodes (LEDs), carriers are injected from the n- and p- sides into the active i-region, where their recombination occurs with simultaneous photon emission. Sidewall roughness introduces surface states through edges, steps and point defects caused mainly by ion bombardment. The latter is affecting sidewall roughness, especially in the case of a large positive slope, where the kinetic and directional ions hit the sidewalls too. Note here, that ions are expected to impinge only on the unprotected areas of the surface, assuming that the top side of the mesa is sufficiently protected by the etch mask. These etching-induced surface states are usually located in the middle of the bandgap and mediate for phenomena such as carrier trapping, non-optical carrier recombination, surface charging and parasitic currents to be obtained. Such phenomena can have a devastating effect on device performance, especially when device dimensions get smaller and smaller. In addition, sidewalls are attacked by neutral reactive species during RIE (figure 4.1), which adsorb and possibly react with the semiconductor atoms to form by-products. If these by-products are not removed by kinetic ions, they will also act as traps or non-optical recombination centers, affecting again device performance. Therefore, obtaining mesas with sidewalls of minimized roughness improves electrical characteristics of optoelectronic, and not only, devices.

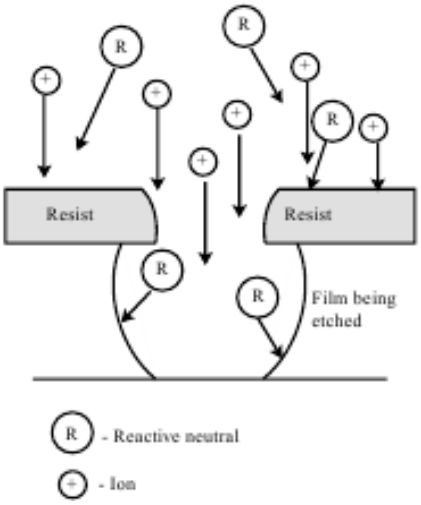


Fig. 4.1 *A schematic illustrating how sidewalls are attacked by neutral species during RIE*

Optical behavior of the device can also be affected by bad quality mesa, with the most extreme case being edge-emitting laser devices. In such devices, optical feedback of the laser's active region is achieved through light reflection on mesa sidewalls, acting as the cavity mirrors. The reflectivity of mesa sidewalls theoretically depends on emission wavelength λ and the semiconductor-air refractive index difference, while cavity mirrors should be vertical to in-plane light propagation, i.e. vertical to the sample surface. Moreover, sidewalls should be "mirror"-like (facets) in the sense that they should introduce no light scattering when a travelling wave reaches their surface and reflects

back. Any deviation from these ideal conditions introduces additional losses, increasing lasing threshold. If losses exceed gain then lasing will not occur at all. In the LED case, where lasing is not the objective, optical behavior of the device is not directly affected by mesa sidewall quality; however, mesa quality can have an impact on the electrical characteristics of the device, as discussed above.

A way to describe this sidewall roughness is through features existing on the sidewall, which have a depth (perpendicular to the sidewall surface) and a correlation length (parallel to the sidewall surface). Such features can efficiently describe roughness commonly observed on RIE formed mesa sidewalls, such as the one shown in fig. 4.2. The sidewall surface of the mesa depicted resembles a wavy, curtain-like surface, with the corresponding depth and spatial period (correlation length) being easily observed. Vurgaftman and Singh[1] theoretically estimated the sidewall reflectivity dependence on the sidewall roughness, using depth and correlation length (L) as the variables. The main results are presented in fig. 4.3, where deviations from the original mode shape inside the cavity have been taken into account.

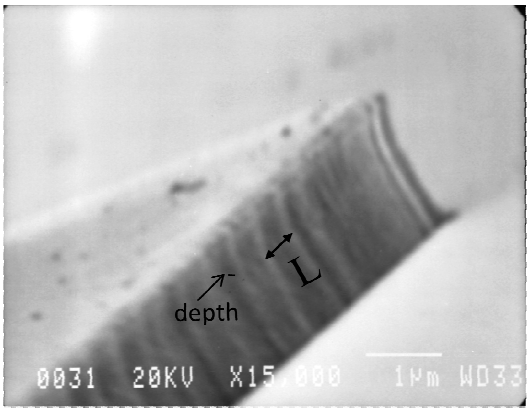


Fig. 4.2 *Typical mesa sidewall with feature depth and correlation length being indicated.*

For zero feature depth, the reflectivity of smooth semiconductor/air interface is obtained, with the 0.4 value corresponding to the theoretical reflectivity value of dielectric/air interface with the dielectric refractive index being ~ 3.5. The major outcome of this study is that, even for a much smaller than λ feature depth value (see fig. 4.2) of ~ 0.1λ, the drop in reflectivity may vary from 5-6% for L=0.1λ up to 25% for L=0.3λ. Therefore, sidewall roughness values often refer to the correlation length L (fig. 4.2), assuming that the approximation: feature depth << λ is valid. In this light, the sidewall roughness in fig. 4.2 is estimated to be ~ 300 nm, with the feature depth being much smaller.

Slope of mesa sidewalls is an important feature too. If lasing is to occur inside a Fabry-Perot cavity, the two plane cavity mirrors should be exactly parallel. The latter is relatively difficult to be achieved in large-scale cavities, where deviation of few arc seconds can be detrimental in achieving lasing. However, short cavities (< 1 cm) are less sensitive to deviations of mirrors

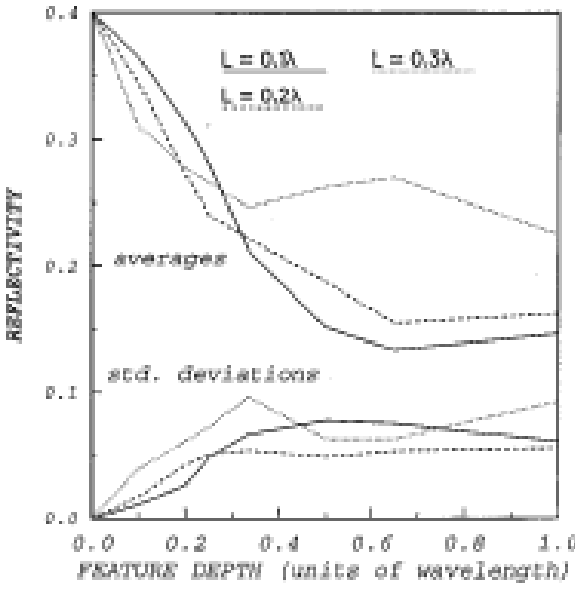


Fig. 4.3 *Calculated results of sidewall reflectivity dependence on feature depth for 3 different correlation length values (after Vurgaftman and Singh).*

from being parallel to each other, which has enabled the widespread use of Fabry-Perot configuration in semiconductor lasers. Nevertheless, the closest is the sidewall slope to verticality, the better is for gain.

As will be seen in chapter 6, the emission wavelength λ of typical InAlGaN/GaN or InGaN/GaN QWs, commonly used as the active region in nitride-based LEDs and LDs, range from 350 to 450 nm. Even shorter emission wavelengths can be obtained if GaN/AlGaN QWs are used. For a characteristic refractive index of ~ 2.5 for nitrides in this wavelength range, the results of figure 4.3 point that the roughness-induced drop in reflectivity will range from 5-6% for 16 nm sidewall roughness to 25% for 50 nm. Non-optimized mesas, like the one in fig. 4.2, will intensively scatter light, exhibiting reflectivity values reduced by as much as 50%, which makes them unsuitable for optical cavity. In this light, sidewall roughness has to be minimized in order for cavity mirrors losses to be minimized, with the lower roughness obtained on the sidewalls, the better for lasing. Therefore, short emission wavelengths of nitrides makes mesa formation a very challenging task requiring careful optimization of lithography and RIE procedures, especially in the LD case. Fortunately, LEDs are not so sensitive to mesa quality and therefore the procedure is not as demanding as for LDs.

4.2 Importance of masking material

It must be clear by now that pattern formation through dry etching requires utilization of an etch-mask for sufficient protection of the material that will not be etched. These areas of the

sample should remain intact by plasma species, in the sense that their properties should remain unaffected. As can be seen in the schematic of fig. 4.1, plasma species attack the sample surface in a uniform way, with the processes responsible for etching occurring on the masking material's surface as well, i.e. impinging kinetic ions and reactive, neutral species. Ions penetrating the etch-mask can hit material underneath causing point defects and lattice deformation, which can lead to degradation of electrical and optical properties. The masking material therefore, should be either etch-resistant, or at least be etched with an etch-rate lower than that of the semiconductor and should remain thick enough to sufficiently protect material underneath. Therefore, the right choice of masking material is a very important issue affecting the outcome of the procedure.

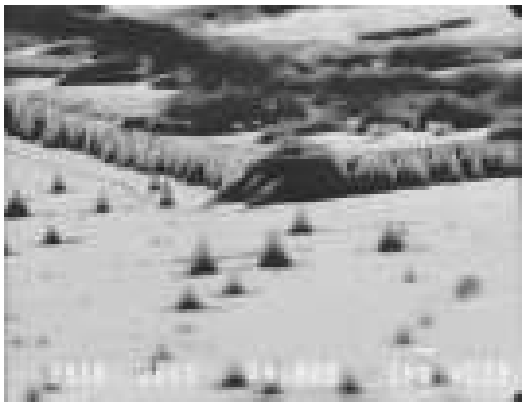


Fig. 4.4 *SiN etch-mask pattern after RIE. Intense degradation and lost of pattern dimensions are readily observed.*

There are some cases however, where partial etching of the etch-mask can be beneficial. As discussed in section 2.3.3, sidewall slope is mainly affected by chemical mode of etching, corresponding to reactive species attacking mesa sidewalls, as can be seen in the schematic of fig. 4.1. If the etch-mask is partially etched, some of the material removed from it, or by-products formed from it, will cover the sidewalls and partly protect them from these randomly moving reactive species, suppressing in this way the chemical component of etching. This is desirable in the case of LDs, where the right choice of etch-masking material can favor the verticality of mesa sidewalls. Of course, the above mechanism should be occurring in such a way that the dimensions and/or shape of the pattern are not lost, as is the case shown in fig. 4.4, where strong degradation of the SiN etch-mask during RIE has led to bad quality mesa and loss of pattern dimensions. Such a material is obviously unsuitable for use as an etch-mask.

Considering the above, the choice of the etch-mask is highly dependent on the application and the plasma chemistry used. For nitrides etching, chlorine-based chemistry is employed, with BCl_3 and Cl_2 being the gases mainly used. Materials that have been used as etch-masks for such plasma chemistry are Ni, Cr, Ti, Al, SiO_2 and PR. The metals and dielectric mentioned above, are highly resistant to this plasma chemistry, exhibiting zero, or practically zero, etch rate and their use is preferred when the slope and mesa dimensions are not critical and/or long RIE runs have to

be performed. PR on the other hand, such as AZ 5214, is also etched in this plasma chemistry. However, their use as the etch-mask is preferred in cases where mesa sidewall slope and roughness are important, due to sidewall protection from plasma reactive species, a mechanism described above. Furthermore, both slope and roughness of PR patterns' sidewalls can be controlled in a more direct way through the lithography procedure (see paragraph 2.3.2), in contrast to the metal and dielectric counterparts, where additional processes, like lift-off, or patterning and etching after their deposition, must be employed prior to semiconductor etching. Nevertheless, sufficient material protection throughout the whole etch process is still a requirement, and towards this end the lithography parameters must be adjusted to enhance mechanical and chemical stability of the PR etch-mask, as well as increase its thickness. The rest of this chapter presents the results of the experimental work on the highly demanding topic of optical cavity formation in nitrides. These results will be presented with respect to two main considerations: mesa sidewall morphology (slope and roughness) and RIE induced material damaging and means to avoid it.

4.3 Results on slope and roughness of mesa sidewall

Optical cavity formation through dry etching permits the realization of optical pumping experiments, which are very helpful in exploring lasing properties of nitride-based active region structures, as well as comparing different heterostructures, as will be highlighted in chapter 6. In this way, optimized active region structures (layers' composition and thickness, number of layers) can be designed and grown for potential use in nitride LDs with improved operation characteristics. As mentioned above, optical cavity formation is a highly demanding process, and if the acquired know how is utilized for other less demanding applications, such as nitride-based LEDs, Schottky diodes, sensors, transistors and others, operation characteristics of devices in all cases can always be favored by improved mesa quality.

Our work on nitride etching was essentially divided in two main issues: the etch-mask preparation and the etching procedure itself. These two issues are interconnected, since etch-mask preparation should be customized for specific etching conditions. Consequently, feedback of the etch-mask preparation procedure after evaluation of the resulting mesa is usually needed in order for the desired result to be finally obtained. The results of lithography and RIE procedures

are evaluated in this work by utilization of Scanning Electron Microscopy (SEM), which enables sidewall roughness and slope estimation after observation of the PR patterns and mesas formed on the surface of nitride films. The PR patterns are usually observed with SEM both before and after the RIE run, while mesas can be observed after PR removal in acetone. Moreover, PR and mesa thicknesses where measured with an A-step 100 profilometer of Tencor Instruments. Unfortunately, an AFM image and hence an rms value of this sidewall roughness is not feasible due to small dimensions of the mesas (~1μm height). The following two paragraphs present the results on PR etch-mask preparation and etching of nitride films respectively.

4.3.1 Photoresist etch-mask preparation

The basic idea here is that in order for smooth and vertical mesa sidewalls to be obtained, the starting PR sidewalls should be as smooth and vertical as possible. Therefore, the lithography procedure should be optimized towards this end, meaning that a set of optimized values for the parameters controlling the lithography steps should be found. These steps are: spin-coating, soft-bake, exposure, development and hard-bake and are the typical steps employed to pattern photoresist AZ 5214, which is the PR used here as the etch-mask. A non-optimized lithography procedure used for common lift-off or etch-mask purposes is the following:

Spin-coating: 4,000 rpm, 20”
Soft-bake: 85°C, 20’
Exposure: 13 mW/cm^2, 3” **(Lithography 1)**
Development: AZ 400/Di-H_2O: 1/4, 20-30”
Post-bake: 110°C, 10’

The above lithography procedure yields a PR layer thickness value of 1.1-1.2 μm and a typical resulting PR pattern is shown in fig. 4.5. In that pattern’s sidewall, a roughness of ~ 400 nm and profound positive slope is observed. Considering the high degree of directionality of the RIE process, it is very possible that the resulting sidewall quality of mesa formed, will be the same or even worse than that of the starting PR sidewall. Therefore, the lithography procedure should be improved in order to meet the requirements of optical cavity formation.

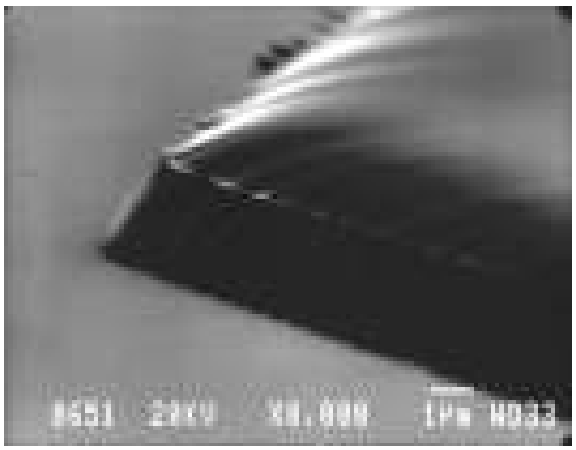


Fig. 4.5 *PR pattern formed with the non-optimized lithography procedure 1.*

Sufficient material protection has to be obviously considered as well; improved mechanical stability combined with increased thickness of the starting PR etch-mask can ensure better protection for longer processes. Improving PR layer's mechanical properties is mainly achieved by its post-bake and/or application of other treatments, such as the chlorobenzene one, which will be discussed in section 4.4. Thickness of the PR etch-mask is mainly determined by spin-coating (thickness is also affected by the bake steps) and towards this direction the spin velocity was reduced to 3,000 rpm, which finally results in a PR pattern thickness of 1.7-1.8 μm. Further lowering spin velocity can affect thickness uniformity, which is undesirable if one wants to be able to uniformly control the PR pattern's quality across the sample's surface. Taking this into account, spin-coating's duration is increased to 30" to ensure that resist has completed spreading over the surface. Of course the edge bead effect is always present (paragraph 2.3.2), especially for small sized samples as is the majority in this work. The 20' soft-bake step at 85°C in an oven is kept as is, because this step is related to partial moisture and solvent removal from the PR film, which is more efficient at this temperature with the 20'being enough for the increased PR thickness. Soft-bake of the PR on a hot plate is better to be avoided when lithography is demanding, due to the one-sided heating of the sample, which might result in an unexpected PR behavior during the next steps.

The increased sidewall roughness of PR patterns seen in fig. 4.5 and the deviation from verticality have their origin mainly in the exposure step of the lithography. Sidewall roughness was described in section 4.1 as features existing on the sidewall, having a depth and a correlation length, resembling like the folds of a curtain. These features originate from the shape of the SiO_2-CrO_x border lines of the photo-mask's patterns, which after a number of exposures it transforms into a sinusoidal-like curve rather than the original straight line. This effect might be related to thermal stress of the oxide patterns after their heating from the light absorbed and is more intense as the number of exposures increase. Ideally a photo-mask should be replaced every 100 exposures due to this effect. Therefore, sidewall roughness of PR patterns is always present with this

roughness being acceptable for common applications. Another thing to be considered is the fact that photo-masks need to be cleaned every 2-3 exposures due to PR residues after intimate contact with the samples during the exposure. This is done with the organic degreasing procedure (acetone/propanol/Di-H_2O) described in paragraph 2.3.1, since PR is a polymeric (organic) material. The positive sidewall slope on the other hand, has its origin to the undesired diffraction effects occurring on the SiO_2-CrO_x border line (paragraph 2.3.2). Even if the light beam is completely normal to the sample surface and intimate contact between the sample and the photo-mask is ensured, there will still be a minimum, practically imperceptible, positive slope.

In order to examine the relation between the exposure time and the sidewall roughness, different exposure times were tried and the results were observed with SEM. For all experiments, the MA6 mask-aligner with the 356 nm lamp was used, while power of light impinging on the sample was kept constant and had a value of 13 mW/cm^2 as measured by a power meter. The non optimized exposure time is 3 sec (1.1-1.2 μm thickness) and the corresponding development time is 20-30". The 20-30 sec development time corresponds to the time needed for exposed PR removal to be visually observed including a 5 sec additional time to ensure its complete removal. For comparison reasons, this 5 sec additional time after visual PR removal was kept the same for all exposure time experiments. These include 4 different exposure times: 2.5, 3.0, 3.5 and 4.0 sec, with these values taking into account the increased PR thickness (1.7-1.8 μm) after spinning at 3,000 rpm. After observation of each lithography's outcome at the SEM, the best results, in terms of sidewall roughness and slope, were obtained for the 3 sec exposure time. In the 2.5 sec case, traces of PR always remained at the supposedly exposed areas of the surface, therefore being less than the minimum time required. The 3.5 and 4.0 sec exposure times gave worse results as compared with the 3 sec, with the 4.0 sec case being worse than the 3.5 one. After these results, experiments with 2.7-3.1 sec exposure times were performed and indicated 2.8 sec as the exposure time giving the best results. A SEM picture of a PR pattern exposed for 2.8 sec is shown in fig. 4.6. Despite the improvement of the observed roughness (~ 250 nm) in fig. 4.6 as compared to that of fig. 4.5 (~ 400 nm), **it is clear that optimizing the**

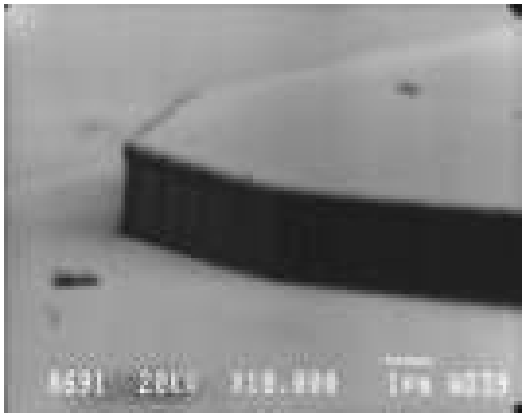


Fig. 4.6 *Typical PR pattern exposed for 2.8 sec. A roughness of ~ 250 nm can be observed.*

exposure time alone cannot completely eliminate the roughness transfer from the SiO_2-CrO_x interface to the PR sidewall. The same applies for the sidewall slope, despite the improvement observed.

One effect that should be taken into consideration, if optimization of the exposure step is the objective, is the edge bead effect, discussed in paragraph 2.3.2. Due to edge bead, PR layer is thicker at the edges of the sample as compared to the center. Consequently, when sample comes in contact with the photo-mask, the areas of the PR film that are actually in contact with the photo-mask are at the edges, while there is a gap formed between the central area of the PR film and the photo-mask (fig. 4.7). As a result, diffraction effect at the SiO_2-CrO_x border lines is more intense in the central area of the sample. As a way to overcome this issue, the edges of the PR layer should be removed prior to the exposure step. Therefore, an additional step is added to the lithography procedure (edge removal), where sample is exposed, after soft-bake, with the central area of the sample covered with an obstacle of the same geometry with the sample but smaller in size. Subsequent dipping of the sample in the developer will remove edges of the PR film, resulting in increased thickness uniformity of the remaining PR film. Observation of the resulting PR patterns with SEM, confirmed the above considerations, **with edge removal step favoring mainly the verticality of PR patterns' sidewalls, while improvement of roughness was less pronounced and in terms of feature depth's reduction.**

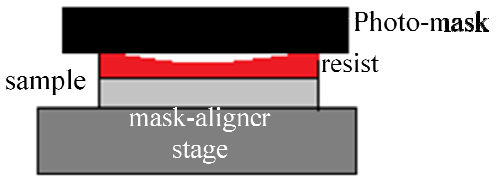


Fig. 4.7 *Photo-mask in contact with PR covered sample. A gap between the central area of the sample with the photo-mask due to edge bead effect is observed.*

After having optimized the exposure step of lithography, next comes development of the PR film. The development time for 2.8" of exposure is ~ 75 sec, with this time including the 5 sec interval described above. In order to check if roughness and slope are related to the development time, samples remained in the developer solution (AZ 400:Di-H_2O = 1:4) for 20% additional time, i.e. ~ 90 sec. The obtained results showed a clear improvement of the sidewall roughness, indicating that some exposed areas were illuminated with a smaller light dose, due to diffraction effect, and therefore needed more time in the developer for their removal. To On the other hand, dipping the sample in the developer for even more time results in increased roughness, most probably due to the opposite effect; areas that shouldn't normally be illuminated and have been

due to diffraction effect, start to detach from the sidewalls. Therefore, the 20% additional development time was found to improve sidewall roughness and was included in the optimized lithography procedure. A SEM picture of the resulting PR pattern sidewall with the optimized exposure and development steps, including edge removal, is shown in fig. 4.8, where the improvement in the sidewall roughness and slope is readily visible. **It seems that in order for roughness reduction and verticality of the PR patterns sidewalls to be obtained, the offered light dose during exposure should be restrained close to its minimum value, leading to slow and more controllable development of the exposed PR film, with intimate contact of the PR film and the photo-mask through edge removal being necessary for diffraction effects and other undesired effects to be minimized.** The estimated roughness value of sidewalls in fig. 4.8 is ~ 100 nm and their slope is very close to zero (vertical). This slope is satisfactory for the purposes of optical cavity formation. On the other hand, roughness needs to be further reduced in order to ideally reach a value of < 50 nm. Despite intense efforts to further optimize the lithographic procedure, roughness wasn't significantly reduced. Therefore, the origin of this persistent ~ 100 nm roughness, always present on the sidewalls, must be sought elsewhere, and more specifically to the original photo-mask pattern. If the supposed straight line of the photo-mask pattern has a wavelike shape of this value in its origin, then the resulting sidewall roughness will be of the same value at the best case. This was also confirmed by the photo-mask vendor, whose claim is that, photo-masks fabricated with the usual fabrication procedure are characterized by this 100 nm wavelike fluctuation of border line's shape and if one wants to get rid of this sidewall roughness, a specially fabricated photo-mask must be ordered and used. Indeed, a specially fabricated photo-mask was ordered and the results are shown in fig. 4.9, where one can clearly see the difference between exposure with an old and a new, specially fabricated photo-mask, as this is the only processing difference between the results of fig. 4.9 (a) and (b), with the lithography procedure used being the optimized one for both results. **The results indicate that this procedure yields sidewalls of**

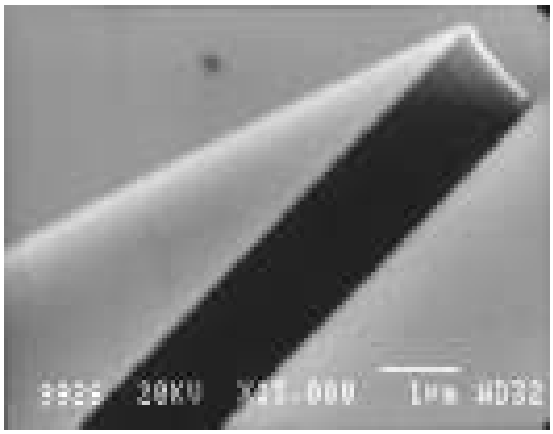


Fig. 4.8 *PR pattern after optimization of the exposure and development steps of the lithography.*

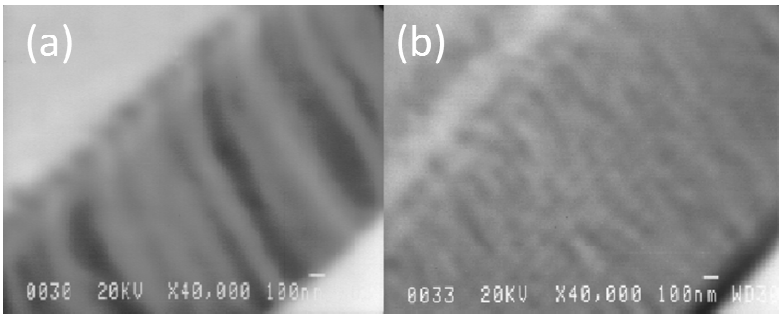


Fig. 4.9 *PR pattern sidewalls using an old (a) and a new, specially fabricated (b) photo-mask. In (b) roughness is imperceptible.*

roughness > 100 nm when a beaten photo-mask is used, while the same, optimized procedure yields sidewalls of imperceptible roughness when a new photo-mask is used.

The above remarks point out the fact that lithography procedure is optimized enough to enable us to proceed with nitrides etching. However, there is still the issue of photo-mask's degradation-induced roughness and the PR patterns mechanical stability enhancement for better material protection. Concerning the latter, mechanical properties of PR layer can be improved if residual moisture and solvent, existing in its volume, is removed and this occurs during the **post-bake** step of lithography. During post-bake however, another effect is the one that really enhances PR layer's mechanical stability, and this is cross-linking of polymeric chains inside the PR volume. This effect is accompanied by PR layer's reflow, which also occurs during post-bake and affects the shape of mesa sidewalls with a pronounced effect on the slope of sidewalls, as can be seen in fig. 4.10, where SEM picture of a PR pattern sidewall before and after the 110°C for 10' post-bake step is shown. In the case of optical cavity formation, the PR patterns depicted in fig. 4.10 (b) are not suitable for use as the etch-mask due to the strongly positive slope of the sidewalls, while it is acceptable in cases where slope of the resulting mesa sidewall is not

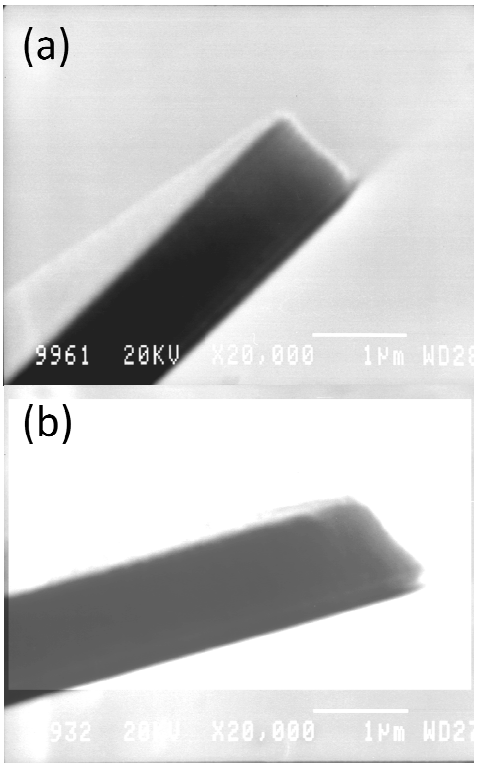


Fig. 4.10 *PR pattern before (a) and after (b) 10 min post-bake at 110°C. The positive slope observed in (b) is due to PR*

important. Clearly, a compromise between enhanced PR layer stability and sidewall slope deformation is needed. With cross-linking and reflow being more intense as bake temperature and duration increase, different post-bake conditions (temperature, duration) were tried for the PR etch-mask preparation and the samples were consequently subjected to the same RIE process. After RIE, the etch rate of PR patterns in each case was determined through thickness measurements. This analysis showed a slight PR etch rate reduction when post-bake is performed at 110°C as compared to 85°C, while the effect of post-bake duration on PR etch-mask endurance is negligible. Therefore, the set of 85°C for 5' was chosen as the optimized post-bake conditions. The corresponding sidewall deformation for these conditions is almost imperceptible, while a slight improvement of PR endurance is observed. At this point, it would be useful to summarize the optimized lithography procedure, denoted as lithography procedure 2:

Spin-coating: 3,000 rpm, 30"

Soft-bake: 85°C, 20'

{Edge removal} **(Lithography 2)**

Exposure: 13 mW/cm^2, 2.8"

Development: AZ 400/Di-H_2O: 1/4, ~ 90"

Post-bake: 85°C, 5'

The above lithography procedure results in PR patterns of ~ 1.7 μm thickness, with practically vertical sidewalls and roughness determined by the photo-mask used. Whether thickness and endurance of PR patterns are sufficient to protect material underneath during etching, remains to be seen when nitrides etching experiments begin and characterization of etched samples is performed. This will be considered in the last section of this chapter.

In the meanwhile, roughness introduced by photo-masks still remains an issue. This roughness depends on the photo-mask condition and cannot be further reduced through the lithography procedure. A possible way to control this roughness is by employing a RIE process, known as **oxygen plasma ashing,** which utilizes O_2 as the etching gas and is used when organics or polymers, like PR, have to be removed from the sample surface. In practice, reactive oxygen species react with carbon atoms from the polymeric chains to form CO and/or CO_2, which are volatile and are removed by chamber's pumping system. In many applications this process is used after the main etching process for in situ removal of PR etch-mask remainings, instead of using acetone. The idea here though, is to employ an oxygen plasma process prior to the main etching process, having as an objective to possibly smoothen PR pattern's sidewalls without sig-

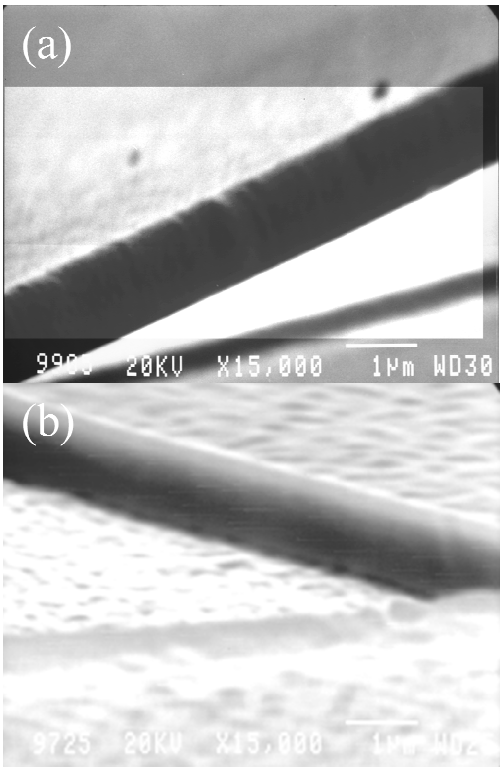


Fig. 4.11 *PR pattern before (a) and after (b) oxygen plasma ashing process. A clear smoothening of the sidewall is readily observed.*

nificantly reducing initial thickness and/or deteriorating PR pattern's properties. Therefore, the O_2 RIE process to be developed should be a mild etching process with chemical component of etching dominating over the physical, without affecting slope of sidewalls, which is close to verticality after the lithography procedure. The latter was confirmed by the results of O_2 RIE process experiments, where a decrease of rf-power from 100 to 50 W favored sidewall roughness without affecting slope. Same was the case when chamber pressure during etching increased from 20 to 50 mTorr. The results of a 5' O_2 RIE process, with parameters: 20 sccm O_2 flow, 50 W rf-power, 50 mTorr chamber pressure are shown in fig. 4.11 (b), whereas the initial PR pattern can be seen in fig. 4.11 (a) for comparison. Although the image quality of the two SEM pictures is moderate (charging effects during SEM), **smoothening of sidewall roughness is clearly obtained, most probably due to sidewall feature depth's reduction through the oxygen RIE process.** Especially in the case of fig. 4.11 (b), the sidewall roughness is almost imperceptible. As a side effect, this process results in size reduction of PR patterns. For 5' exposure in the above mentioned oxygen plasma process, a reduction in PR pattern thickness of ~ 300 nm is measured. Due to chemical-like character of this RIE process, material must be removed from the sidewalls as well, resulting in reduction of the lateral size of PR patterns. Although this reduction is estimated to be less than 2x300 nm in each x-, y- directions, if crucial, it can be incorporated in the photo-mask design. Whether the remaining PR pattern thickness is sufficient to protect material underneath will be discussed in section 4.4.

In conclusion, the lithography procedure was optimized for use of PR as an etch-mask for optical cavity formation experiments. **The objectives were PR patterns sidewall roughness minimization and verticality, as well as increased endurance in nitrides plasma etching conditions. This research has led to the optimized lithography procedure 2, which along**

with a 5' O_2 RIE (50 W, 50 mTorr, 20 sccm O_2) step constitute the etch-mask preparation procedure. The overall behavior of PR etch-mask will be evaluated in direct nitrides RIE experiments, which are discussed next.

4.3.2 RIE parameters

Defining the mirrors of an edge-emitting laser is a demanding process in terms of facets' desirable roughness and slope, as mentioned earlier. With PR AZ 5214 as the etch-mask and an optimized procedure for PR patterns preparation of superior sidewall quality, in terms of roughness and slope, dry etching research for nitride-based laser cavity formation should ideally lead to a set of optimal RIE conditions which assure that the etch process does not introduce additional roughness on the facets, as compared to the initial PR etch-mask patterns, while at the same time, the anisotropic (kinetic) component of the dry etch procedure is sufficiently enhanced to obtain facets as vertical as possible. The RIE parameters that have to be investigated are: etch gas chemistry and gas fluxes (partial and total), the chamber pressure during etching, the rf power of the plasma generator, and the dc-bias.

There are numerous gas combinations that have been used for dry etching of nitrides, with each one of them containing at least one halogen-based compound (BCl_3, Cl_2, SF_6 and others) as the main etch gases and Ar, N_2, O_2, CH_4 as additives. The use of such highly reactive compounds is almost mandatory in the III-nitrides case, since their wurtzite crystal structure and the relatively high bonding energy give rise to the increased chemical inertness and enhanced mechanical stability which characterizes these materials. The RIE system in MRG, which is the one used in this work, offers the feasibility of using either chloride- or fluoride-based chemistry (BCl_3, Cl_2 or SF_6), as the main etch gases and Ar, N_2 or O_2 as the additives. Chloride-based chemistry was chosen among the two available chemistries, due to the volatility of all possible etch by-products, since for instance, AlF_3 is not volatile if fluoride-based chemistry was used instead. The above consideration is of fundamental importance, since surface coverage by non volatile species can hinder RIE process and, in the worst case, terminate it. Furthermore, the dry etching process optimized here should be able to etch GaN, ternary (AlGaN, InGaN) and quaternary (InAlGaN) nitride alloys, which can be found in typical LED and laser structures. In this light, BCl_3 was em-

ployed as the main etch gas, while the effect of Ar and/or Cl_2 addition in the plasma was investigated.

Argon is an inert gas and its addition to the plasma is expected to enhance only the physical component of etching. On the other hand, Cl_2 is a highly reactive gas and its incorporation in the plasma is expected to mainly enhance chemical mode of etching. Preliminary experiments, using 25 mTorr as the chamber pressure and BCl_3 flow of 20 sccm, indicated that rf power should be restricted to 50 W, since a reduction from 150 to 100 and finally 50 W favoured PR etch-mask endurance and sidewall roughness, while lowered etch rate. By varying BCl_3 flow from 20 to 60 sccm for this initial set of parameters, an increase in the etch rate, sidewall roughness and slope were observed with SEM, indicating that the main etching mechanism for nitrides and this chemistry is through reactive BCl_x species, with chemical component of etching being the dominant. Ar incorporation gave intense sidewall roughness for all different flow ratios, while slope improvement could not compensate for the increased roughness, as can be seen in fig. 4.12 (a). It seems that, the purely mechanical way of removing material from the sample surface through Ar atoms in the case of nitrides, requires increased rf power values, which results in increased sidewall roughness. By adding Cl_2 in the plasma on the other hand, sidewall roughness began to improve significantly but an intense positive slope, as a result of the enhancement of chemical component of etching, is observed, as shown in fig. 4.12 (b). In order for a compromise between the two distinct etching mechanisms to be found, experiments with varying $BCl_3/Cl_2/Ar$ flow ratios followed, with BCl_3 flow being set to 20 sccm, rf power to 50 W and chamber pressure to 25 mTorr. The best results were obtained for zero Ar flow, and hence, it was decided that Ar will not be further used due to roughness introduced with its use. Next, different BCl_3/Cl_2 flow ratios were tried, with a ratio of 10/1 giving the best combination in terms of roughness and slope, as seen in fig. 4.12 (c) where 20 sccm BCl_3 and 2.0 sccm Cl_2 were used. One can see that, mesa sidewalls of fig. 4.12 (c) have lower positive slope as compared to the one in fig. 4.12 (b), where 20 sccm BCl_3 and 4.0 sccm Cl_2 were used (5/1 flow ratio), while roughness is practically the same. The results in fig. 4.12 (c) move towards the right direction, with a lot of improvement still needed in both roughness and slope.

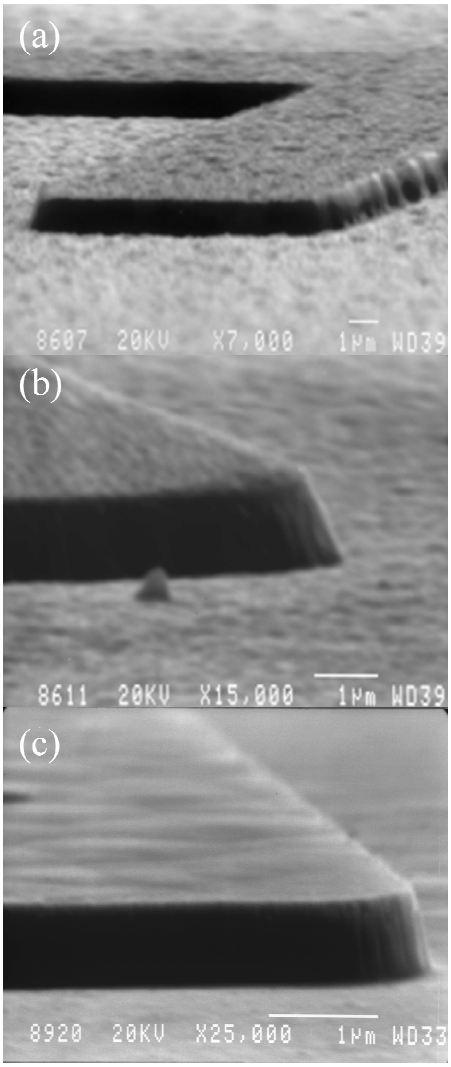


Fig. 4.12 *Mesas after chloride RIE using BCl_3/Cl_2 ratio of 5 (b) and 10 (c).Addition of Ar (a) increased roughness under all conditions.*

A way to enhance the chemically-assisted kinetic component of the etching is to decrease the gas pressure inside the chamber during RIE, which results in longer mean free path for ions to become more kinetic. **By reducing pressure from 25 to 20 and 16 mTorr, sidewall slope improved, but a simultaneous increase in roughness was observed.** It has to be noted here that, 16 mTorr is the minimum pressure that can be obtained in the RIE system used for 20 sccm BCl_3 and 2.0 sccm Cl_2. In order to further reduce pressure and sidewall slope, BCl_3 flow is reduced down to 10 sccm and, in the same time, experiments with BCl_3/Cl_2 flow ratios were performed for roughness reduction. **Finally, a compromise between the chemical and the kinetic components of the etching process was achieved by setting the BCl_3/Cl_2 ratio equal to 7 (7 sccm BCl_3/1.0 sccm Cl_2) and the gases' pressure during etching around 10 mTorr.** As can be seen in fig. 4.13, pressure reduction has favoured slope (practically 0°) and yielded roughness of ~ 180 nm, which is greater than the one of the initial PR etch-mask, while features' depth . Therefore, the chlorides-RIE process should become milder, while keeping the anisotropic character.

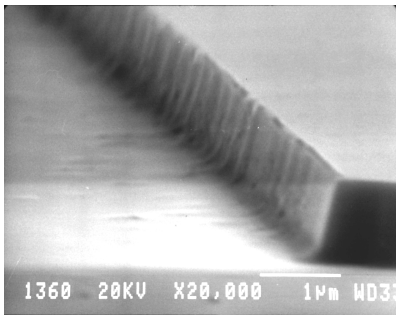


Fig. 4.13 *Mesa after RIE using 7 sccm BCl_3/1.0 sccm Cl_2 and 10 mTorr chamber pressure. A compromise between roughness and verticality is achieved.*

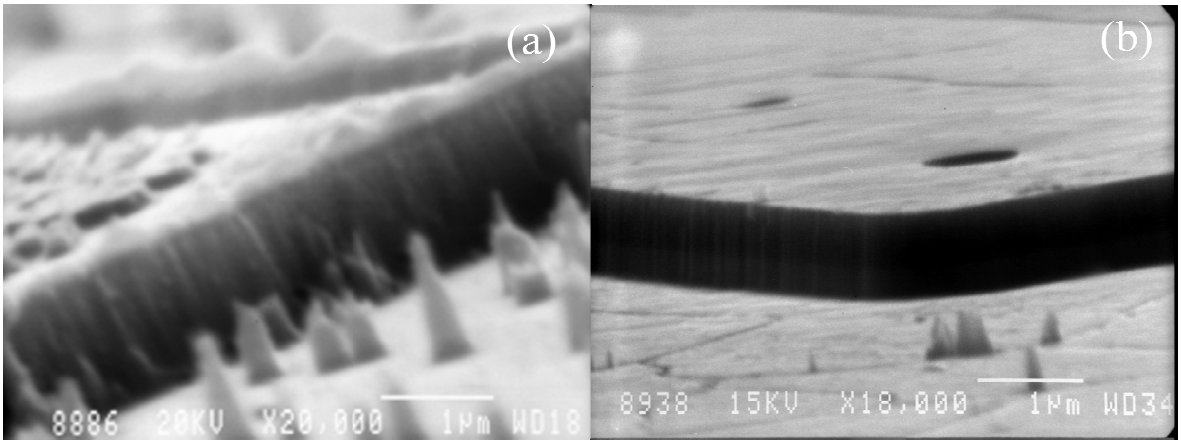


Fig. 4.14 *Results of RIE with optimized set of: 7 sccm BCl_3/1.0 sccm Cl_2, 10 mTorr chamber pressure and dc-bias values of -170 V (a) and -180 V (b). The former resulted in micro-masking effects, while the latter is not introducing additional roughness to the sidewall as compared to the initial PR pattern.*

All the above mentioned experiments were conducted under a constant rf-power of 50 W. With BCl_3/Cl_2 gas ratio equal to 7, pressure around 10 mTorr and rf-power of 50 W, dc-bias spanned from -203 to -246 V. As a reminder (paragraph 2.3.3), dc-bias is indicative of ions kinetic energy and can be affected by all the other RIE parameters, the type of sample to be etched and contamination inside the chamber. Its magnitude during the process, with all other parameters fixed, has a starting value and increases monotonically towards a maximum. Rf-power directly affects dc-bias, i.e. an increase in rf-power, even by 1 Watt, results in dc-bias increase by 3-4 V (absolute values) and vice versa. Therefore, the ability to control dc-bias value was achieved through rf-power reduction throughout the process. **By decreasing the magnitude of dc-bias from -220 V (-218 to -223V) to -180 V (-178 to -182 V), an obvious improvement of facets' roughness was observed, while the slope was not significantly affected.** This can be explained if one considers that the PR etch mask is a polymeric material, which is not totally immune to the kinetic ions. **Therefore, lowering ions kinetic energy leads to smaller PR patterns' profile degradation, improving eventually sidewall roughness.** By further reducing dc-bias magnitude from -180 to -170 and -160 V, spikes appeared on the etched surface, as a result of micro-masking effects. That is, irremovable by-products of etching which remain on the surface and cannot be sputtered away by the low kinetic ions, as can be seen in fig. 4.14 (a) where dc-bias during RIE is set to -170 V. For dc-bias value of -180 V (fig. 4.14 (b)) no micro-masking effects are observed, while sidewall roughness of the resulting mesa is very close to those of the initial PR etch-mask and sidewalls are practically vertical. These are the prerequisites that have been set at the beginning of nitrides RIE experiments.

In conclusion, the optimum set of RIE parameters for nitrides' dry etching is: BCl_3/Cl_2 ratio equal to 7, gas pressure of around 10 mTorr and rf-power such that a constant dc-bias of -180 V is obtained. This set of RIE parameters insures practically vertical and smooth sidewalls of the mesas' facets, provided of course that the PR etch-mask is sufficiently smooth and vertical to start with. The fact that the RIE process developed here does not introduce additional roughness to the mesa sidewalls is confirmed in fig. 4.15, where the remained PR etch-mask has not yet been removed. Both the PR and he GaN layer show very similar sidewall roughness. It should be noted, however, that the above, relatively mild, RIE procedure is characterized by low etch rates of around 12 nm/min for nitrides, while for PR, etch-rate is around 20 nm/min. This issue will be discussed in section 4.4.

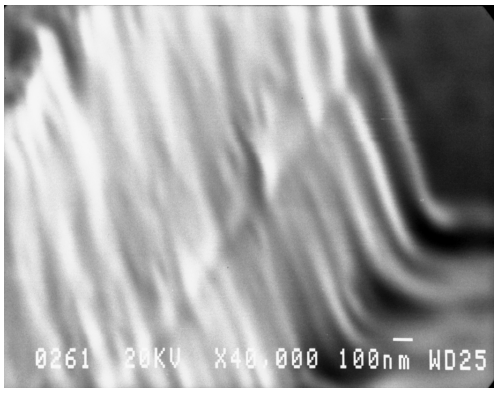


Fig. 4.15 *Mesa and PR etch-mask left on top after the optimized chloride RIE. Roughness and slope are similar in both PR and GaN. The 100 nm roughness is due to old photo-mask exposure.*

Cleaving is an alternative approach of fabricating the cavity of edge-emitting lasers, which in the case of arsenides can yield atomically smooth facets with minimized mirror losses. This is not the case for nitrides however, since lack of thick GaN substrates and heteroepitaxy on non-lattice matched substrates, hinder quality of cleaved surfaces, which are characterized by an observable roughness, as seen in fig. 4.16 where facets of a nitride-based laser structure grown on SiC substrate are shown. With cleaving being a sample- and time-consuming method of fabricating optical cavities, as compared to RIE, comparison of figures 4.14 (b) and 4.16 tip the scales in favour of dry etching as the most cost and time efficient method to fabricate optical cavity of nitride-based edge-emitting lasers, especially if roughness observed in both fig. 4.14 (b) and 4.15 is further reduced. The roughness observed there, can be attributed to photo mask-induced roughness of the initial PR etch-mask pattern, since the photo-mask used to pattern the samples in these figures had been used

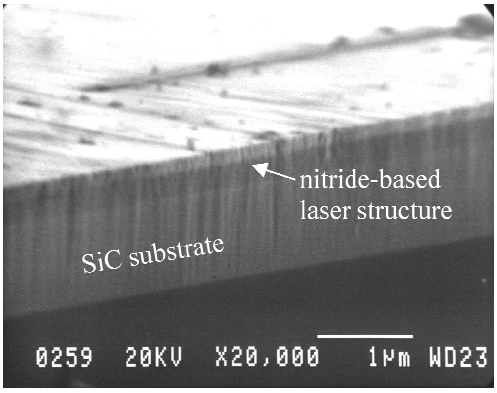


Fig. 4.16 Roughness on cleaved sidewall due to heteroepitaxy on SiC.

for many exposures, while the O_2 RIE process was not employed. The dry etch process being optimized here can yield better quality mesas than those depicted in fig. 4.14 (b) and 4.15, as will be shown in the next section, where PR etch-mask preparation procedure is further optimized.

4.4 Results on RIE-related material damage

The optimized RIE procedure for nitride etching yields etch rates of ~ 12 nm/min, which can be characterized as slow. The mild character of the process originated from restricting dc-bias value ~ -180 Volts, which was necessary in order for the initial PR patterns' profile to remain as intact as possible. Nevertheless, the chlorides RIE process etches PR patterns as well with an etch rate of ~ 20 nm/min, which is greater than that of nitrides. With etch depths usually varying from 0.8 to 1.0 μm for typical optically pumped laser structures, the time needed to etch in such depths should be 70-90 minutes. In the case of an LD, the etch depth, and hence etch duration, can be even larger due to the p-type GaN contact and AlGaN cladding layers needed to complete the electrically pumped laser structure. Consequently, the corresponding thickness reduction of the PR etch-mask after such a long RIE process varies from 1.4 to 1.8 μm. Considering that the tial thickness of the PR patterns ranges from 1.6 to 1.8 μm, it becomes clear that material protection during etching becomes a serious issue. For even longer plasma exposure, the PR patterns are entirely etched, leaving material underneath unprotected. This is the case depicted in fig. 4.17, where samples that have been exposed to chlorides RIE for ~ 120 min are shown. Clearly, terial from the top surface of sa, which is supposed to be protected, is attacked by plasma after complete removal of PR etch mask, with the resulting material damage being readily obtained in the SEM.

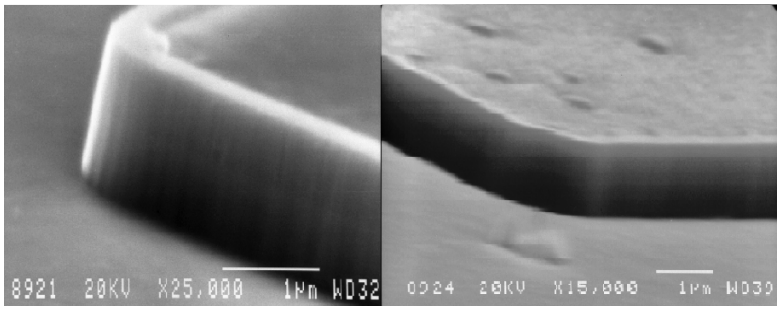


Fig. 4.17 *Mesas after 120 minutes RIE. Top material damaging is observed due to complete PR removal during RIE.*

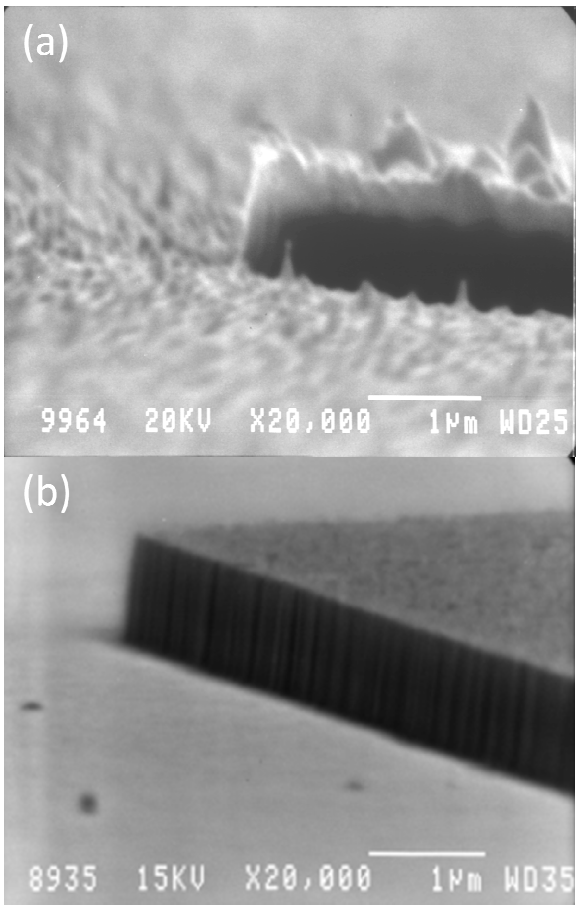


Fig. 4.18 *Mesas after 90 minutes of RIE with (a) and without (b) the 300 nm left-over PR etch-mask. No visible material damaging on the top can be observed.*

The 120 min RIE process is an extreme case however, since the process is continued after the complete PR etch mask removal occurs. The usual chlorides RIE process duration is ~ 90 minutes, which usually results in a mesa depth of ~ 1 μm and left-over PR's thickness of 200-300 nm. Typical mesas for such process duration are shown in fig. 4.18, both before and after the left-over PR's removal by acetone. In fig. 4.18 (a) a left-over PR layer of ~ 300 nm has remained for material protection, while no visible material damage can be detected by SEM, as seen in fig. 4.18 (b). The trenches shown on the mesa's top surface in fig. 4.18 (b) are due to PR remainings, which can be removed by sample immersion in acetone in a hot ultrasonic bath. Material damage however, was ascertained by optical characterization. The etched sample of fig. 4.18 (b) is an optically pumped laser structure, which is consisted of three quaternary InAlGaN quantum wells (QWs), located about 50-100 nm below the top surface, AlGaN cladding layers of various Al concentrations below the QWs for waveguiding and a thick GaN buffer layer on the bottom of the structure, which is grown by MBE on a 2" sapphire substrate. A comparison of PL spectra before and after RIE of the structure described above is shown in fig. 4.19. Note that the laser excitation beam impinged only on the mesa to ensure that light gathered was emitted only from the layers of the mesa. After RIE, the PL peak intensity of the InAlGaN QWs dropped by a factor of 20, while that of the underneath GaN buffer by only a factor of 2. The observed, strong suppression of the InAlGaN QWs PL intensity can be explained by the existence of a large number of non-radiative (NR) centers at these layers, suggesting significant RIE-induced crystal quality degradation. This is supported by the QWs proximity to the mesa's top surface, which makes them vulnerable to plasma ions attack, as opposed to the GaN buffer layer, which is located 700-

800 nm beneath the surface. Point defects, interstitials and/or contamination of the top layers with plasma species result in crystal quality degradation and all of them can be caused by ion penetration in the sample's top layers (50-100 nm) and collisions with the crystal atoms, after passing through the PR pattern. The latter seems to allow ion penetration through its volume, when its thickness is not enough to protect material underneath. Although ions may not be able to reach mesa's top surface at the beginning of the process, when PR's thickness is ≥ 1.5 μm, they are probably able to do that when PR's thickness is decreased below a certain level. This effect is enforced by the relatively slow etch rates of nitrides (<1μm/hr), which impose long exposure times of the PR mask to the chloride-based plasma. Since endurance of PR etch mask cannot be enhanced without degrading its profile, as discussed in paragraph 4.3.1, increasing PR thickness remains the only possibility for its utilization as etch-mask.

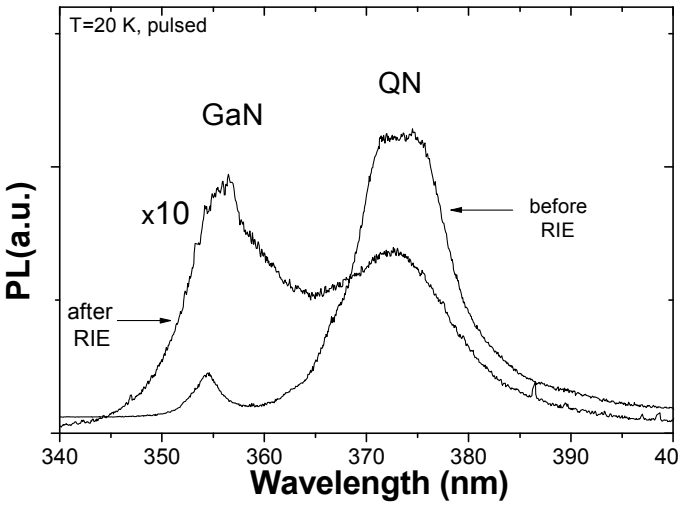


Fig. 4.19 Comparison of PL spectra of an etched sample before and after RIE. The "QN" peak corresponds to three quaternary nitride QWs which are located about 50-100nm below the top surface of the sample.

Finally, after failing to increase the thickness of a single PR layer and before starting to research and optimize the procedure of metal mask for optical cavity formation, the double PR layer solution was examined. This solution includes coating of the sample surface with two PR layers and subsequent pattern formation of controllable sidewall roughness and slope. A major concern though, is that the first (bottom) PR layer has to be subjected in two soft-bake steps before exposure, since for coating of the second PR layer a solid surface is required. Moreover, the double PR layer should behave as a uniform, single layer during the forthcoming exposure and development steps and this might be affected by the double soft-bake of the bottom PR layer. First results, however, indicate that the double PR layer behaves similarly as the single one, which allowed us to take advantage of all the acquired know-how from our previous experiments in order to obtain patterns with desirable sidewall roughness and slope. The thickness of the PR etch mask now is 2.8-3.4 μm after the lithography, depending on spin-coating's conditions and after etching the samples for 90 minutes, there is always a 1.5-2.0 μm photoresist left, as seen in

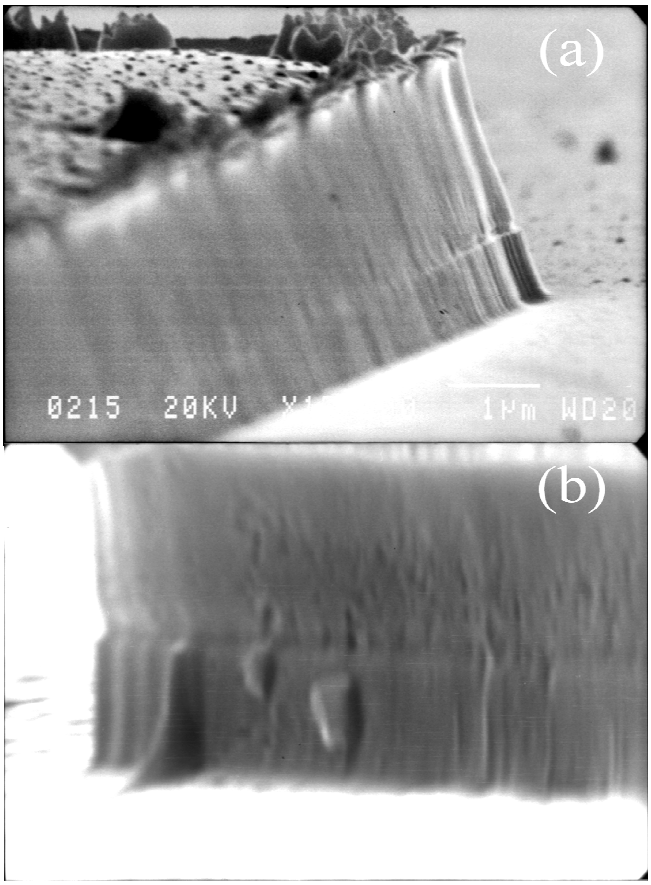


Fig. 4.20 *(a) Etched mesa with the left-over PR layer on top right after 90 minutes of RIE. The mesa's height is ~ 0.8 μm while the left-over PR is ~ 2 μm. The roughness is more intense at the pattern's corners, most probably due to diffraction effects. (b) Apart from local effects sidewall roughness is < 100 nm.*

fig. 4.20 (a). The thickness of the etched nitride is 1 μm. We can also see the roughness of ~ 100 nm, a slope of 90° and the 2.0 μm thick photoresist layer left after the RIE. Another observation is that the optimized RIE process does not introduce additional roughness as compared to the initial PR, in all places except at the corners of the patterns, most probably due to enhancement of unwanted diffraction effects there. Therefore, apart from local effects occurring at the corners of the patterns, as seen in fig. 4.20 (b), the overall sidewall roughness can be even less than 100 nm. Moreover, a comparison of fig. 4.18 (a) and 4.20 (a) indicate that thickness of the left-over PR layer after RIE has been increased by 5 times for the same process duration, while a visual improvement of the left-over PR etch mask morphology can be observed.

The 1.5-2.0 μm of left-over PR mask after RIE should be sufficient to prevent RIE-damage of the laser active region beneath. This is supported by our observation of reduced RIE damage as the thickness of the left-over PR was increased from 0.3 to 0.7 μm. In Fig. 4.21, we show a comparison of PL spectra before and after RIE, as well as the layers of the test structure of the GaN/AlGaN QW sample that was used and was patterned using the two-layer PR procedure. This structure was grown only to investigate RIE damaging, therefore no cladding layers were incorporated in the structure. The nominal thicknesses of the well and barrier layers were confirmed with XRD measurements. After 120 min of etching only 0.7 μm of PR were left. We observed an important decrease in PL intensity of the two closest to the surface QWs (4.5 and 3

nm). However, the PL of the 1.5nm QW, located less than 40nm below the surface, remains practically unchanged, which is a clear improvement compared to the case of Fig. 4.19 where optical degradation of the QWs was much more pronounced. This result is even stronger if we consider that in the PL spectra of Fig. 4.21 cw excitation was used, as opposed to pulsed laser excitation used in Fig. 4.19. Therefore, our results suggest that, with a 0.7 μm of PR left, ion penetration depth and consequent RIE-induced NR centers are confined within the top 40 nm of the structure[2]. Systematic work is presently under development in order to determine the thickness of the left-over PR layer that is necessary to completely protect the material.

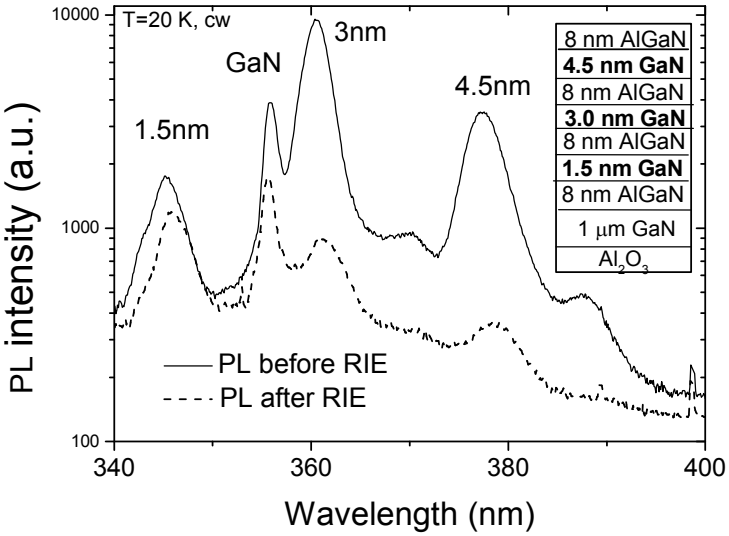


Fig. 4.21 PL spectra comparison before and after RIE of a sample with 3 GaN/ AlGaN QWs of thicknesses 1.5, 3 and 4.5 nm, as shown in the inset. We observe suppression of the PL of the two top QWs relatively to GaN template. The thickness of the left-over PR layer in this RIE process is 0.7 μm.

4.5 Conclusions

In this chapter, we have developed an optimized dry-etching procedure for optical cavity formation on nitrides. Mesas with practically vertical sidewalls of roughness < 100 nm were achieved after combined optimization of etch-mask preparation and RIE process. Sidewall roughness and slope of the final mesas were found to be strongly dependent on the starting PR pattern's sidewall roughness and slope, provided that the chloride-based RIE process is mild

enough as to not introduce any additional sidewall roughness, while the chemical compponent of etching should be suppressed in order for verticality to be the case. Moreover, an oxygen plasma ashing process can further reduce sidewall roughness of the starting PR patterns, which can be important if an old photo-mask is used for PR exposure. This optimized procedure can yield sidewalls of comperable roughness as the one of a cleaved facet of a nitride-based structure on SiC substrate.

Towards sufficient material protection during RIE, chlorobenzene treatment or post-bake of the PR etch-mask patterns have not significantly improved PR endurance under chloride-plasma conditions. Nevertheless, we have developed a two-layer PR approach, with which it is possible to have more than 1.5 μm PR etch-mask left-over after RIE. This PR thickness should be sufficient to completely protect the underneath material from RIE damage.

[1] I.Vurgaftman and J.Singh, Appl. Phys. Lett. 66 (9) (1995) p 105 6

[2] F. G. Kalaitzakis et al., phys. stat. sol. (c) 3, No. 6, 1798–1802 (2006)

CHAPTER 5

Ohmic contacts to p-type GaN

5.1 Theoretical background

The importance of forming good quality ohmic contacts is self-evident since they provide the means for a device's connection to the outside world. Ohmic contacts, as opposed to the rectifying ones, are defined as the contacts which, when formed to a semiconductor permit equal current flow in both directions, regardless of the bias' polarity. Furthermore, the voltage drop introduced at the contacts should be small compared to that occurring to the rest of the device, with this voltage drop connected to the contact resistance, which should be low in order for the contact to be characterized as of good quality. Optoelectronic devices are somehow more sensitive to the quality of ohmic contacts, with LDs being the most extreme case as lasing might not occur at all for high contact resistances. Since these devices, as well as the LEDs, usually are based on a p-n or p-i-n structure, realization of low resistance ohmic contacts to both n- and p-type layers is essential. III-Nitrides are direct band gap semiconductors with optoelectronics being one their most important application field. The short emission wavelengths that characterize the nitride based emitting devices, makes them important applicants for potential use in a variety of applications,

like dense optical data storage, white lighting, detectors and many others. A main issue in obtaining optoelectronic devices of practical use, emitting in the spectral region of UV (UV-LEDs, UV-LDs), is the ohmic contacts to p-type GaN. With internal polarization fields reducing emission efficiency of nitride-based optoelectronic devices, especially for wavelengths below 380 nm, the voltage drop and heat originated in the conventional kΩ range p-type ohmic contacts, makes the realization of reliable and low-operating voltage devices a very difficult task. While obtaining good quality ohmic contacts to n-type GaN has been satisfyingly resolved with use of the Ti/Al metal scheme, achieving good quality ohmic contacts to p-GaN is a real challenge from the fabrication point of view, as will become apparent in section 5.2.

5.1.1 Schottky-Mott theory for Metal/Semiconductor contacts

Ideally, a metal ohmic contact is formed to a p-type semiconductor when the metal has a nearly equal or larger work function than that of the semiconductor. If this is the case then no potential barrier for holes is built up at the metal/semiconductor (M/S) interface after contact, as can be seen in the band diagram of fig. 5.1. The small upward band bending, with respect to the bulk levels, observed in the near-interface region when the metal and semiconductor are brought into contact, permits free hole transport from the metal to the semiconductor and vice versa if biases of both polarities are applied, resulting in a linear relationship between current and bias applied (ohmic contact). On the other hand, in the case of a M/S contact of a metal having lower work

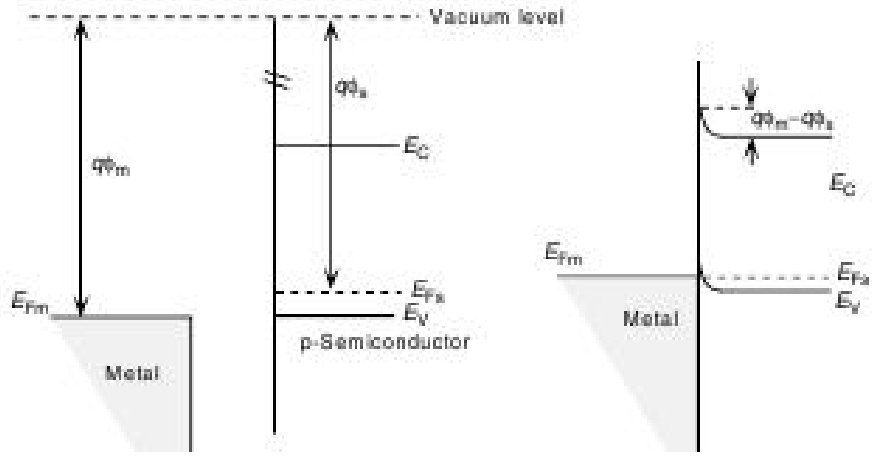


Fig. 5.1 *Band diagram of an ohmic M/S contact for a p-type semiconductor (after*

function than that of the semiconductor (p-type case), the semiconductor bands are bended in an opposite direction, as shown in the band diagram of fig. 5.2, which schematically describes a Schottky contact to a p-type semiconductor[1]. The build-in potential barrier formed at the interface of such contacts, also called the Schottky barrier (SB), is strongly related to the work function difference between the semiconductor and the metal as measured from the vacuum level. The

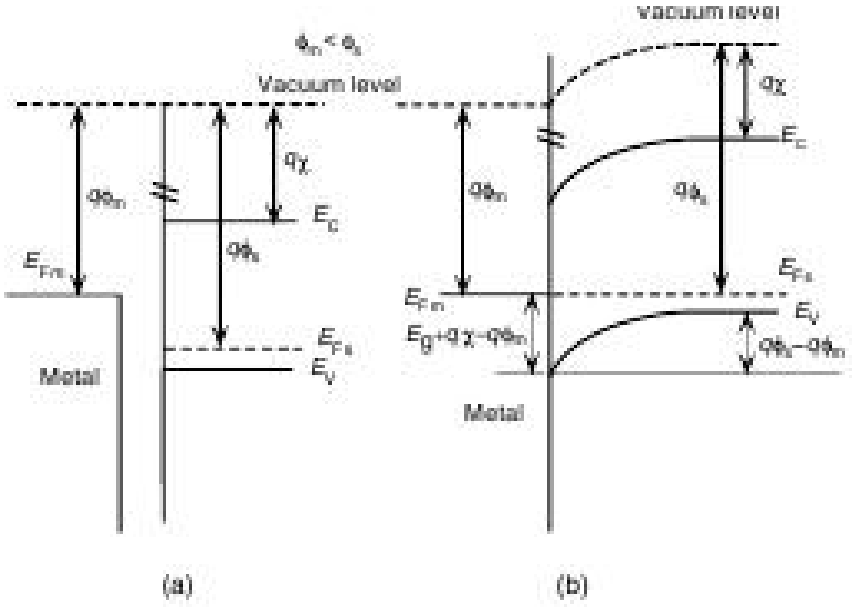


Fig. 5.2 *Band diagram of a Schottky M/S contact for a p-type semiconductor. The build-in potential barrier is shown (after [1]).*

downward band bending observed in fig. 5.2 represents a region depleted from mobile holes, while a space charge caused by the acceptor atoms exists at the whole width of this region. Thus, in order for current to be obtained through such contacts, holes should be able to surpass the build-in potential barrier, with the height of the barrier (SB Height or just SBH) depending on the work function of the metal used and its width on the doping levels of the semiconductor. Consequently, Schottky contacts behave differently under forward and reverse bias conditions; under forward bias (positive potential to semiconductor with metal grounded) barrier's height and width decreases, allowing carriers' transport through the contact, with current generally depending exponentially on the applied voltage. Under reverse bias conditions on the other hand, the build-in potential barrier becomes even larger, both in height and width, allowing for a very small leakage current to be obtained. All the above lead to the rectifying character of Schottky contacts, which have a similar behavior as that of p-n$^+$ junctions, where the "+" sign indicates an overdoped semiconductor as an approach to the metal, since the width of depletion region in each side is in-

versely proportional to the doping concentration, as a consequence of Poisson's equation, and no depletion region practically exists in the metal side.

In summarizing the above and towards focusing on the p-GaN case, ohmic contacts to this material can be theoretically obtained if a metal of a work function equal (Schottky-Mott limit) or higher than that of p-GaN comes in contact with it. However, one cannot just order for work function matching and especially in wide band-gap semiconductors, like p-GaN, things are even worse; p-GaN has a work function of about 7.5 eV, while the metal with the highest work function is Pt which has a work function of about 5.6 eV when polycrystalline[2]. Note that e-beam thermal evaporation technique utilized for metal deposition yields polycrystalline metal films, as discussed in 2.3.4. Therefore, p-GaN/metal contacts are usually Schottky-like, with a potential barrier always present at the M/S interface, in turn inhibiting hole transport.

Holes can pass either through or over the interface potential barrier leading to three distinct transport mechanisms through Schottky contacts: field emission, thermionic-field emission and thermionic emission. In **field emission**, barrier's width is thin enough to permit direct hole tunneling through it and this is the case for highly doped semiconductors ($N_A \geq 10^{18}$ cm^{-3}), where narrow depletion regions are formed. For moderately doped semiconductors ($10^{17} \leq N_A \leq 10^{18}$ cm^{-3}), holes at the valence band maximum cannot directly tunnel through the barrier, instead they need some excess energy to be able to tunnel through a reduced barrier width, describing in this way the **thermionic-field emission** mechanism. When holes gain sufficient energy to be able to pass over the barrier, i.e. energy greater than the barrier height, the **thermionic emission** mechanism takes place. This mechanism permits current flow even for poorly doped semiconductors ($N_A < 10^{17}$ cm^{-3}) and requires sufficient energy gain from the bias applied. A more detailed treatment of metal/semiconductor contacts, including electron-hole generation-recombination and leakage current mechanisms, needed to complete the picture, can be found in many textbooks. However, an effect worth mentioning that should be taken into account to complete the above ideal description of the M/S contact is the surface dipole effect, which originates from charge neutrality requirement at the surface/near-surface region in the semiconductor side. As a consequence, a correction of the potential barrier's shape at the metal-semiconductor interface is introduced, which as shown in fig. 5.3, causes SBH reduction by an

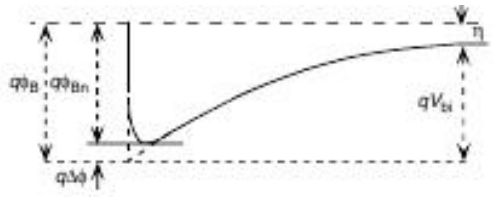


Fig. 5.3 *Image force lowering of SB by an amount qΔφ (after [1]).*

amount $q\Delta\varphi$, which is called the image force lowering. Apart from height, the shape and position of the barrier's maximum is also affected; under equilibrium, the maximum is not located exactly at the interface but has rather moved inside the semiconductor, while its position and height changes with the applied bias. Therefore, when surface dipole effect is considered, the potential barrier that holes should actually surpass (fig. 5.3) is slightly lower and thinner as is the one depicted in fig. 5.2 (b), favoring hole transport through the interface in all cases. It has to be noted here, that thermionic-field emission and tunneling (field emission) can turn a Schottky into an ohmic contact if the interface barrier becomes sufficiently low and/or narrow. Consequently, the Schottky or ohmic nature of M/S contacts in the ideal description for a given semiconductor depends on the choice of metal, through its work function, and on doping levels in the semiconductor, which affects SB thickness through the depletion region width and the space charge existing in this region.

5.1.2 Surface states and surface sites

The above ideal M/S contact description, first introduced by Schottky and followed by Mott, can satisfyingly predict or, to be more exact, can give the right trend of the relation between the metal work function and the height of barrier formed at M/S contacts only in the case of abrupt interfaces. An interface is abrupt when the metal and semiconductor layers are in contact but are apart by a constant distance $\delta \geq 0.5$ Å throughout the whole area of the contact. If this is the case, each M atom at the interface is bonded to both M and S atoms, with the M-S bond being as loose as possible and weaker than the M-M one[3]. The metal layer then adheres to the semiconductor with Van Der Waals type of interactions, which at the same time decreases the interface energy by relaxation of strain induced by lattice mismatch during deposition. An abrupt interface ensures that a well defined border line exists between metal and semiconductor bulk properties in a direction normal to the interface, with thickness of this border (δ) being sufficiently large for metal-like and semiconductor-like wavefunctions of electrons and holes not to overlap. However, the Schottky-Mott theory failed to describe real M/S contacts since the beginning and is still very difficult to be experimentally demonstrated. The reason for these is that neither Schottky nor Mott included surface and/or interface properties in the M/S contact description.

A more realistic description of the M/S contact should inevitably incorporate surface properties, since an interface is actually comprised of two surfaces. In the case of ohmic contacts, where "free" carrier transport through the M/S interface is the objective, surface properties can be crucial in determining both SBH and the resulting electrical behavior of the contact. Especially in semiconductor surfaces, crystal symmetry interruption at the semiconductor/vacuum interface reveals the existence of intrinsic bandgap states, with their corresponding wavefunctions being localized at the surface[4]. The energy levels of these states lie inside the gap, while their energy distribution is not constant in this energy regime; it rather exhibits a U-shape relation, with the minimum of the density of states corresponding to a characteristic energy level, called the branch point energy level W_{bp}. These intrinsic bandgap states are called **surface states** and can have a donor- or an acceptor-like character inside the bandgap, depending on whether their branch point energy level is below or above the Fermi level respectively in thermal equilibrium. As treated by Tight-Binding-Approximation methods, these surface states are originated by the unoccupied orbitals of surface S atoms. Such unoccupied orbitals, one per surface atom, are called **dangling bonds** and as is easily understood need to compensate. In elemental semiconductors (Si, Ge), the related energy levels (W_{bp}) of dangling bonds are resonant with valence band states. This is the case for the anion dangling bonds in compound semiconductors (GaAs, GaP, GaN, CdTe), while the cation dangling bonds levels are above the valence band maximum (VBM) of the surface. Surface energy minimization includes charge transfer from the cation to the anion related levels, a process accompanied by re-hybridization of surface atomic orbitals and re-arrangement of surface atoms, an effect called **surface reconstruction**. This effect includes deformations in bonds of surface atoms, affecting both distances and arrangement of surface atoms, as well as of atoms in the first 1-2 or more atomic layers beneath the surface. Surface reconstruction is always present at bare surfaces of both elemental and compound semiconductors as a means for the surface to lower its energy.

With surface states in the picture, the semiconductor surface now becomes active, since it can participate through dangling bonds in chemical interactions between S atoms and foreign species. In reality, as soon as a freshly grown crystal surface is exposed to the atmosphere, the uncompensated dangling bonds will attract these species that are able to lower surface energy, with the appropriate charge exchange between S atoms and these species included in the procedure. The adsorbed species will then induce surface states with each species corresponding to a different W_{bp} energy level. In the case of monovalent adsorbed atoms (adatoms), these levels can

be estimated by incorporating the surface molecule approach in the description, i.e. by treating the adatom-S atom system as a molecule existing at the interface. The adatom-induced surface states energy levels will then correspond to the molecule's energy levels, which are obtained by linear combination of the separate atomic orbitals (LCAO). The phenomenological atom electronegativity difference concept applied in normal molecules for charge displacement and molecular polarization estimation can be also applied to surface molecules to predict charge transfer between the adatom and the semiconductor. Charge transfer will be automatically accompanied by surface reconstruction, while it results in dipoles formation at the interface. Exactly the way dangling bonds induce surface states with characteristic energy distribution and W_{bp}, any surface irregularity can also induce states inside the bandgap. Crystallographic steps, defects, impurities, inversion domains or, on the other hand, adsorbed species, can all induce states inside the gap, with states of each origin differing from the others in their energy distribution and W_{bp}. All these surface states' origins are also called **active sites** or **surface sites**, since the above described surface activity is promoted via such sites.

As expected by the above discussion, the deposited metal layer of a M/S contact also induces surface states, the so-called **Metal-induced Gap States (MiGS)**, in the same way adatoms do. The donor- or acceptor-like character of the MiGS also depends on the position of the corresponding W_{bp} relative to the Fermi level and, if they coincide, no charge transfer from the semiconductor to the metal or vice versa occurs at all. This is the reason why the W_{bp} level of MiGS is also called charge neutrality level (CNL) of the MiGS. In all other cases there will be a charge transfer, which roughly follows the electronegativity concept and it will force the surface to reconstruct under the new conditions. The same arguments apply for surface states induced by all other kinds of active sites, with each one characterized by a specific CNL. Regardless of the origin of surface states, there are always dipoles formed at the interface due to charge transfer, even if it is only a small fraction of an electron charge per active site. Depending on the electronegativity difference between metal/adatom and the semiconductor, the molecular dipoles formed at the interface will tend to increase or decrease the SB formed.

In all the above analysis, sparsely dispersed adatoms on the semiconductor surface are considered. In case of monolayer coverage, the adatom-adatom interactions should be incorporated in the description, which can lead to two-dimensional energy bands of adatom-induced states and broadening of the corresponding W_{bp} from a sharp energy level to a zone inside the gap. However the main considerations of charge transfer and dipoles' formation at the interface

also apply for monolayer coverage. Moreover, in real M/S contacts one can find different kinds of species at the interface, which have been adsorbed on the semiconductor surface before the metal atoms come in contact with it during deposition. Such species can be molecules from the atmosphere or ions/radicals from surface cleaning process and, of course, contamination from lithography or any other process that have preceded metal deposition. As mentioned, these species will attach to the surface via active sites, which in semiconductors like GaN can have a dense area distribution. The forthcoming metal atoms will then start to attach on either these species or on surface active sites and, depending on the deposition conditions (substrate temperature, deposition rate, vacuum level) can grow to a film through three discrete growth modes. A detailed discussion about these growth modes is out of the scopes of this work, although in a first approximation, two-dimensional, layer-by-layer growth rather promotes formation of abrupt M/S interfaces than epitaxially grown metal layers. The latter would be favorable for carrier transport through a M/S interface which is the objective when forming ohmic contacts. On the other hand, if surface sites are compensated by specific species, like H, H_2O or OH^- groups, metal atoms cannot easily interact with active sites anymore, which can also result in abrupt M/S contacts[5]. Such a contact interface is depicted in the cross-section TEM image shown in fig. 5.4 (b). This interface was formed when Ni is deposited on AlGaN surface, which have been subjected to a multi-step pre-deposition surface treatment, with RIE and immersion in KOH solution being the last two. The resulting Schottky diode had an ideality factor $\eta = 1.14$, as opposed to the 6.81 of the one corresponding to the interface depicted in fig.5.4 (a), which has been subjected to boiling aqua regia treatment as the last step. Although AlGaN crystal used in this study was N face (it can be partly wet etched as opposed to Ga face nitrides), it is important to stress that the abruptness of the M/S interface can have a major effect on contact's electrical behavior, depending on whether active sites are passivated or not. The above results

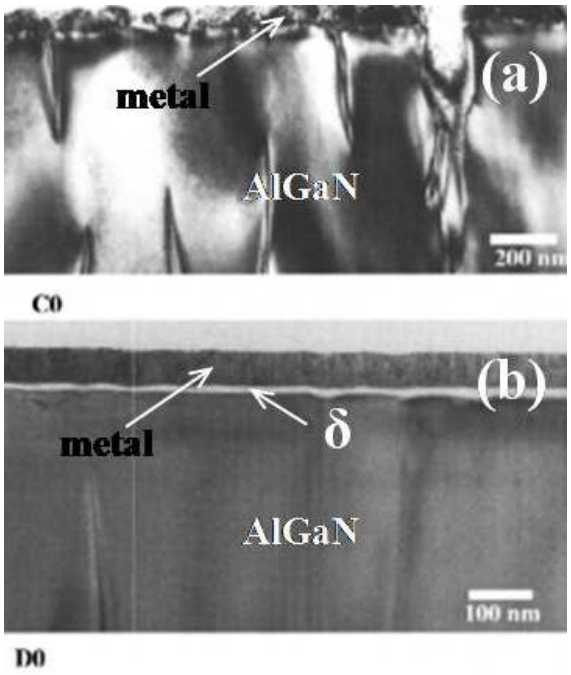


Fig. 5.4 *Ni/AlGaN interfaces after boiling aqua regia (a) and KOH (b)surface treatment. A well defined interface is observed in (b), typical of an abrupt M/S interface as defined here.*

also stress the importance of pre-deposition surface treatment, which will be also confirmed by the results of the present study, as will be discussed below.

The fact that most of the above discussion concerns Schottky instead of ohmic contacts should not be surprising, since contacts to p-type GaN is the issue. As discussed above, the high work function of p-GaN and lack of such high work function metals, leads to the eager formation of large SBs at the M/S interface, hindering the ohmic behaviour of the contacts. On the other hand, p-GaN surface might prove to play a role in the above disadvantageous predictions of Schottky-Mott theory concerning the nature of M/p-GaN interfaces. Moreover, there are established technological solutions for reducing height and width of the interface barrier in metal/semiconductor contacts. Such solutions usually involve deposition of a suitable metal or metal stack, which upon annealing can promote alloying of the deposited metals with the semiconductor's atoms, which can lead to formation of either an overdoped near-surface region or conducting phases at the interface[6]. In this way, the build-in potential is weakened or can even be eliminated leading in enhanced carrier tunneling and ohmic behavior. Towards this direction, removal of any isolating layers, like native oxide or contamination, from the semiconductor's surface prior to metal deposition can enhance contact conductivity. Surface effects and the way they affect ohmic contact formation will be discussed in details when the results on as deposited contacts to p-GaN are presented. Prior, a short introduction in p-GaN material properties is attempted and the study concerning the standard oxidized Ni/Au contact scheme are presented. This chapter ends with the results on a low resistance, as deposited metal contact scheme to p-GaN and its possible formation mechanism.

5.2 The p-GaN case

Despite the intensive research towards the realization of low resistance ohmic contacts to p-type GaN for 15 years, good, reliable and wide-used solutions have not been given yet, except the oxidized Ni/Au scheme and the less used, as deposited Pd/Au one, which still suffer from contact resistances in the kΩ range, while their thermal and time stability are under question. As mentioned in the previous paragraph, there is always formation of SB at the metal/p-GaN inter-

face due to non existence of such high work function metal (7.5 eV) to meet the Schottky-Mott limit of work function matching for fortuitous ohmic contact formation. Another inherent issue of wide bandgap semiconductors is the fact that they suffer from large hole effective mass and low hole mobility, and p-GaN is not an exception since the typically obtained hole mobility values in this material are ~ 10 $cm^2V^{-1}s^{-1}$.

The well established p-type dopand of GaN is magnesium (Mg), with the majority of commercially available material, as well as the most studied, being the MOCVD (Metal Organic Chemical Vapor Deposition) grown epilayers, which are usually grown on 2" c-axis GaN/Al_2O_3 substrates. In general, p-type doping of GaN has always been problematic, since magnesium, which was the only element of group-II of the periodic table that was able to be a p-type dopand for GaN, has low solubility in the GaN matrix leading to a maximum in Mg incorporation, with these maximum [Mg] values being around 10^{20}-10^{21} cm^{-3}. If higher carrier concentration levels are tried to be achieved, crystal and surface quality of p-GaN epilayers will be affected, in turn degrading their electronic transport properties[7, 8]. Actually, the 10^{20}-10^{21} cm^{-3} values of [Mg] are not so low if it weren't for the Mg-H and/or Mg-N-H complexes, which are always present in the MOCVD grown material due to the Mg-source used in this method, which in turn de-activate (passivate) the Mg dopand atoms[9,10]. The latter is the well accepted explanation for the inability to obtain p-type conductivity in the as-grown MOCVD GaN: Mg epilayers, which is finally obtained if the samples are irradiated by low energy electrons or annealed at elevated temperatures. These were the methods initially utilized to activate (de-passivate) the Mg dopands and are still used, since in order for p-type conductivity to be obtained, a post-growth thermal treatment step is mandatory. Nevertheless, the best reported post-growth treatments result in activating only ~ 1% of the Mg atoms, restraining hole concentration values (p) at ~ 10^{18} cm^{-3}, with epilayers of p values ~ $5x10^{17}$ cm^{-3} being the best compromise in hole mobility, layer resistivity and crystal quality. Therefore, the solution of highly doping GaN with Mg as a way to reduce SB thickness of metal/p-GaN interfaces is not an option. In all the above it should be added the ~ 130 meV activation energy of the Mg dopands, which is rather high as compared to the 26 meV of carrier's thermal energy at room temperature. Considering the high hole activation energy mentioned above, Mg cannot be characterized as a shallow acceptor of GaN and this fact makes the situation even worse.

Intense efforts for a new p-type dopand of p-GaN to be found were not very successful, especially in the most commonly used c-axis grown epilayers, since Be doping cannot yield p-

type conductivity in a systematic and reproducible way. On the other hand, the MBE (Molecular Beam Epitaxy) grown GaN: Mg material is expected to be free of Mg-H and/or Mg-N-H complexes due to the hydrogen-free Mg source used in this method and this fact is expected to enhance both bulk electrical properties, as well as conductivity through M/S contacts. Unfortunately, MBE p-GaN was obtained later than the MOCVD one, which for many years was the only p-type material choice and has gathered all the attention. As will be discussed later, our experimental results on ohmic contacts to MBE p-GaN, as well as results from surface analysis, also indicate the superiority of the MBE p-GaN material, as compared to its MOCVD counterpart.

Apart from the above inherent issues, it is rather difficult to form an overdoped surface/ near-surface region under the contact area through metal alloying with the semiconductor's atoms at moderate annealing temperatures (< 600ºC). At higher temperatures, thermal dissociation of Ga-N bonds and subsequent removal of nitrogen from the surface/ near-surface region of the crystal begins to take place, resulting in compensation of holes due to the donor-like nature of N vacancies. Therefore, the well known methods for ohmic contact formation used in other compound semiconductors (GaAs, SiC, ZnTe, n-GaN)[11] are also not applicable in the p-GaN case. Moreover, a more realistic approach should take into account a thin native oxide or adsorbed O layer on the semiconductor surface, which further enhances the rectifying behavior of the contact. Especially in the case of MOCVD GaN: Mg, the possibility that a native oxide layer is formed on the surface of the semiconductor is strongly increased due to the above mentioned relatively high temperature annealing process for acceptor's activation. In addition, this thermal process results in p-GaN surfaces richer in Ga than in N, compensating in this way the surface/near surface region.

From all the above it should have become clear the peculiarity of the p-GaN material case, especially the MOCVD grown one, which is the material mainly studied in this work. Forming low resistance and reliable ohmic contacts to that material is a very challenging task and ideally there should be a close interaction between researchers in the growth and processing fields in order for good results to be obtained. Towards this direction, uniformity along wafer and detailed knowledge of growth conditions can be very helpful in explaining the results on M/p-GaN contacts. The latter was not always feasible in our case, since most of the experiments were performed on purchased samples, while the lateral non-uniformity of the epilayer properties was a major issue throughout this work. For that reason, special care was given in the preparation of samples as will be discussed later, while many experiments were repeated thoroughly when con-

clusions on the impact of a process were to be formed. In the rest of this chapter, the results of the experimental work concerning ohmic contact formation to p-GaN will be presented, starting from the standard oxidized Ni/Au scheme and continuing with as the deposited contacts, i.e. metal contacts without post-deposition thermal treatment. Finally, photoemission spectroscopy was employed to characterize bare p-GaN surfaces, as well as Cr/p-GaN interfaces.

5.3 Oxidized Ni/Au contacts

Considering the special features of p-GaN mentioned in the previous paragraph, it is not surprising that an oxidized metal scheme, the oxidized Ni/Au scheme, is the well-established contact to p-GaN. It is the first case that a compound, as well as an elemental semiconductor, uses an oxidized metal as electrical contact. During annealing of this contact at ~ 500ºC in air or O_2 ambient, a combination of processes take place and are responsible for ohmic contact formation[12, 13, 14]. Firstly, the p-GaN sample exposure to O_2 during annealing results in H removal from the surface/ near surface region, further de-passivating Mg-H complexes, leading in an overdoped region underneath contact. The role of Ni in this process is literally catalytic, since Ni mediates for the reaction between H and O_2 and the subsequent desorption of formed H_2O molecules from the p-GaN layers' surface. This result is supported by other works, which performed the activation annealing process on Ni covered MOCVD p-GaN epilayers at ~ 500ºC in air and showed lower layer resistivity and higher hole concentration as compared to the established ~ 750ºC activation annealing in vacuum or N_2 ambient. At the same time, oxidation of the contact takes place and by oxidizing the Ni/Au contact, Ni is transformed into NiO[15], which is considered to be

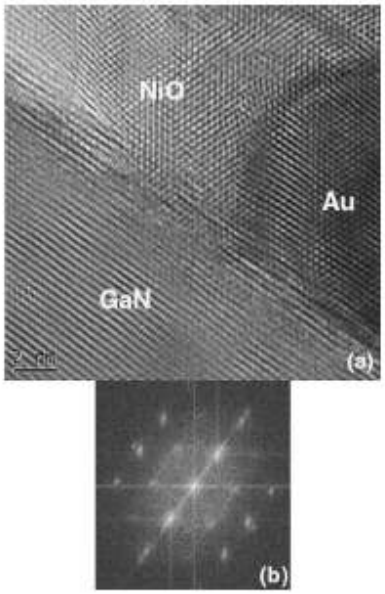


FIG. 3. (a) High-resolution TEM cross section of Au/GaN($10\bar{1}0$) showing epitaxial growth of Au by domain matching epitaxy with a 30° or a 90° rotation) in the GaN basal (0001) plane, where Au is acting as a template for NiO growth. The epitaxial relationships for Au/GaN are [111]Au// [0001]GaN; $[1\bar{1}2]$Au// $[2\bar{1}\bar{1}0]$GaN. NiO grows on Au with a lattice matching epitaxy. (b) Corresponding FT diffraction pattern confirming the above epitaxial relationship for Au: (110) plane of Au matching with ($10\bar{1}0$) plane of GaN in diffraction.

Fig. 5.5 *High-resolution TEM image of p-GaN/Ni/Au after oxidation. Au clustering in NiO's volume and in contact with p-GaN ensures paths for carrier transport (after [14]).*

a p-type semiconductor, while Au diffuses through NiO to form clusters which are randomly situated in its volume, in contact with the semiconductor surface as shown in fig. 5.5. The ohmic behavior finally obtained can also be related to the fact that Ni and Au are both high work function metals, and the fact that there is an intimate contact between these metals and the overdoped p-GaN region beneath them. Furthermore, by transforming Ni to NiO an intermediate semiconducting layer is introduced, which reduces SB height and actual thickness, giving in turn ohmic characteristics to the contact. Qiao et al reported that oxidized p-GaN/Ni or p-GaN/Au contacts alone do not have ohmic behavior[16]. Therefore it is the combination of all the above processes taking place during oxidation of the Ni/Au system that is responsible for the formation of ohmic contacts to p-GaN.

In the rest of this section, the experimental results on the oxidized p-GaN/Ni/Au system will be presented. These experiments aimed at optimizing the process flow of oxidized Ni/Au contact formation, both for reproducing the reported results, as well as having a reference for comparison with other contacts. All the experiments in this study were conducted on the same MOCVD p-GaN wafer, with all the samples being ~ 7x7 mm^2. This sample size was selected to fulfill three requirements: a) multiple samples can be obtained from the central area of the same wafer, necessary when comparing the impact of different processes, b) ensures that each sample contains at least 4 TLM patterns for result verification and c) minimum of sample handling during processing. Fulfilling these requirements ensures the extraction of safe conclusions within a reasonable experimental error, while especially requirement (b) favors observation of a sample's typical contact behavior and extraction of its typical I-V curves for each TLM spacing. The latter can be proved very useful in electrical characterization of contacts, since the typically observed behavior in some wafers was that contact resistance values for the different TLM spacings do not follow the linear relationship of R_i vs. d_i, where d_i is the distance of the ith and the (i+1)th metal pads of the TLM pattern and R_i is the corresponding ohmic resistance, which made the realization of a TLM graph, with more than 5 points, not the usual case. Moreover, in order for reliable ρ_c values to be extracted, the sheet resistance of the material has to be determined in advance and to be incorporated in the TLM graph results through the slope of the straight line. Slope determines both directly and indirectly the experimental ρ_c value through the graph's Y- intercept, which affects the transfer length L_T, as mentioned in paragraph 3.2.2. It is in the author's belief that the comparison of typical I-V curves would be more useful towards quest of a low resistance contact

to p-GaN and this is the case for the rest of this chapter. Nevertheless, wherever a TLM graph extraction is possible, the specific contact resistance values will be extracted and presented.

The MOCVD wafer used, was a commercial TDI p-GaN wafer (TDI 11OK29-2), having a nominal hole concentration of about $8x10^{17}$ cm^{-3}. Ni and Au films were deposited with the e-beam evaporator (Temescal BJD 1700) available in MRG, with pre-deposition chamber pressure being ~ $5x10^{-7}$ Torr in all cases. Since linear-TLM was employed for the electrical characterization of contacts, mesas were formed on the samples' surfaces by utilizing the optimized chloride-

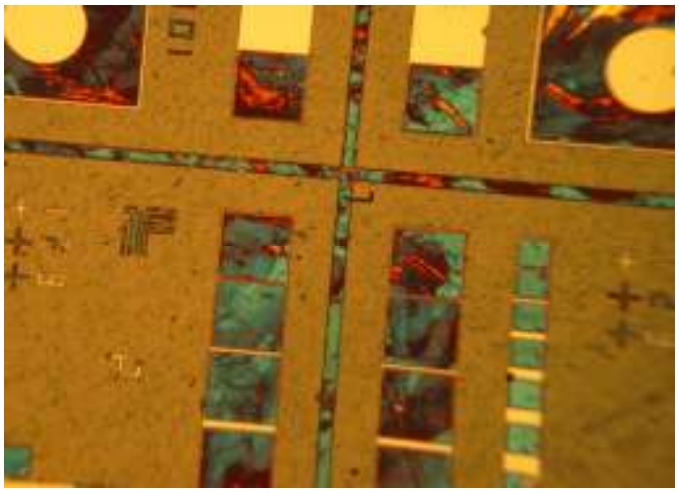


Fig.5.6 *Optical microscope image of oxidized Ni/Au contacts forming linear TLM patterns.*

based RIE process (see Chapter 4) using a SiO_2 etch mask due to its enhanced endurance in chlorides, necessary not to affect the p-GaN surface during the RIE process of the deep (~ 4 μm) mesas formed. Patterning of the semiconductor's surface was performed by the lift-off technique and AZ 5214 photoresist, while samples were immersed in various acid solutions for 60'' prior to metal deposition. This pre-deposition surface treatment step was included in the procedure for removing any native oxide formed during Mg activation annealing and/or by contact with air, since acids can be efficient in native oxide removal from the GaN surface. Contact annealing processes were performed in the Rapid Thermal Annealing (RTA) system of Jipelec, with N_2, forming gas (95% N_2 + 5% H), air or vacuum being the choices for the annealing ambient. For these experiments, nitrogen, air and vacuum were chosen as the annealing ambient, while forming gas was avoided due to the increased possibility of extra H incorporation inside the p-GaN epilayers, which might de-activate more Mg acceptor atoms. A microscope image of typical TLM patterns formed on the surfaces of p-GaN samples is shown in fig. 5.6.

5.3.1 Annealing experiments

First, the role of annealing ambient had to be explored. For this reason 5 nm Ni/5 nm Au films were deposited on three samples, which were subsequently subjected to an RTA process at 500°C in N_2, vacuum and air ambient. For this study, immersion in a 32% HCl solution prior to metal deposition was employed. The corresponding I-V curves of the thermally treated for 5 minutes contacts and the as-deposited ones are shown in figure 5.7, where the rectifying behavior of the as-deposited contacts, as well as of the contacts annealed in N_2 and vacuum can be clearly seen. This behavior is indicative of the SB formed at the p-GaN/Ni interface upon metal deposition (as deposited case), which is further enhanced upon heat treatment, as can be seen in the N_2 and vacuum annealed cases, with this SB enhancement most probably being related to non-conducting phase formation at the interface and/or N loss from surface/near-surface region of p-GaN, since the N_2 case is slightly better than the vacuum one. The only case that yielded a linear

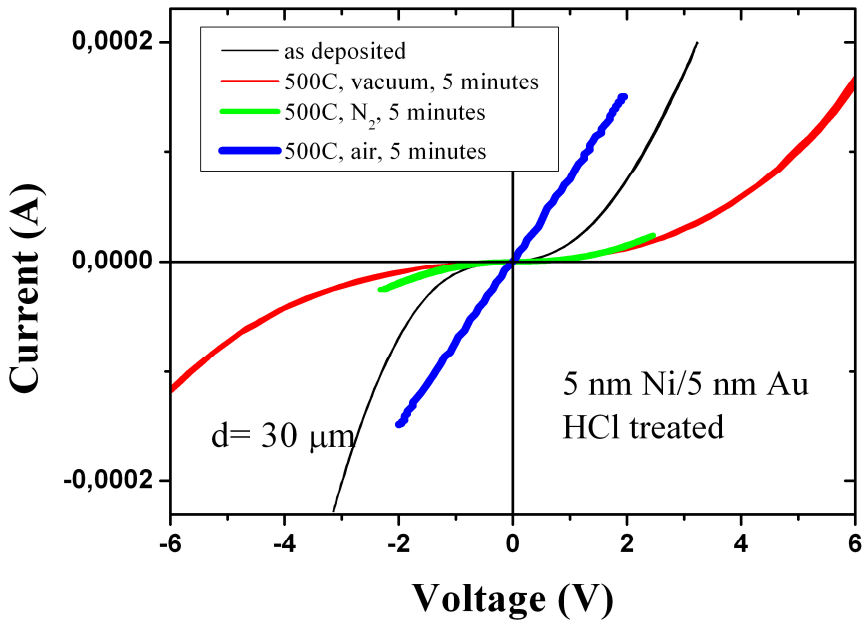


Fig.5.7 *I-V curves for different annealing ambients. The contacts in all cases are rectifying except the air annealed one.*

current-voltage curve is the air-annealed sample with this result indicating that, the interface barrier is decreased when oxidizing the p-GaN/Ni/Au contact, leading finally to the ohmic behavior

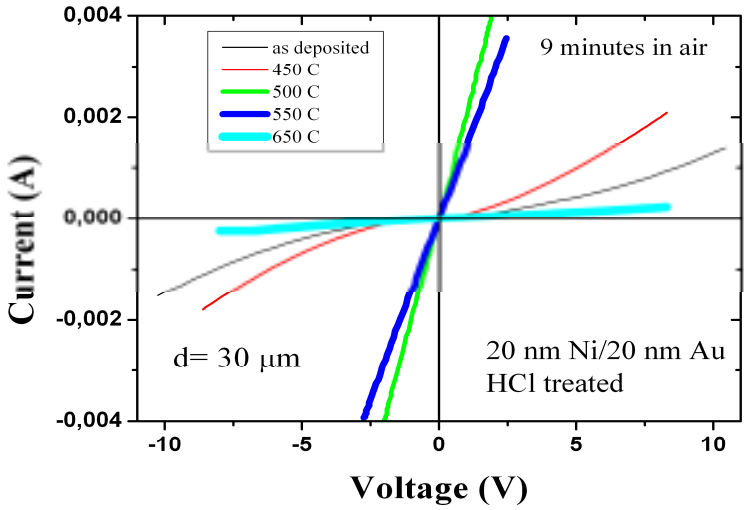


Fig.5.8 *Typical I-V curves for air annealed Ni/Au contacts at different temperatures.*

obtained in fig. 5.7. Nevertheless, both resistance and specific contact resistance values are still high ($\sim 10^{-1}$ Ω cm^2) for the air annealed sample. One reason for this could be the very thin 5nm/5nm metal layers of the Ni/Au films, which also proved to be very sensitive to probe contacting during electrical characterization. Thus, based on the bibliography and after preliminary tests, the metal thicknesses for the rest of this study are set to 20 nm Ni/20 nm Au.

In order to optimize the oxidation procedure, a series of annealing processes at various temperatures was performed. All the RTAs where done in air ambient for 9 minutes (gave the best results as discussed below) and the temperature varied from 450°C to 650°C. As can be seen in fig. 5.8, annealing at 450°C and 600-650°C did not give ohmic behavior to the Ni/Au contacts. The best results were obtained for annealing at 500-550°C, whereas ohmic contacts with resistance values < 0.5 kΩ were obtained. These are amongst the lowest reported ones for comparable contact size and TLM spacing. Nevertheless, a duration study of the 500°C annealing in air followed and the results are shown in fig. 5.9. For 20 nm Ni/20 nm Au, an-

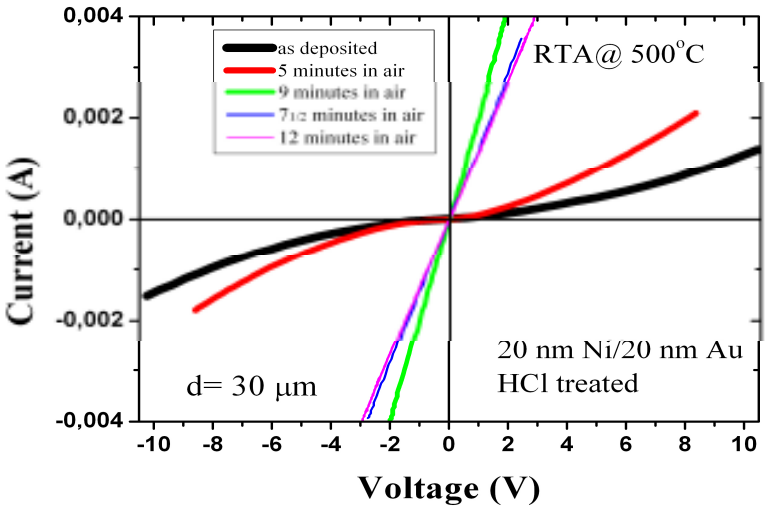


Fig.5.9 *Typical I-V curves for air annealed Ni/Au contacts for different durations.*

nealing for 5 minutes proved to be insufficient for the necessary reactions to be completed. The best obtained result was for the 9 minute case, while annealing for longer time seems to be degrading contact performance. A possible explanation for the latter could be the complete layer inversion between Ni/NiO and Au as opposed to Au clusters embedded inside the NiO volume (fig. 5.5). Since the results are indicating that annealing for longer than 10 minutes increases contact resistance, the upper limits of annealing duration were not tested beyond 12 minutes, which is also beneficial for keeping the contamination levels of RTA system's chamber low.

In conclusion, the annealing process of Ni/Au contacts was studied. The rectifying behavior of the as deposited p-GaN/Ni/Au contacts became ohmic when contacts were annealed in air, while remained rectifying for the vacuum and N_2 ambient annealed contacts. Parameter optimization study showed best results for annealing at 500°C for 9 minutes in the case of 20 nm Ni/20 nm Au, with contact resistance values being < 500 Ω for 30 μm spaced contacts. However, the best obtained ρ_c values by now in our Ni/Au contacted samples are $\sim 10^{-2}$ Ω cm^2. These values should be compared to much lower reported ones (10^{-5}-10^{-6} Ω cm^2), even though the respective contact resistances are comparable or even higher than ours. The reasons for this discrepancy still remain unknown. Nevertheless, a point that hasn't yet been researched is the surface contamination or native oxide layer, which if present can limit contact performance. The influence of several acids as the pre-deposition surface treatment step on the contact performance is discussed in the next paragraph.

5.3.2 Surface treatment experiments

NiO is considered to be a p-type semiconductor but surface native oxides are electrically insulating. Either in the form of adsorbed O atoms from the air or GaO_x phase, its existence at the metal-semiconductor interface might be the reason for the still high ρ_c values obtained in the oxidized 20 nm Ni/20 nm Au contacts. A more detailed discussion on the commonly obtained contamination of p-GaN surfaces and the impact of surface treatments on the contact electrical behavior follows at paragraph 5.4. Towards removing any contamination layer from the p-GaN/Ni interface, several acid solutions were employed as the surface treatment step prior to metal deposition, namely: HCl 32%, HF 5% and 50%, Buffered Oxide Etching (BOE), HF: HCl: H_2O and

boiling aqua regia (HCl: HNO_3). Typical I-V curves of as deposited 20 nm Ni/20nm Au contacts subjected to the above surface treatments are shown in fig. 5.10. A first observation by this graph is that not all treatments have the same influence, with the HF treatments causing pronounced degradation in contact conductivity. The rest treatments seem to slightly improve contact conductivity, with HCl, aqua regia and BOE giving the best results among the ones tested. Nevertheless, this improvement is marginal and is probably related to thickness reduction of the interface SB, since this improvement mostly occurs in the low-voltage regime, where tunneling dominates. The fact that HF treatment is not favoring contact conductivity can be explained by the increased tendency of F ions to be adsorbed on and passivate GaN surface. On the other hand, this effect seems to be reduced in the BOE case, where the solution's pH value is fixed. The exact reasons for this different behavior of BOE, as well as of the HCl: HF: H_2O treatment as compared to HF, are not yet known.

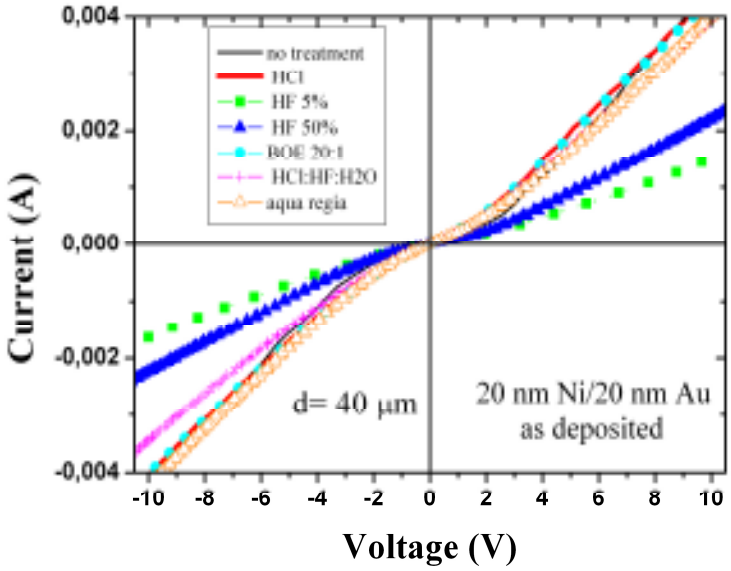


Fig. 5.10 *Typical I-V curves for as deposited Ni/Au contacts after different pre-deposition surface treatments.*

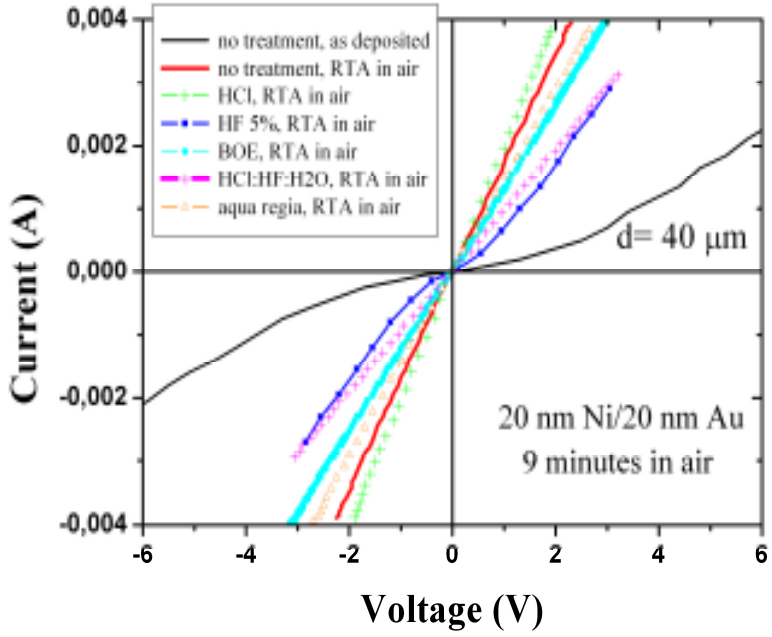


Fig.5.11 *Typical I-V curves for air annealed Ni/Au contacts after different pre-deposition surface treatments.*

Typical I-V curves of the treated samples after annealing at

500°C for 9 minutes in air are shown in fig. 5.11. The HF treated sample gave again the worst results among treated and non treated samples. It is the only case that did not give a completely linear I-V curve, indicative of a barrier existing at the interface not thin enough for holes to tunnel through. The latter is the case for the rest of the treatments used, with the HCl treated sample giving the best results, followed by aqua regia, BOE and HCl: HF: H_2O. Nevertheless, the I-V curve of HCl treated sample is very close to the non treated sample's one, which yields lower resistance values than aqua regia, BOE and HCl: HF: H_2O treated samples. It seems therefore, that the marginal beneficial effect of these treatments on the as deposited p-GaN/Ni/Au contacts is not enforced during the air annealing, rather the opposite. A possible explanation would be the incomplete or insufficient removal of the non conducting native oxide phases or adsorbed O layer from p-GaN surface prior to metal deposition, which leads to enhancement of these non conducting phases at the interface, as opposed to the proposed NiO and Au clustering formed, during annealing in air (80% N_2, 18% O_2). Moreover, existence of such phases at the interface might inhibit H removal from the surface/ near surface of p-GaN, since O atoms from air are involved in this process, which need to come in contact with p-GaN surface through Ni. The results of fig. 5.11 indicate that HCl is more efficient in removing native oxide or adsorbed O from the p-GaN surface, which is in agreement with XPS results.

In conclusion, immersion of p-GaN samples in HCl solution prior to metal deposition seems to favor tunneling through as deposited and air annealed p-GaN/Ni/Au contacts and this behavior can be attributed to more sufficient oxide or adsorbed O removal from the p-GaN surface prior to metal deposition. However, the fact that the best results of the HCl treatment is very close to the results of the non treated sample indicates that during contact annealing in air, O reaction with Ga atoms from the surface of p-GaN probably lead to GaO_x and/or Ni-Ga-O phases formation as well[5], dominating over any beneficial effect of surface treatments. Nevertheless, the fact that HCl treatment had a positive effect to the contact conductivity after the air RTA points out the possibility of improving p-GaN/Ni/Au ohmic contacts if the surface has been treated efficiently prior to metal deposition.

5.3.3 Two-step metallization procedure

In order to clarify the effect of the oxidation at the interface, a two-step metallization procedure was employed, which firstly involved the deposition and thermal treatment of p-GaN/Ni contact and secondly the deposition of Au with an additional thermal treatment step. Thus, two experiments were done within the two-step metallization procedure: (a) Ni deposition / 1st RTA in air for 2 minutes/ Au deposition / 2nd RTA in air for 7 minutes and (b) deposition of Ni / 1st RTA in vacuum for 2 minutes/ deposition of Au / 2nd RTA in air for 7 minutes. The only difference in the two experiments is the first annealing step of the p-GaN/Ni contact, which in case (a) might result in Ni-Ga-O phases at the interface and NiO formation on top, while in case (b) might result in Ni-Ga (gallide) or Ni-Ga-N formation at the interface and Ni on top or just a non abrupt p-GaN/Ni interface.

Typical I-V curves of Ni/Au contacts prepared with cases (a) and (b) of the two-step procedure, as well as single step, oxidized with the optimized procedure, contacts are shown in fig. 5.12. Case (a) did not give ohmic contacts under all temperatures and annealing times tested for both RTA steps. To the contrary, case (b) yielded ohmic contacts with lower resistance values than the optimized single step ones and the best result so far for the specific contact resistance (5 x 10^{-2} Ω cm^2). One explanation for this behavior is that, in case (a) the first annealing in air resulted in the formation of Ni-Ga-O phases, which generates a huge barrier at the interface. Evidence for the Ni-Ga-O phase was obtained from XRD measurements. In this explanation however, the possible inability of Au to diffuse through NiO, or whatever are the first

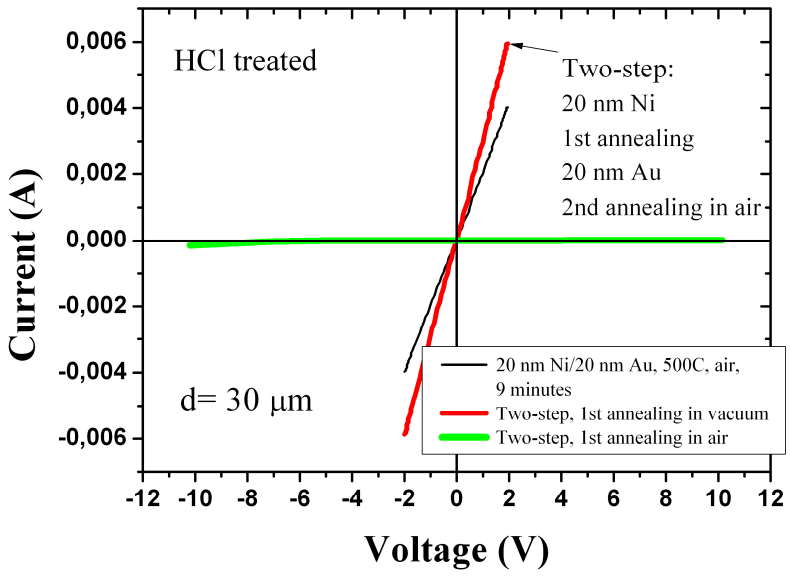


Fig.5.12 *Typical I-V curves of Ni/Au contacts after the two-step procedure. Only in the case of first annealing in vacuum ohmic behavior was obtained. I-V from single-step procedure is shown as well.*

annealing byproducts, with final formation of a p-GaN/NiO/Au configuration should be taken into account to complete the picture. On the other hand, in case (b), the first annealing in vacuum resulted in the reaction between Ni and GaN with the most possible product being Ni_3N, which is also identified from the corresponding XRD spectrum, while no Ni-Ga-O phase-related peaks were identified. Although XRD is not the appropriate technique for interface characterization, it seems that the combination of these two facts is the reason for obtaining an ohmic-like behavior in case (b). Note that in case (b) the second RTA leads to the formation of NiO and Au clustering in NiO's volume, since the first annealing in vacuum cannot have resulted in complete phase transformation of Ni, while any Ni-N phase possibly formed during first annealing is located at the interface. A linear TLM graph of the case (b) sample is shown in fig. 5.13. This graph yields the lowest specific contact resistance value achieved in this work for Ni/Au contacts in the specific wafer used.

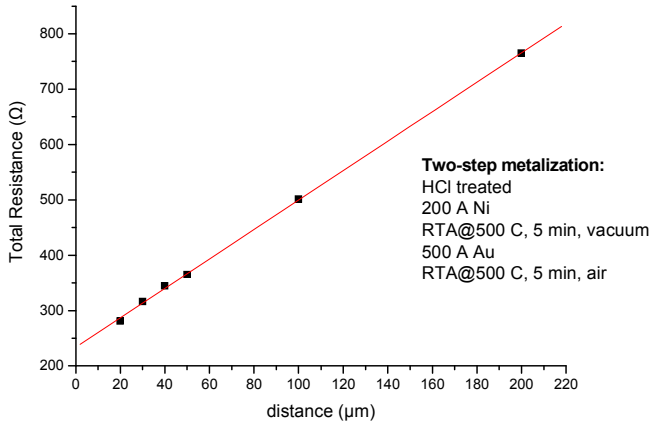


Fig.5.13 *Linear TLM graph of the two-step metallization which gave the best specific contact resistance so far.*

5.4 As deposited metal contacts

Beyond the oxidized Ni/Au contact scheme, a study involving different metal contact schemes followed. The initial objective of this study was to try if a different combination of metal scheme and annealing treatment, other than oxidation, can be found that can yield low resistance ohmic contacts to p-GaN. Towards this, many approaches can be followed, with each one employing different mechanisms to achieve ohmicity, such as metal atom diffusion in the semiconductor side and vice versa, which might result in alloying and/ or overdoping the

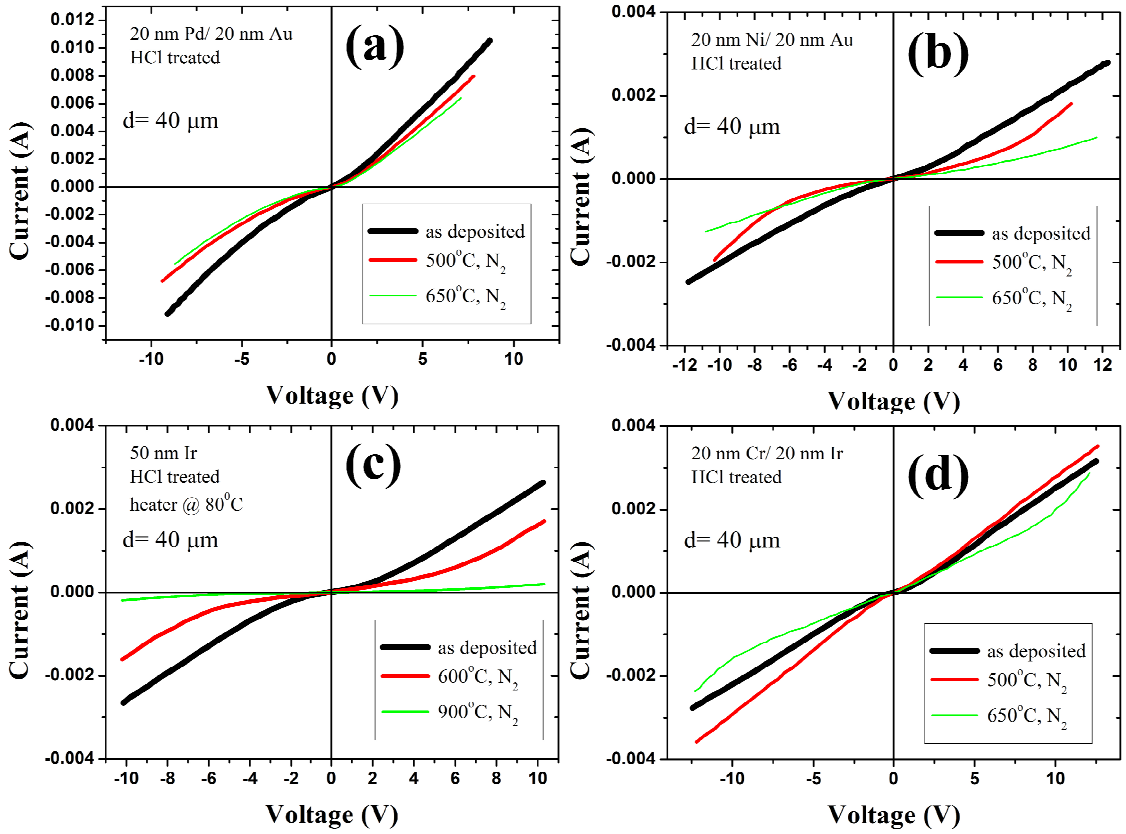


Fig. 5.14 *Typical I-V curves of as deposited and annealed Pd/Au (a), Ni/Au (b), Ir (c) and Cr/Ir (d) contacts to p-GaN. Contact degradation after annealing is clearly observed in all cases.*

semiconductor, as well as contacting p-GaN with a p-type semiconducting layer, like in the case of NiO. Note that, alloying of metal and semiconductor atoms should result in conductive phases at the interface if ohmic contacts are to be formed, while overdoping can occur if H is removed from the surface/ near-surface region of p-GaN. Efforts to find a different metal combination able to alloy with and/or overdope p-GaN upon annealing at moderate temperatures have not resulted

in ohmic contact formation, as can be seen in fig. 5.14 (a), (b) and (c) and (d) for the cases of Pd, Ni, Ir and Cr respectively. Although this study was not fully completed, in the sense that neither many multilayered structures nor annealing at high temperatures (T > 750°C) for various annealing ambients and pressures were tested, the first results clearly indicate contact degradation after annealing. In the Pd, Ni and Ir cases, contact resistance increased after annealing at all temperatures tested, while a slight improvement obtained for the Cr/Ir contacts when annealed at 500°C, also turns into degradation if temperature rises to 650°C. These results are indicative of the enhanced chemical inertness of GaN on one hand, but its increased tendency to lose surface nitrogen on the other. Despite the facts that N_2 was used as the annealing ambient in all cases and that samples were capped with a properly sized piece cut from a GaN wafer (GaN top layer faces the sample surface) for annealing temperatures ≥ 600°C, N loss seems unavoidable with a negative effect on metal contacts' performance. Moreover, the I-V curves depicted in fig. 5.14 are typically obtained ones, since these experiments where repeated more than once in some cases.

Based on the observation that as deposited contacts conduct better than annealed ones, along with the conclusions formed in paragraph 5.3 about the beneficial effect of HCl on contact performance, our research focused on surface preparation prior to metal deposition rather than annealing the deposited metal contacts. This decision was supported by published results, where as-deposited Pt/Au[17, 18] and Pd/Au[19] ohmic contacts have been demonstrated on one hand, while alloyed contacts typically measure in the kΩ range. Despite the fact that as-deposited Pt/Au and Pd/Au contacts are also in the kΩ range, it is very important to stress that the ohmicity of these contacts was achieved mainly after the use of a proper surface treatment and the subsequent deposition of high work function metals, like Pt and Pd. This suggests that if lower resistance ohmic contacts were to be obtained on p-GaN, the pre-deposition surface treatment step would be crucial through reduction or even elimination of any non conducting interface layer (oxide or adsorbed O atoms or other contamination), having as a final result the modification of the surface for deposition of high work function metals. A detailed analysis of semiconductors surface properties and the way surface treatments can modify a surface can be found in subsection 5.1.2. Therefore, a study involving the use of different contact metals and several surface treatments for novel, as deposited ohmic contact formation to p-type GaN followed, with these results presented in the following two subsections.

The p-type GaN samples used in this study (par. 5.4), were from the same commercial (TDI 11OK28-1) Mg-doped GaN wafer grown on a 2" c-axis Al_2O_3 substrate with a MOCVD system, which is different from the one used in paragraph 5.3 (TDI 11OK29-2). The p-GaN wafer was delivered thermally-activated with a carrier concentration of ~ $3.5 \cdot 10^{17}$ cm^{-3} as determined from Hall measurements. Again for uniformity reasons, all samples used were from the central area of the same MOCVD wafer and had the size of ~ 7x7 mm^2. After organic degreasing and lithographic patterning of the samples, the surface treatment step was realized, followed by immediate loading of the samples in the vacuum chamber of our deposition system. In order to ascertain the rectifying or ohmic nature of the contacts, and the influence of the various surface treatments and metals used, I-V curves were obtained with a programmable curve tracer. For the ohmic contacts, the circular Transmission Line Model (c-TLM) was employed to obtain specific contact resistance values, with the pattern used having seven different spacings varying from 10 to 58 μm. As a reminder, the c-TLM geometry does not require mesa isolation of the patterns therefore no chloride RIE was performed. This is important for the study of as deposited contacts since no surface contamination originating from the RIE process (see also par. 4.1 and 4.4) occurs prior to metal deposition process. The latter utilizes the lift-off patterning technique, thus the sample's surface is subjected to at least one lithography procedure prior to metal deposition. Partial or even complete removal of the lithography- related contamination is another purpose for using a surface treatment process prior to sample's loading inside the high vacuum chamber of our e-beam system. This issue will be discussed again in 5.5, where an alternative process flow is considered.

5.4.1 Contact metal study

First, the relation between the contact metal's work function and the corresponding contact electrical behavior was examined. It has to be stressed at this point that apart from enhanced conductivity, equivalent to low serial resistance (slope of the contact's linear I-V curve; $\Delta V/\Delta I$ at the linear part of the curve if not linear), contacts can be considered ohmic if the corresponding I-V curve is both symmetrical and linear. The various metals tested for this study as the contact metal to p-GaN were: Ni, Al, Cu, Ir and Cr. Ir and Ni were chosen due to their high work func-

tion values (5.2 and 4.9 eV respectively), although this was not the only criterion for the metal choice. Typical I-V curves of 42 μm spaced, as deposited contacts, with the above mentioned metals as the contact metal, are shown in fig. 5.15, where the corresponding work function values are shown as well. Immersion in HCl solution for 120 seconds was chosen as the surface treatment and was kept the same in all cases. The latter is necessary for a meaningful comparative study, since each surface treatment can yield different contact resistance for the same contact metal, as discussed in 5.3.2. The treatment's duration was increased to 120 from 60 seconds, which was the duration in the oxidized Ni/Au treatment experiments, for more efficient removal of any interface oxide or contamination. It has to be noted that in the case of Ir only, mild heating (< 100ºC) of the sample in the vacuum chamber prior and during the deposition took place for better metal adhesion on the p-GaN surface, while thorough checking for metal cracking or other failure were performed before the sample's electrical characterization. This procedure was followed due to Iridium's high elasticity modulus, which causes Ir films deposited on foreign substrates, like GaN, to form cracks and detach from the substrate during the lift-off procedure.

Although I-V characterization cannot provide a quantitative estimation of the interface

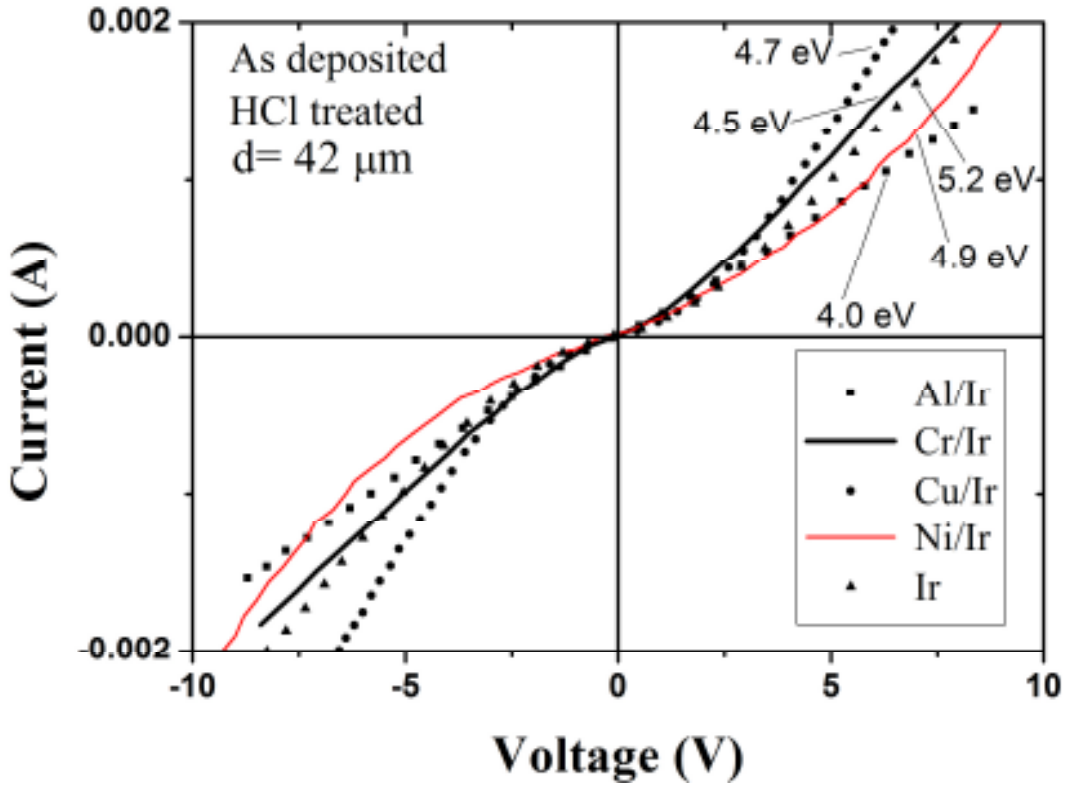


Fig. 5.15 *Typical I-V curves of different as deposited contact schemes to p-GaN. Contact metal's work function values are also shown.*

barrier, it can be useful in a qualitative analysis of the results. By inspecting the I-V curves of fig. 5.15, there seems to be no apparent relation between the metal work function and the corresponding electrical behavior of the p-GaN contact, in terms of both resistance and ohmic-like nature (linearity), obtained from the contact's corresponding I-V curve. p-GaN/Ir system is the most characteristic example, since this contact conducts worse (higher resistance) than p-GaN/Cu and p-GaN/Cr ones despite the higher work function of Ir as compared to that of the rest metals[20]. The picture remains the same if linearity is considered, since I-V curves of Cr/Ir and Al/Ir contacts are almost linear as can be more clearly seen in fig. 5.14(d) for the case of Cr/Ir. Despite the fact that Al possesses the lowest work function, Al/Ir contacts are very similar to Ni/Ir ones (especially for voltages up to 5 V) and this observation supports the above mentioned insensitivity of contact behavior to the metal work function, since Ni possesses the second higher work function value in this study. On the other hand, Cu and Cr (4.7 and 4.5 eV respectively) form contacts that conduct better than Ir and Ni do (5.2 and 4.9 eV respectively), although Cu/Ir contacts cannot be characterized as ohmic due to the intense non linearity of their I-V curves. Considering the lower work function of Cr than that of Cu, the interface barrier should have been more noticeable in the Cr/p-GaN case than in the Cu/p-GaN one.

Table 5.1
Metal and GaN electronegativities (after [24])

	Work function (eV)	**Electronegativity χ**	$\chi_M - \chi_{GaN}$
GaN	7.5	4.5	0
Al	4.0	4.20	- 0.3
Ti	4.3	3.65	- 0.85
Cr	4.5	4.65	0.15
Cu	4.7	4.55	0.05
Ni	4.9	5.20	0.70
Ir	5.2	5.55	1.05

The fact that, I-V curves of fig. 5.15 are from as deposited contacts limits possible interactions between p-GaN and metal at the M/S interface, since no alloying or atom diffusion from the metal to the semiconductor side and vice versa are expected. The above remarks are first indications that surface properties of p-GaN are present and influence metal/p-GaN interfaces. Especially in the p-GaN case, the possibility that p-GaN surface is active becomes stronger if one considers three facts: a) hexagonal c-axis GaN surface has a strong polar character adsorbing polar molecules or charged species, b) Mg doping affects crystal quality and further increases defect density both in the bulk and at the surface and c) p-GaN samples have been subjected to an acceptor activation annealing, which might be promoting oxide formation at the surface. Moreover, large amounts of H exist in the bulk of MOCVD GaN: Mg crystals through Mg-H complexes and this is the picture also expected at the surface. Moreover, p-GaN surface is characterized by inversion domains (N-faced areas on a Ga-faced surface) and grain boundaries (borders of such neighboring different polarity areas), which also affects carrier concentration [21]. Furthermore, Mg accumulation effect has been observed at p-GaN surfaces, leading to O adsorption on Mg atoms too[22]. Therefore, a large active site density is expected for the p-GaN surface from crystal defects alone, since dislocation density values of ~ 10^{10} cm^{-2} are commonly observed[23]. Considering that each dislocation extends up to the surface and involves more than one surface atoms, the corresponding active site density must be much larger. At least 50% of them have been occupied with adsorbed oxygen or other species after air exposure[24].

Assuming that all the adsorbed species are removed by the HCl surface treatment and that all sites are interacting with metal atoms, the simple electronegativity concept can be used to give a rough estimation of charge transfer and polarization of the corresponding dipoles formed at the interface. These dipoles then contribute to the effective interface barrier formation, which is the one actually inhibiting carrier transport through the interface. For more electronegative than GaN metal atoms, the induced metal-GaN dipoles are expected to decrease barrier height and width and enhance hole tunneling. In table 5.1 are summarized the p-GaN electronegativity differences with Al, Cr, Cu, Ni and Ir according to Miedema's scale[25], as well as their work function values. As can be seen in this table, enhanced hole transport through p-GaN/Ir interface should have been obtained, since Ir is the most electronegative metal used in this study. Nevertheless, this is not the case neither for Ir nor Ni, which is the second most electronegative metal used. On the other hand, p-GaN/Al contact's higher resistance is consistent with the lower Al electronegativity as compared to that of p-GaN. However, Al is the only case that yields negative electronegativity

difference and one would expect a noticeably worse p-GaN/Al contact behavior, which is also not the case. Cr- and Cu-related differences are on the average, with Cr-GaN dipole being in theory slightly more polarized than the Cu-GaN one. Still, it cannot explain the increased serial resistance of the Cr/Ir contacts as compared to that of Cu/Ir contacts for voltages > ~ 3.5 V.

The above abnormal behavior indicates that the assumption initially made for complete contamination removal is not valid in our case. This implies that a considerable amount of metal atoms are actually adsorbed or bonded on already adsorbed species, with area distribution of this effect being rather random. The latter could explain the abnormal electrical behavior dependence of p-GaN/M contacts on χ_M-χ_{GaN} difference. If these species do not favor charge transport, through inappropriate alignment of their molecular (or atomic) orbitals to the bulk metal and p-GaN states, then the equivalent picture is of a metal layer deposited on a partly covered p-GaN surface with a thin insulating layer. These species can be either adsorbed O or oxide phases formed or any other adsorbed polar molecule/ion/radical at the surface that have not been removed by HCl, or that have been re-adsorbed on the freshly exposed, after the HCl treatment, active sites. This point calls for research towards surface treatment's efficiency to remove contamination from the surface prior to metal deposition on one hand, which will be dealt in the next subsection. On the other, it might prove impossible to obtain a surface totally free of contamination due to practical reasons (even if the processing fellow is very agile, there will be 5-10 seconds mediating for sample mounting and loading inside the vacuum chamber). Furthermore, there is always H which is very effective in passivating active sites and Mg acceptors in p-GaN. If this is the case, the contact metal research should turn towards seeking another metal property other than work function and electronegativity.

Considering the above, it would be beneficial if the deposited metal can further assist contamination removal from p-GaN surface and a way for this to be done is by using **getter** metals. As getters, are generally considered the substances that have the ability to pump ambient gases (H, O_2, N_2, CO, CO_2, H_2O, etc) through chemisorption on their surface and subsequent diffusion into their volume[26]. Some metals, like Ba, Zr, Ti and Cr have excellent gettering properties[27], while Ni is also known to adsorb gasses on its surface (remember the catalytic role of Ni during Ni/Au oxidation). In fig. 5.16 are shown typical I-Vs of contacts formed with Ti, Cr and Ni as the contact metals. Despite the facts that Ti possesses the lowest work function value and is the less electronegative metal among the three, Ti forms contacts with the lowest resistance. The latter, as can be observed in fig. 5.16, holds only under forward bias conditions, i.e. rectifying behavior is

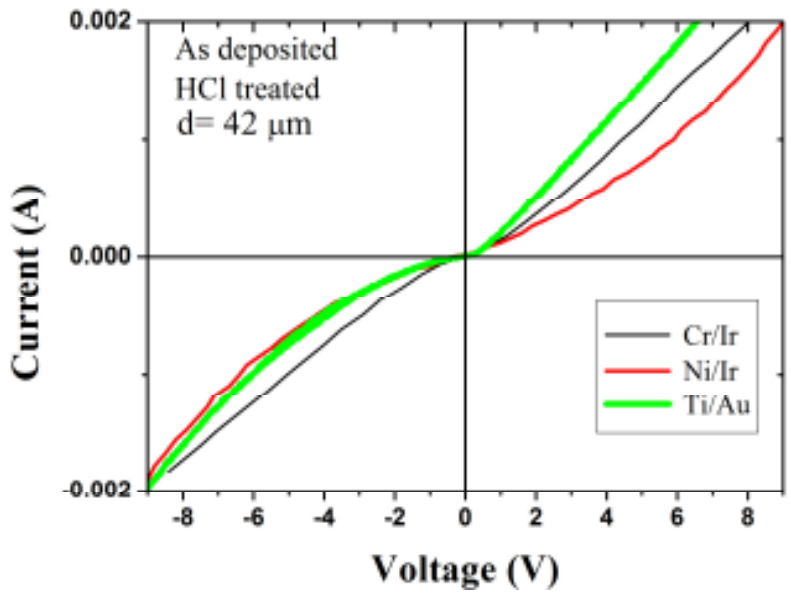


Fig. 5.16 *Typical I-V curves of contacts to p-GaN using getter contact metals (Ti, Cr and Ni).*

observed. One possible explanation for this might be lateral non uniformity of the effective barrier across the Ti/p-GaN interface, which is locally varied, since circular TLM geometry cannot introduce such deviations in current under reverse and forward bias. In this light, a closer look in the gettering mechanisms of Ti and Cr would be enlightening in explaining the different electrical behavior of Cr/Ir and Ti/Au contacts.

Ti and Cr are two characteristic examples of getter metals although they differ in gas atoms' diffusion extend inside their volume after adsorption of gases on the metal surface. Adsorption rates of O_2 and N_2 were found to be similar for Ti and Cr[28], although their behavior is distinguished with presence of H. Both Cr and Ti adsorb H, however, in the Cr case is rather limited at the surface as opposed to Ti where diffusion in the bulk occurs[29]. Moreover, in the presence of both H and O_2, Ti starts to adsorb O_2 rather than H, while H adsorption rate in Cr is not affected by O_2 adsorption. The fact that H and O_2 diffuse into the bulk of Ti must affect its chemical composition and properties, whereas no such effect is observed for Cr [Dylla et al.]. In the case of p-GaN surface, where all of the above contamination can be found, Ti and Cr gettering properties make the difference. However, Cr/Ir contact's corresponding I-V curve is closer to becoming linear, as opposed to the rectifying behavior of Ti/Au. Thus, it would be safe to assume that Cr gettering mechanism, which is based in simultaneous pumping of hydrogen, oxygen or other species seems to outrank the preferential oxygen species adsorption of Ti. It also has to be noted that Au as the second metal seems to favor contact conductivity compared to Ir, as will be discussed below. In this light, Ti/Ir contacts should be conducting worse than Ti/Au and probably Cr/Ir. Moreover, Cr/Ir results are repeatable and contacts are more robust than Ti/Au ones.

Nevertheless, the above remarks indicate that H, O, N, and probably other species, have simultaneously been adsorbed on p-GaN surface active sites prior to metal bonding. Especially for the presence of O species, the nature of which having been disputed for many years now, the possibility of considerable, residual O-related contamination on p-GaN surface after the HCl treatment is further supported by our observations on the role of ambient during annealing of Cr/Ir contacts. As mentioned in this section's introductory, our initial study involved annealing experiments. An unexpected result, considering the role of H in p-GaN, was that annealing Cr/Ir contacts in forming gas ambient (95% N_2 + 5% H_2) consistently improved contact resistance. Nevertheless, this improvement is marginal and might be connected to H-mediated O removal from the Cr/p-GaN interface. The latter stresses again the importance of surface treatment prior to metal deposition.

5.4.2 Boiling Aqua Regia surface treatment

By surface treatment is meant any process used to modify surfaces of semiconductors for precise surface analysis experiments or subsequent metal deposition. Such processes commonly utilize wet chemicals, dry etching, ion bombardment, annealing or a combination of them. For instance, N_2 atom bombardment or exposure to NH_3 and subsequent annealing in UHV can result in obtaining well-known GaN surface reconstructions[30]. The surface treatment to be applied depends on the application; if Schottky contact formation is the objective (Schottky diodes, FETs), the surface treatment applied prior to metal deposition should result in reduction of active sites in order for abrupt interfaces and Van Der Waals type of bonding to be obtained, according to discussion of subsec. 5.1.2. This can be accomplished by utilizing appropriate wet chemicals, like KOH, P_2S_5 or $(NH_4)_2S_x$ solutions, since OH^- and S^{-2} are very effective in passivating dangling bonds and other types of active sites[31], [32], [Motayed]. For ohmic contact formation, however, a major objective of pre deposition surface treatment should be direct metal adsorption and covalent type of bonding on active sites of p-GaN surface, which might even result in short-range epitaxial growth. In this light, any insulating layer (as termed in the previous subsection), even partly covering p-GaN surface prior to metal deposition, must be removed. In the followings, the study involving again utilization of several wet chemicals is presented. The

chemicals used here were the same as in the study for oxidized Ni/Au contacts, i.e. HCl 32 %, HF 10 %, BOE, HF: HCl: H_2O and **boiling aqua regia** (1 part HNO_3: 3 parts HCl, T>36°C). Utilization of ion bombardment and/or dry etching techniques is generally considered to be beneficial for ohmic contact formation due to generation of more surface active sites available for metal bonding. In p-GaN, however, such techniques are not expected to promote ohmic contact formation, since a considerable amount of surface N will be ostracized as well, introducing in this way donor states on the surface. However, such experiments will be presented in subsection 5.5.1.

Typical I-V curves of as deposited 20 nm Cr/20 nm Ir after the several surface treatments mentioned above are shown in fig. 5.17. The better electrical behavior of the boiling aqua regia (AR) treated sample is evident after observation of this graph, despite the shorter duration (30 seconds) of this treatment as compared to the rest (120 seconds). The reason for this shorter duration is intense degradation of photoresist (PR) patterns due to fast etching by boiling AR. The 30 seconds immersion time in boiling AR is marginal for the minimum PR thickness needed for the lift-off process to be successful. However, if one considers the isotropic nature of wet etching, a lateral reduction of ~ 1 μm in PR pattern's dimensions must be occurring. This corresponds to a twice reduction in each TLM spacing of ~ 2 μm, which affects our measurements and would rather be avoided. Nevertheless, boiling AR seems to have a positive effect on contact performance and so does immersion in HCl for 2 minutes, which gave better results as compared to the non treated sample's I-V. This has been reported in the past, where the efficiency of both HCl and boiling AR to remove O and C related contamination from the surface was ascertained by means of XPS analysis, although boiling AR was more effective

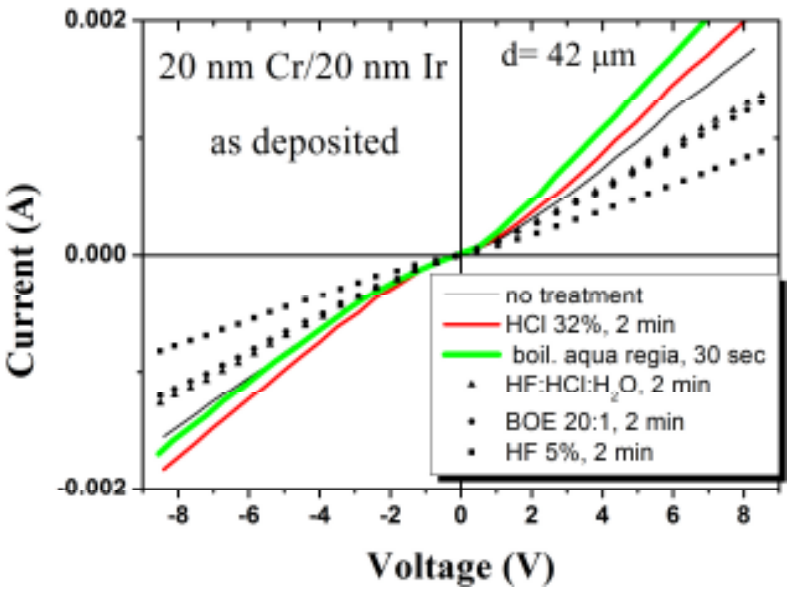


Fig. 5.17 *Typical I-V curves of as deposited Cr/Ir contacts to p-GaN after use of several pre-deposition surface treatments. Boiling AR and HCl give the best results.*

and gave Pt contacts with lower ρ_c value by 3 orders of magnitude, as compared to HCl [Kim et al, Electr. Lett.]. On the other hand, BOE, HCl:HF:H_2O and HF treatments gave again the worst results, like in the Ni/Au case (subsec. 5.3.2). It seems that F ions are effective in passivating active sites, inhibiting in this way covalent-type of bonding between Cr and GaN. Since the negative effect on contact performance of F containing treatments was confirmed once more, these treatments were not used any further.

From the above discussion, the need for optimizing the boiling AR treatment process has emerged. Therefore, a study involving exposure/development times and hard bake conditions followed, with the objectives being PR endurance in boiling AR and minimized pattern dimension loss. Taking advantage of the acquired know-how from subsec. 4.3.1, exposure and development times were tuned for minimum exposure conditions in order to increase, as possible, dimensions of the initial PR pattern, while a hard bake step at 110°C on a hot plate proved to enhance endurance in boiling aqua regia. Moreover, experiments with varying AR solution's temperature during immersion were performed. The temperature is monitored with a liquid mercury thermometer, which is also immersed in the solution. However, the hot plate used and the nature of the solution didn't allow for many temperature points to be taken above AR's boiling point (~ 36°C). The depicted in fig. 5.18 I-Vs of as deposited Cr/Ir contacts, formed after using the 2-step boiling AR treatment at two solution temperatures, ~ 40° (35-45°C) and ~ 50° (45-55°C), indicate that temperature of boiling AR solution during immersion does affect contact performance, with the lower temperature tested giving better results. Therefore, AR solution's temperature during immersion was monitored every time. Note that the metal tip of the thermometer didn't show any marks of etching as

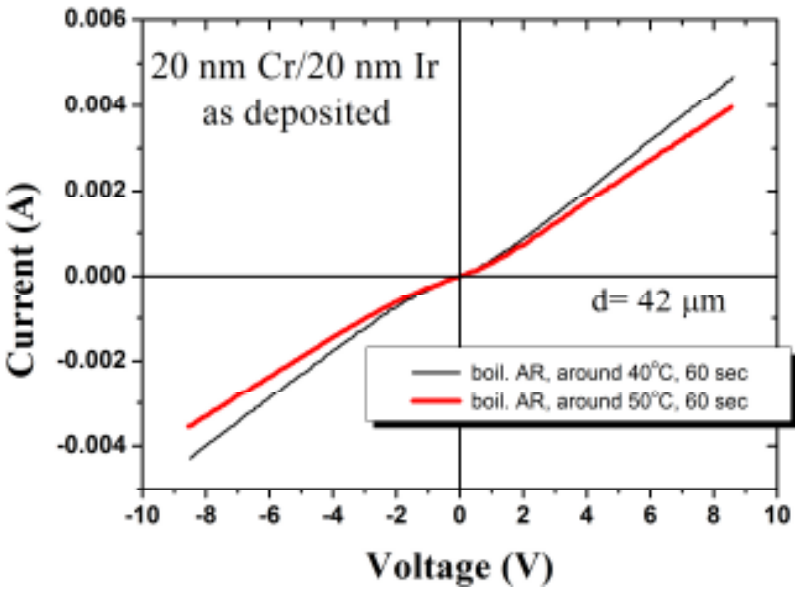


Fig. 5.18 *Typical I-V curves of as deposited Cr/Ir contacts for two different AR solution temperatures.*

checked repeatedly at the optical microscope. The result was endurance of PR patterns for immersion up to 90 seconds, although not repeatedly, with 60 seconds giving submicron reduction in TLM spacings, as estimated by thickness measurements of PR and SEM observations, while lift-off was not problematic. Nevertheless, the 60 seconds immersion time might not be enough for complete contamination removal, thus the idea of subjecting p-GaN

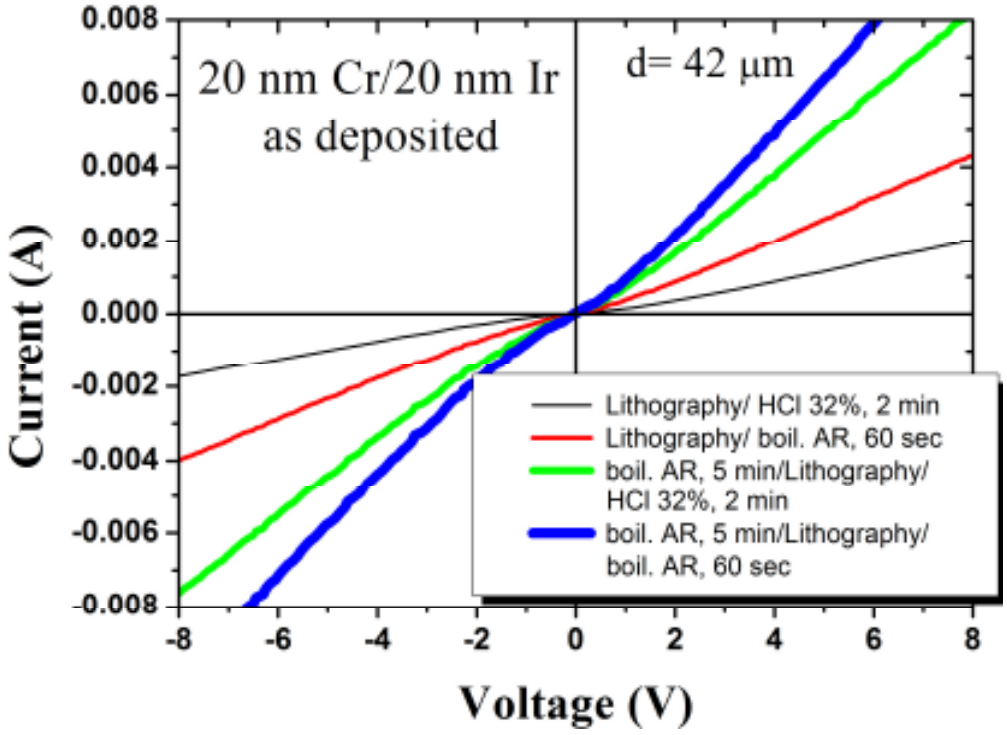


Fig. 5.19 *A long boiling AR step prior to lithography improves conductivity of as deposited Cr/Ir contacts to p-GaN.*

samples in the boiling AR prior to the lithography procedure was realized. Moreover, since the surface is free from PR patterns, much longer immersion times in boiling AR can be realized. The resulting conductivity of as deposited Cr/Ir contacts after utilization of a 5 minute boiling AR treatment step prior to lithography are shown in fig. 5.19.

The depicted I-Vs are from contacts where p-GaN surface has been subjected to the above described 2-step surface treatment procedure (first step: 5 minutes in boil. AR/lithography/second step: HCl or boil. AR), where results of single-step 2 minute HCl or 60 seconds boiling AR treated samples after lithography are shown for comparison. Addition of the long boiling AR first step, significantly improves contact conductivity, since contact resistance is now reduced (~ 800 Ω) by a factor of 2.5 as compared to the single-step boiling AR treatment (~ 2 kΩ) and goes up

to a factor of 5.5 (~ 4.5 kΩ) for the single HCl one. The 2-step treatment employing only boiling AR gives better conductivity than the one employing HCl, as the second step, and this implies the increased efficiency of boiling AR to also remove lithography-induced O and C contamination.

In order to verify the positive effect of boiling AR to contact ohmic behavior beyond the Cr/Ir contact scheme, a similar study followed with Pd, Ti and Ni. Ni/Au is the most used contact scheme to p-GaN (in its oxidized form) and, as mentioned, Ni has a strong catalytic role in the contact's formation mechanism. Furthermore, Ni has been used for low temperature p-GaN activation, which is commonly performed at temperatures higher than 750°C[33]. Some published works claim that Ni-mediated p-GaN film activation was observed for annealing as low as 200°C[34]. Such catalytic behavior has been also reported for Pd, when resistivity reduction and p-type conductivity of Pd covered GaN:Mg layers obtained, after annealing at 200°C in N_2 ambient, was ascribed to Pd-mediated H desorption from the layers through Mg-H complex dissociation[35]. Pd/Au is also a scheme often preferred as a metal contact to p-GaN due to its high work function value (5.0 eV). Ti, as discussed previously, is a well-known getter metal and it would be useful to check with it the 2-step boiling AR treatment. HCl was employed as the second treatment step for contacts of fig. 5.20(b) to be obtained, as is the case for (a) and (c).The results are shown in fig. 5.20 (a), (b) and (c) for as deposited Pd/Au, Ti/Au and Ni/Au contacts respectively. Especially for the latter, the results after air annealing are shown too. From these graphs, it is evident the positive effect of the long boiling AR step prior to lithography as compared to the conventional HCl treatment in all as deposited cases. In Pd and Ni cases especially, the 2-step

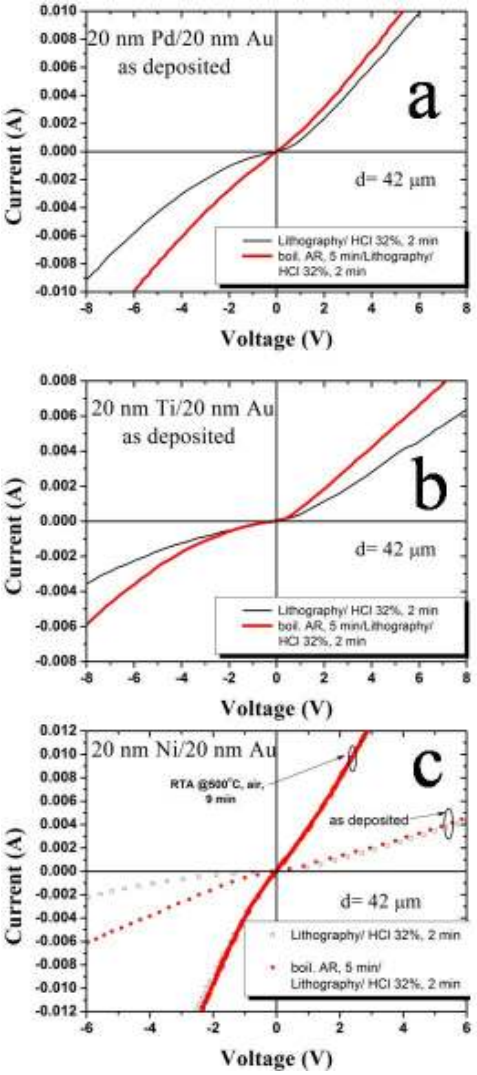


Fig. 5.20 *The long boiling AR step prior to lithography improves conductivity of Pd/Au (a), Ti/Au (b) and Ni/Au (c) contacts*

treatment enhances ohmic nature of contacts as evident by the symmetric and almost linear I-V curves of the corresponding contacts. However, as can be seen in fig. 5.20(b), the rectifying nature of as deposited Ti/Au contacts remains. This behavior can be attributed to the getter mechanism of Ti, which absorbs O species rather randomly in its volume, causing even closely located Ti contact patterns, and the Ti/p-GaN interface underneath, to have different electrical properties. It is worth mentioning that the ~ 200 Ω resistance value of the oxidized Ni/Au contacts shown in fig. 5.19(c) are among the lowest ever reported. This might indicate that electrical properties of the wafer used in this study are at least the typical obtained in the literature for good quality MOCVD GaN: Mg, if not better, while some credits have to be given to the single-step Ni/Au metallization process flow optimized in section 5.3. Another thing to note from fig. 5.20(c) is that upon air annealing, any beneficial effect of pre deposition surface treatment in the as deposited Ni/Au contacts, disappears when contacts are annealed in air. This was, more or less, the conclusion formed in subsection 5.3.2.

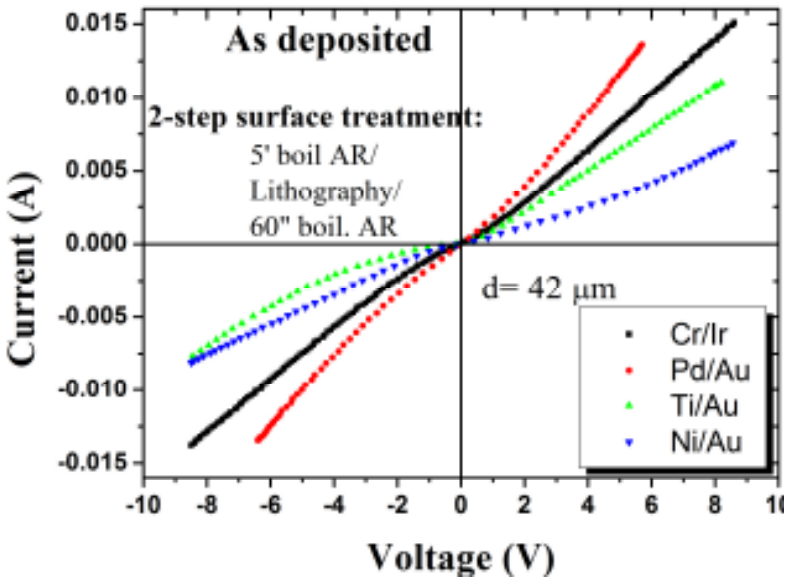


Fig. 5.21 *Typical I-V curves of as deposited contacts after the two-step boiling AR treatment.*

In fig. 5.21, typical I-V curves of contacts formed after the 2-step treatment, with boiling AR applied in both steps, for Pd/Au, Ti/Au, Ni/Au and Cr/Ir are shown. All cases improved further with application of the boiling AR second step as compared with HCl (Cr/Ir curve is the same as in fig.5.19). Nevertheless, the rectifying character of the Ti/Au contacts remained after the full boiling AR treatment. Either random Ti material degradation speculated above or some other Ti property is responsible for ascribing a rectifying nature to the Ti/p-GaN contact. Based on this, Ti/Au was not further searched as feasible solution for as deposited ohmic contact to p-GaN.

To the contrary, conductivity of as deposited Pd/Au after the boiling AR –based treatment is the best among the rest contacts depicted in fig. 5.21, with Cr/Ir contacts being the second best. The latter is the only contact with Ir as the second metal above the contact metal. As a reminder, Ir had been chosen due to its high work function value and the possible ohmic contact formation

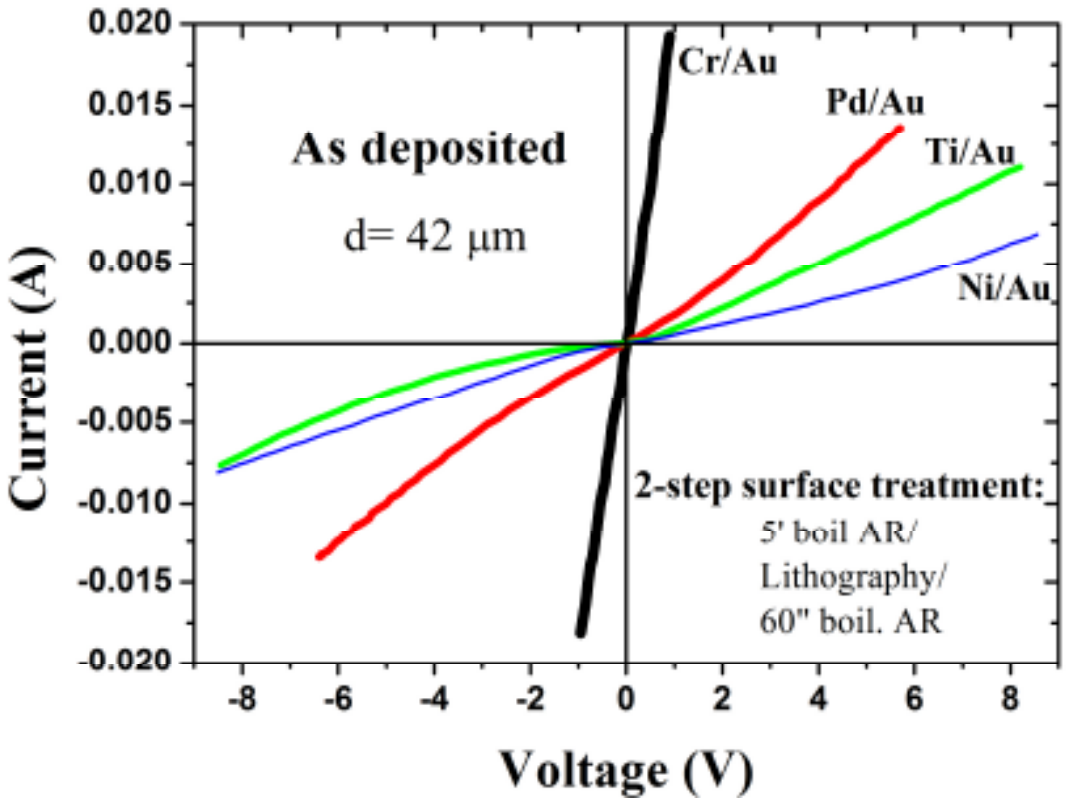


Fig. 5.22 *The combination of the two-step AR treatment and as deposited Cr/Au yielded ohmic resistance value of ~ 50 Ω.*

via diffusion through the getter metal and intimate bonding with p-GaN upon annealing. This mechanism did not seem to be the case and it was decided to aim towards as deposited contacts, as mentioned to the beginning of this section. Moreover, there have been indications from contacts having Pd, Ni and Cu as the contact metal that Au as the second metal gives better results as compared to Ir. For example, Pd/Ir contacts were almost not conducting, whereas Pd/Au are the best obtained in fig. 5.21, while as deposited Ni/Au contacts (fig. 5.20(c) or 5.14(c)) are better by a factor of more than 2 as compared to as deposited Ni/Ir ones (fig.5.15 or 5.16). The same is the case for Cu and, as seen in fig. 5.22 this is also the case for Cr. When the 2-step boiling AR surface treatment was applied and 20 nm Cr/20 nm Au were deposited on p-GaN, a low resistance as deposited ohmic contact to p-GaN was finally obtained. This contact's

I-V curve yields an ohmic resistance value of ~50 Ω, which is the lowest ohmic resistance ever reported for as-deposited or even heat-treated contacts to p-GaN [36, 37, 38].

By replacing Ir with Au as the second metal, contact conductivity is improved by an order of magnitude. In a first approximation, this effect might be purely mechanical, i.e. Cr film is lifted from p-GaN surface due to Ir film-induced strain. On the other hand, this would have resulted in rectifying behavior of the contacts, which is not the case. This point will be discussed again below. Nevertheless, I-V curves of fig. 5.22 are directly comparable, since the only difference among the corresponding contacts is the contact metal and, more importantly, all experimental results presented are from contacts formed on the same commercial TDI wafer, as is the case for the whole section 5.4.

5.5 As deposited Cr/Au contacts

Fig.5.23 resumes I-V curves of all as-deposited metal contact schemes to p-GaN[39] investigated in this study. These curves are the best obtained for each metallization scheme and for all the pre-deposition surface treatments mentioned above (Cr/Ir I-V is after single-step boiling AR treatment). As can be seen, almost all of the as-deposited contacts on p-GaN show rectifying behavior with kΩ range resistances, whereas the Cr/Au contact after boiling AR treatment stands out with its low resistance value of ~ 50 Ω.

By inspection of Fig.5.23, one can clearly see that the three best results (Cr/Au, Pd/Au and Ti/Au contacts), in terms of low contact resistance, are obtained after the use of the two-step boiling AR treatment. Addition of the first, long boiling AR step proved to be crucial for the good results depicted in fig. 5.22 and 5.23. This conclusion, however, does not hold for all metal schemes used. For instance, for the as-deposited Ni/Au contacts, the I-V curves of the AR-treated samples were somewhat better than the HCl-treated ones, with this better behavior of AR-treated samples vanishing upon air annealing, making them altogether not very different from the ones obtained in untreated samples. On the other hand, for all the different metal schemes, the HF-containing treatments gave the worst results in terms of contact resistance, despite the known ability of such solutions to etch oxides, such as SiO_2. It seems that the high reactivity of F ions is

responsible for their strong adsorption on p-GaN surface, passivating in this way active sites with profound effect on contacts ohmic behavior.

As discussed at the end of subsection 5.4.2, the only difference among the three best contacts of fig. 5.23 is the contact metal. In this light, Cr forms the best as deposited contacts to p-GaN, followed by Pd and Ti. With p-GaN suffering from residual H in the bulk, adsorbed species at the surface and a considerable density of dislocations in the bulk emerging at the surface, it must be the gettering properties of Cr and Ti and the catalytic properties of Pd, which are responsible for the three best results, as compared to the rest of metals tested. Among the three, Cr seems to 'fit' p-GaN surface in a better way leading to the low resistance contact formation after the beneficial use of boiling AR. Since deposition of Cr/Au or AR treatment alone cannot lead to such low resistance ohmic contact, it must be the combination of Cr/Au deposition on the p-GaN surface after the use of boiling AR that is responsible for this contact to be formed.

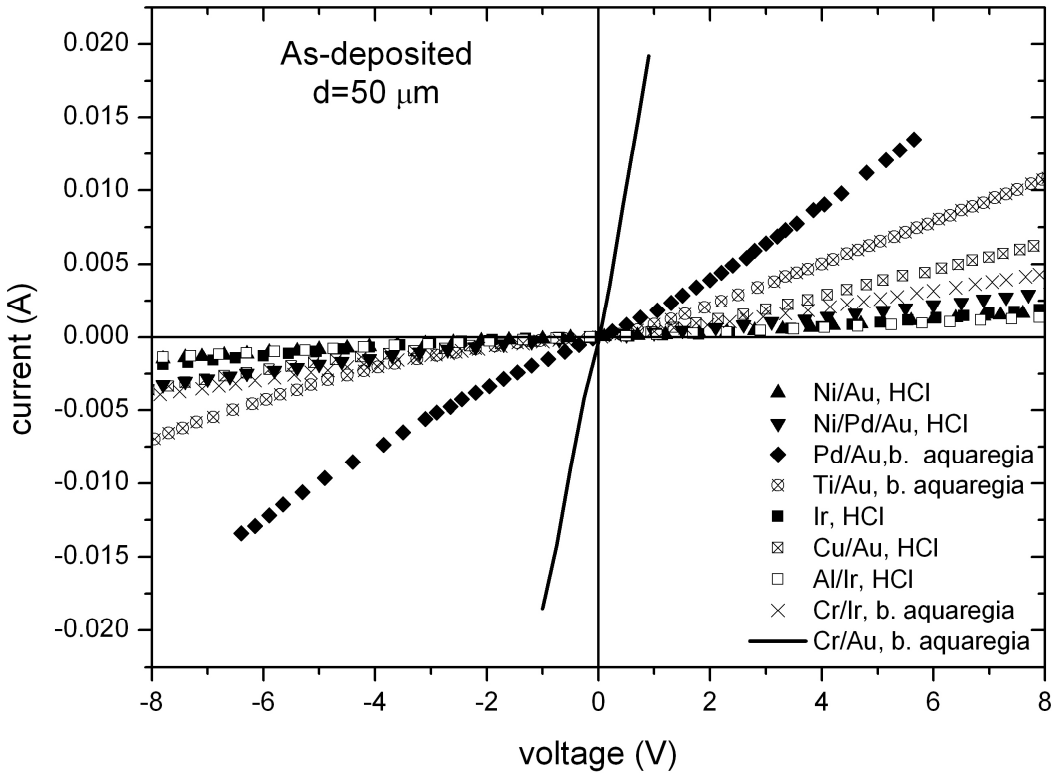


Fig. 5.23 *As deposited contacts to p-GaN after various combinations of contact metals and surface treatments. The low resistance Cr/Au contacts stand out.*

AR is known to be effective in removing oxides, adsorbed O or other contamination from p-GaN surface without passivating the freshly exposed active sites. Any such process has impact on the number of active sites for subsequent metal bonding. As mentioned, dangling bonds can be considered as the simplest example of such sites, demanding for an electron to be exchanged with an adsorbed species[40]. Chromium is a transition metal, with one outer electron and highly oriented d-orbitals available for bonding with the semiconductor atoms (as opposed to the s-like character of Pd and Ti orbitals) which in principle could even favor covalent type of bonding between p-GaN surface and Cr atoms leading to an intimate contact with the d-like orbitals of Ga-related dangling bonds (Ga3d). On the other hand, Cr is a getter material, commonly used in Tokamaks for its ability to pump active gases, such as nitrogen, oxygen and hydrogen, all of which are present in the MOCVD p-GaN material. Especially for H, its absorption from Cr can occur even at room temperature, while Cr can getter even small organic compounds, like CH_4[41]. In this light, as Cr is deposited on the AR treated surface of p-GaN, H and O are simultaneously absorbed by it leading to a contamination-free interface with an overdoped p^+ region underneath. On the other hand, Cr gettering occurs only at its surface leaving bulk Cr unaffected. Moreover, as discussed in 5.4.2, it is when Au was deposited on Cr (after the two-step AR treatment) that a dramatic decrease in contact resistance was obtained. Au is also a well-known H catalyst, whereas Ir catalytic properties are mostly related with interactions with bigger organic molecules[42]. In this light, Au might operate as H reservoir, which diffuses adsorbed-by-Cr H atoms in its bulk, while Cr continues to pump O or C related contamination from p-GaN surface. It is speculated that the combination of the above described mechanisms can explain the good ohmic behavior of the as-deposited Cr/Au contacts after the two-step AR surface treatment.

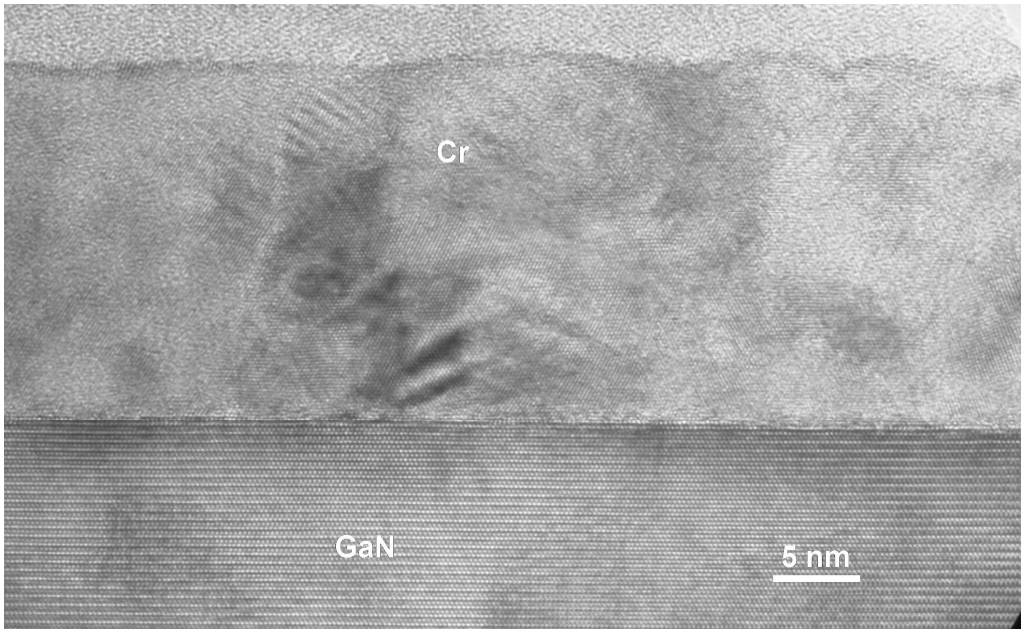


Fig. 5.24 *HRTEM image of Au/ Cr/p-GaN interfaces of a sample yielding the low resistance as deposited Cr/Au value. A non abrupt interface is observed, leading to columnar growth of Cr film on p-GaN.*

In fig. 5.24, a High Resolution Transmission Electron Microscope (HRTEM) image of a p-GaN sample with the low resistance, as deposited Cr/Au contact is shown. This image reveals the intimate bonding of Cr atoms on p-GaN surface, which had as a final result the formation of a non abrupt M/S interface. As discussed in 5.1.2, in non abrupt M/S interfaces there is no such thing as a well defined straight line in a direction normal to the deposition direction, which separates, and keeps apart by a distance $\delta \geq 0.5$ Å the M and S layers. The covalent-like bonding of Cr with GaN atoms has promoted columnar growth of Cr layer on p-GaN as seen in fig. 5.24, with each domain having different growth direction, while no amorphous layer is detected at the interface. Therefore, Cr layer is overall polycrystalline, since epitaxy occurs locally and cannot be characterized as epitaxial. A comparison of fig. 5.24 and bottom 5.4 support the above claims about intimate Cr/p-GaN bonding, which in turn leads to different carrier transport through the two interfaces compared; the one depicted in the bottom of fig. 5.4 corresponds to a nearly ideal Schottky diode. As a reminder, non-abrupt M/S interfaces was the main objective of the study conducted and presented in 5.4 for ohmic contact formation.

5.5.1 Surface treatment in etch-back experiments

A main assumption of the proposed formation mechanism of the low resistance as deposited Cr/Au ohmic contacts is the efficiency of boiling AR to properly modify p-GaN surface prior to metal deposition. The characterization 'proper' refers to surface modification by AR that promotes ohmic contact formation through the covalent-like bonding of metal with S atoms. However, this modification wasn't obtained before application of the long boiling AR step prior to lithography. This point necessitates optimization and accurate control of the whole process for a better understanding of the mechanism and reproduction of the good results to be the case. With photoresist patterning interposing the main surface treatment step and metal deposition, any such control cannot be obtained, since p-GaN surface might be affected in a complex way by the two heating steps, UV irradiation and immersion in chemicals (KOH) of the lithography process. Therefore, process flow of as deposited Cr/Au contacts need to be reconsidered in order for further understanding and optimization of the low resistance system to be obtained through accurate control of the procedure.

Surface treatment, PR patterning and metal deposition are the three different processes involved in the process flow of metal patterns formation. In the most commonly used lift-off technique, which is the one followed so far, p-GaN surface should be patterned with PR before metal deposition. This imposes restrictions to the surface treatment procedure, which in the case of boiling AR had to be broken into two steps. However, if certain requirements are filled, metal patterning can be also obtained by utilizing the metal etch-back approach. As mentioned in subsec. 2.3.4, metal etch-back offers freedom concerning surface treatment prior to metal deposition, since metal layer is first deposited on p-GaN bare surface and then patterning follows. TLM patterns of nominal dimensions were able to be reproducibly obtained after initial experiments for Au and Cr etching optimization. PR AZ 5214 was employed for patterning of the metal layers after adjusting the lithography procedure for image reversal realization (see 2.3.4). Au was etched in an iodine-based solution (2 g KI/0.5 g I_2/ 20 ml Di-H_2O), which left PR patterns unaffected while HCl was used for Cr etching, which also doesn't attack PR. By utilizing the metal etch-back approach, sample can be loaded in the vacuum chamber of the deposition system directly after surface treatment, which simplifies the picture of the surface and makes conclusions extraction safer. It has to be noted at this point that, an optimization of the Cr evaporation procedure was conducted in parallel with metal etch-back process optimization, since fig. 5.24 indicates the

short-range epitaxial character of Cr layer on p-GaN. In this light, fresh Cr flakes were evaporated each time, while deposition rate was reduced to 1 Å/sec (from 3.5 usually employed) as an effort to promote island growth modes (Volmer-Weber and/or Stranski-Kastanov), rather than layer-by-layer, for covalent type of Cr bonding with p-GaN atoms via adsorption on active sites to occur.

In this light, a surface treatment study followed under the revised process flow discussed above. This study aimed in reproducing the low resistance Cr/Au ohmic contacts on one hand and, on the other, to enhance understanding of the formation mechanism of this system. Therefore, samples subjected to the single 5 minute boiling AR treatment step were prepared, as well as samples subjected to a combination of the AR treatment and other chemicals as an effort towards controlling adsorbates on p-GaN surface prior to metal deposition. Measured I-V curves of these samples are shown in fig. 5.25, where the single 5 minute boiling AR treatment gave the

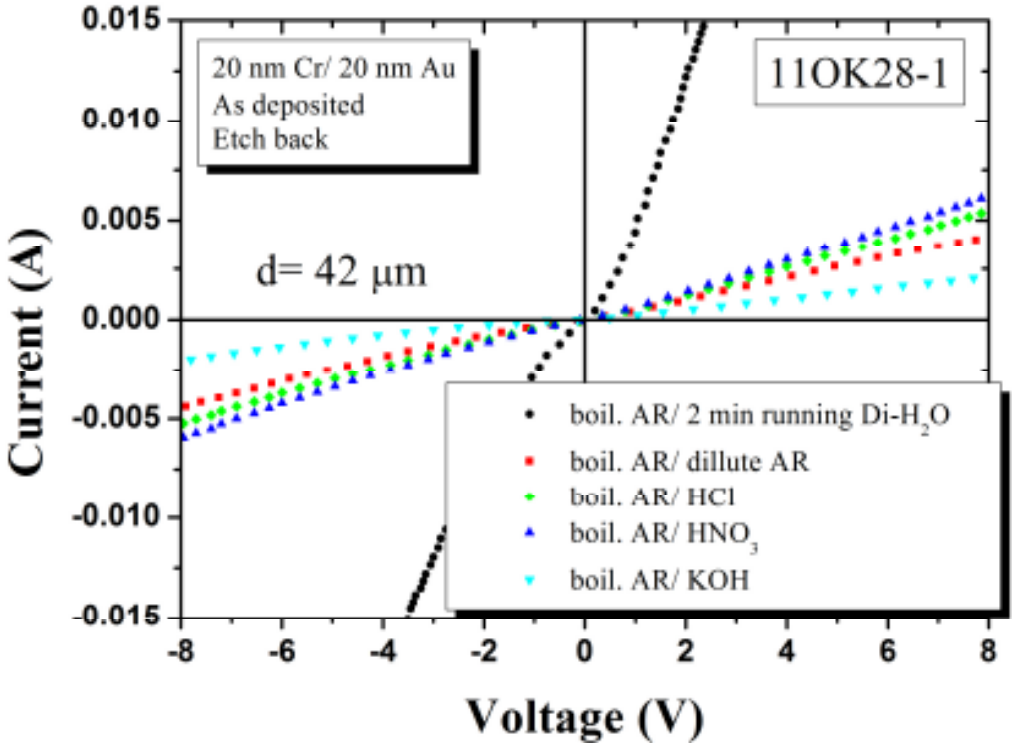


Fig. 5.25 *Effect of different p-GaN adsorbates prior to metal deposition on p-GaN/Cr/Au contacts, where best results are obtained for H_2O after boiling AR treatment. Patterns were formed with metal etch-back.*

best results once more, although not as good as the in results of fig. 5.23. Moreover, the depicted in fig. 5.25 result was obtained only when complete hydration of the p-GaN surface occurred by

sample's thorough rinsing in running de-ionized- (DI-) H_2O for 2 minutes after immersion in boiling AR. Such a long exposure in DI-H_2O ensures complete hydration of the surface according to Morrison[43]. The fact that thorough hydration coming after the AR step is necessary to obtain good ohmic contacts indicates that the ''clean'' polar surface of p-GaN, either needs adsorbed water molecules to passivate unoccupied orbitals of surface states or that water molecules help in Cl ions or other species removal, which have been adsorbed on p-GaN surface during surface treatment. The latter is further supported by the rest I-V curves of fig. 5.25; samples that were just dried with nitrogen after immersion in HCl, HNO_3 or dilute AR solutions, without being hydrated, conduct worse than the ones that were thoroughly hydrated after the AR step, with KOH giving the worst results. The latter results seem to agree with the reported efficiency of OH^- to passivate surfaces through strong adsorption to surface sites [Motayed et al.], which inhibits strong interaction between Cr and p-GaN atoms.

The observed importance of p-GaN surface hydration might also be explained by the fact that, adsorbed H_2O molecules inhibit contact of O or other species from air with the surface restraining their adsorption. In this way, surface is covered by adsorbed water molecules when sample is introduced inside the vacuum chamber, which can in turn be desorbed from the surface, either during vacuum idle time or during Cr deposition, which is also effective in gettering H_2O molecules [Dylla et al.]. The importance, however, of this hydration step hadn't been observed in previous experiments. Therefore, the 2 minute rinsing in DI-H_2O step after the AR or any other treatment was incorporated in the procedure of forming ohmic contacts to p-GaN. However, one has to be very cautious when drying with N_2, since most of the H_2O covering the sample has to be dried away for practical reasons (vacuum of the deposition system), but at the same time, not complete H_2O removal must occur for the above described surface protection from air exposure to be the case.

It has to be noted that the samples used for the results of fig. 5.25 were all from the TDI 11OK28-1 wafer, same as in sec. 5.4. After so many experiments this 2" wafer was consumed and this study had to proceed with new purchased p-GaN wafers. Unfortunately, wafers of resistivity values > 10^4 Ω·cm (as estimated by Hall measurements, since there wasn't the ability for characterization due to this high p-GaN layer resistivity) were delivered to us, which restrained our effort to understand the low resistance contact formation mechanism and consistently reproduce the results. Such a behavior of p-GaN wafers can be the result of Mg overdoping as an effort to increase hole density, which can have the opposite results as mentioned in 5.2. However, not all purchased wafers were so resistive, with TDI 11OK275-4 wafer (actually ¼ of wafer) being one such exception. The behavior and nominal hole concentration of this wafer is very similar to that of 11OK28-1, as indicated by initial correlation experiments with several surface treatments and metals (Pd/Au and Ti/Au). Therefore, the surface treatment study was continued with this ¼ of wafer.

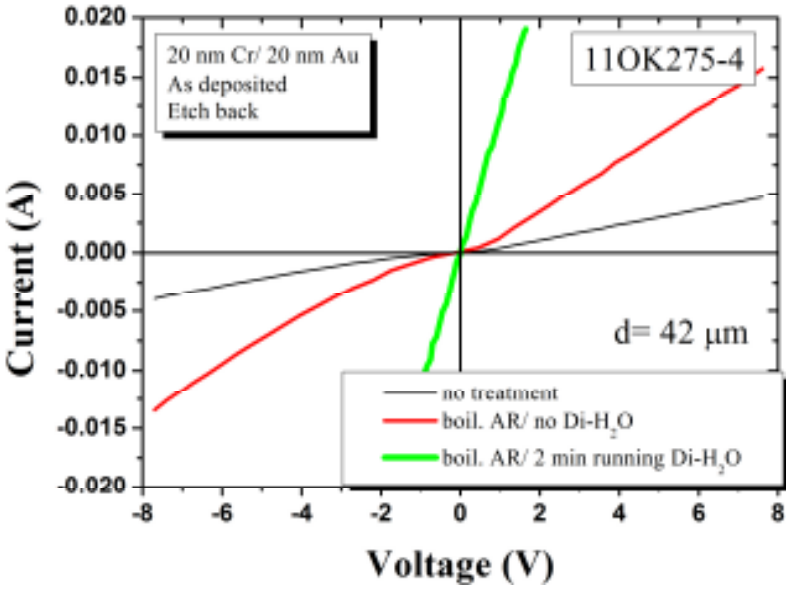


Fig. 5.26 *Effect of hydration after the AR treatment and prior to metal deposition.*

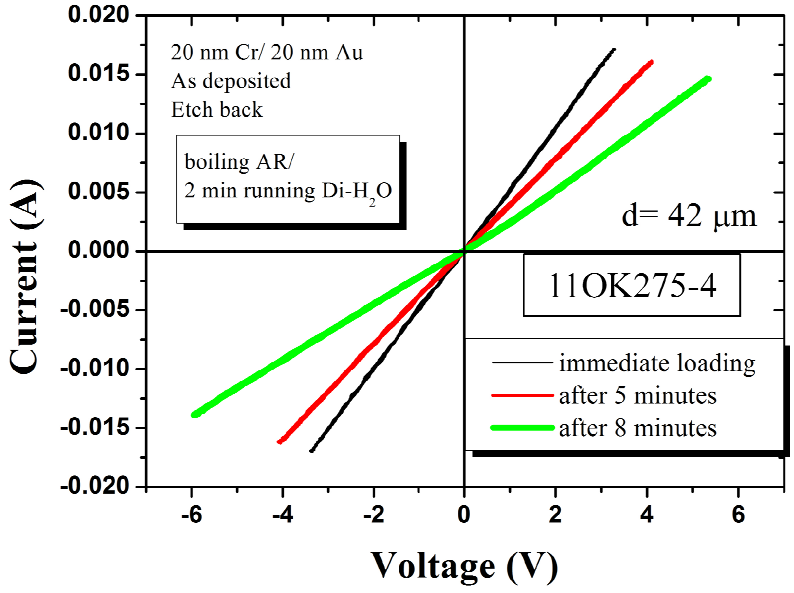


Fig. 5.27 *Effect of p-GaN samples air exposure after surface treatment.*

In exploring the role of surface hydration on contact performance, I-V curves of as deposited Cr/Au contacts with and without DI-H_2O rinsing after the boiling AR step are shown in fig. 5.26. First thing to note from this graph is the similar behavior of this TDI wafer with the one used in section 5.4 and figures 5.24 & 5.25 concerning the effect of boiling AR and surface hydration on contact performance; with application of the boiling AR treatment, a profound improvement can be observed, which is even bigger if the full AR treatment with thorough rinsing is applied.

Furthermore, a series of experiments concerning the time which samples are exposured to air before their loading inside the vacuum chamber followed. All samples were subjected to the same surface treatment process (5 minutes AR/ 2 minutes DI-H_2O rinsing/ rough drying) and, after they were mounted on the holder of Temescal, stayed for 5 and 8 minutes in air or were loaded immediately in the vacuum chamber. Typical I-V curves of samples prepared with the above mentioned procedure are shown in fig. 5.27, which clearly indicate that the longer is the sample in contact with air the more are the chances the surface becomes contaminated from air. The latter assumption must be valid since the only difference in the results of fig. 5.27 is the time interval that samples stayed in air after mounted on the holder and before loaded in the vacuum chamber. Adsorption of air species must be occurring after H_2O molecules have been desorbed from p-GaN surface, while air exposure time needed to start affecting metal bonding to p-GaN depends on hydration degree of the surface. These results also support the assumption made earlier about H_2O molecules desorption in vacuum, which has to be much stronger than in atmosphere ambient. Nevertheless, the importance of both thorough surface hydration and minimized sample exposure to air was evident from the results summarized in figures 5.26 & 5.27, thus, special caution has to be given every time the surface treatment process for ohmic contact formation to p-GaN is executed.

Beyond wet chemicals, RIE and Ion Gun (IG) treatments were tried as well. Both treatments aim in removing any insulating layer from the sample's surface prior to metal deposition. The IG used in this study was the one installed inside our e-beam evaporation system, where there is the ability to etch the sample's surface with an impinging ion beam and subsequently deposit the contact metals in HV without the sample surface being exposed to air. Ar was chosen as the ion source material, thus no chemical interaction is expected between ions and p-GaN surface apart from physical etching. In RIE on the other hand, etching has a chemical component as well, as seen in subsec. 2.3.2, which makes the picture of the post-etched surface more complicated.

Moreover, the sample has to be extracted from RIE's vacuum chamber to be introduced inside the deposition system's one. To minimize air exposure of etched sample, the latter was immediately immersed (inside glove box) inside propanol and stayed there until loaded inside the deposition system. After initial experiments for IG etch rate calibration, a relatively low etch rate process was chosen for the rest of the experiments, namely ~ 1.3 nm/min. In the RIE case, the mild, chloride-based process optimized in the previous chapter was used with an etch rate of ~ 12 nm/min. The evaporator and RIE chamber's pressure were ~ 1.5 x 10^{-7} Torr and ~ 1.5 x 10^{-6} Torr respectively after overnight pumping, while etch depths of 16 and 22 nm for the IG and RIE etched samples respectively were obtained. Finally, Cr/Au contacts were deposited on etched surfaces and defined by metal etch-back.

The samples used in this study were from TG 574 (TopGaN) and 11VS642-1a (TDI) wafers, on which it was not possible to obtain low resistance Cr/Au contacts. This point will be discussed below in more details. Typical I-V curves of boiling AR, IG and RIE treated samples are

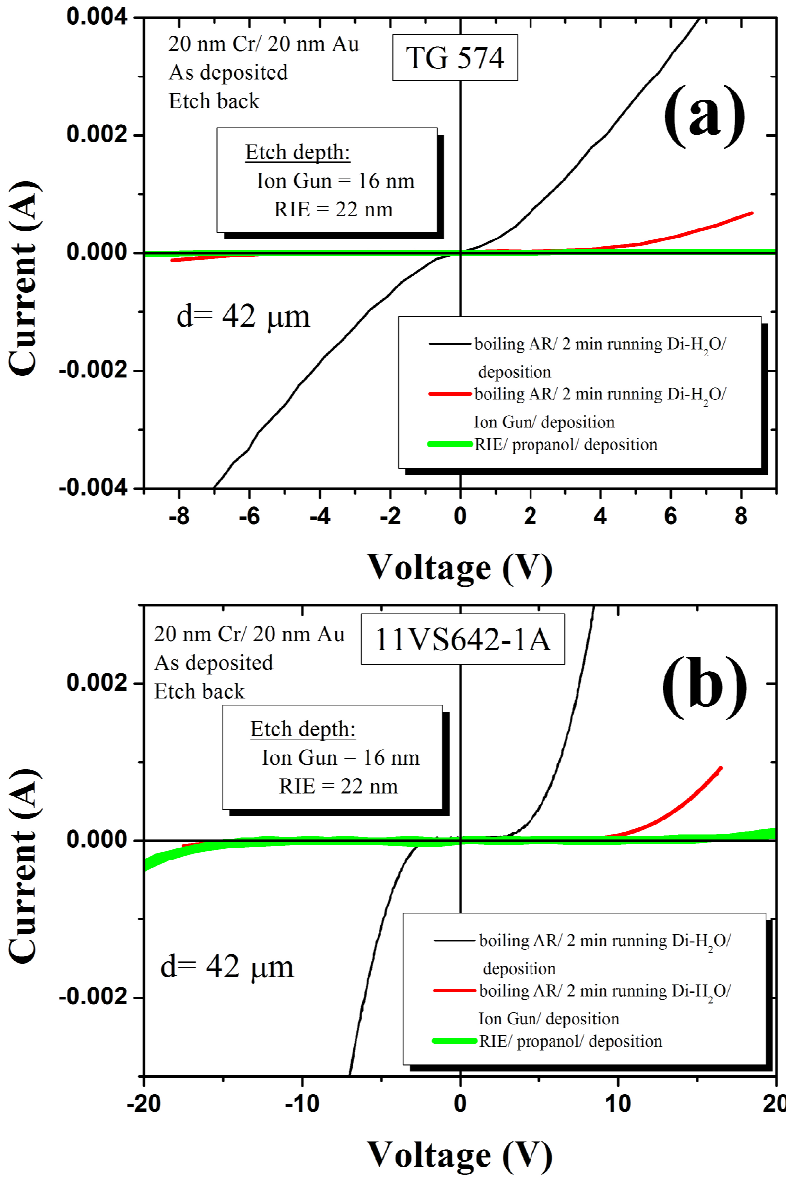


Fig. 5.28 *Typical I-V curves of IG and RIE treated p-GaN samples for the TG 574 (a) and 11VS642-1A (b) wafers. Both treatments have a devastating effect on contact resistance of Cr/Au contacts on both wafers.*

shown in fig. 5.28 (a) and (b) for TG574 and 11VS642-1a respectively. It is clear that both IG and RIE treatments gave worse results in terms of both interface barrier and contact resistance as compared to the AR treated reference samples. The worst results of RIE as compared to IG might be explained by intense surface contamination induced by etch by-products and the lower vacuum levels during RIE process, although all chloride-based chemistry by-products are supposed to be volatile (see 4.3.2). Moreover, one should keep in mind that the RIE sample has been transported from one vacuum chamber to the other and no matter how carefully and fast was the transport it cannot be compared to the in situ IG treatment. Nevertheless, the unavoidable N vacancy introduction on p-GaN surfaces after both treatments seems to dominate any beneficial effect of active site increase induced by them. Overall, IG and RIE treatments prior to metal deposition are not found to favor ohmic contact formation, especially in the case of p-GaN.

In conclusion, a revised process flow was considered and adopted in order to repeat the low resistance as deposited Cr/Au contact scheme and understand its formation mechanism. With this revised process flow no restrictions are imposed to the surface treatments applied, while no PR is present prior to metal deposition, therefore, better control of surface adsorbates is ensured. Again, boiling AR gave the best results; however, thorough surface hydration after AR seems to be necessary to obtain the low resistance as deposited Cr/Au contact scheme, with their performance being affected when sample remains for time > 5 minutes on air after surface treatment. The latter indicates the increased tendency of p-GaN surface to adsorb O or other contamination from air and stresses the importance of thorough execution of sample hydration, N_2 drying and vacuum chamber loading procedures. Finally, IG and RIE processes do not seem to favor ohmic contact formation on p-GaN.

5.5.2 As deposited Cr/Au vs. oxidized Ni/Au

Next, in order to further evaluate the as-deposited Cr/Au contact scheme, we compared it with the well established oxidized Ni/Au one. For this reason, c-TLM patterns were fabricated on adjacent pieces cut from the same area of the 11OK275-4 p-GaN wafer of TDI. The Ni/Au scheme was formed by using the lift-off technique after a two-step surface treatment (first step: 5 minutes in boil. AR/lithography/second step: 2 minutes HCl) was applied, while oxidization at

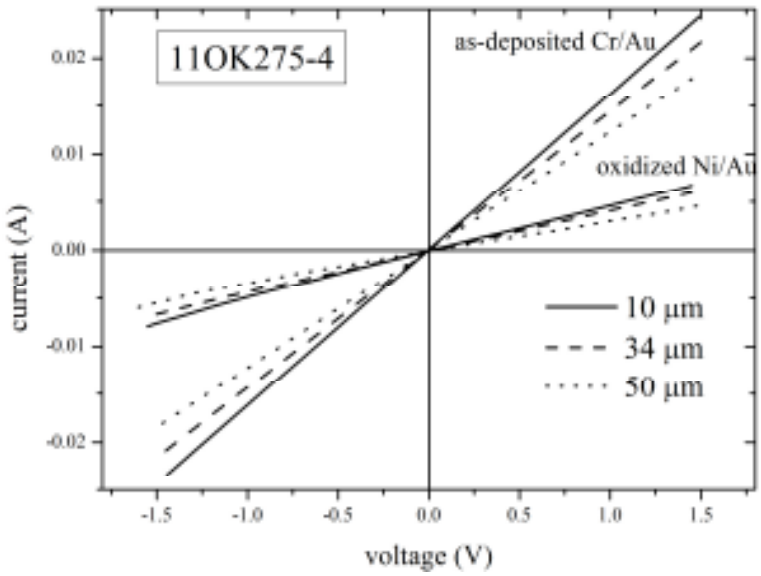


Fig. 5.29 *Comparison of oxidized Ni/Au and as deposited Cr/Au contacts for c-TLM geometry and 3 different spacings.*

around 500ºC in air ambient for 9 minutes followed. In the as deposited Cr/Au case, contacts were formed following the metal etch-back approach with 5' boiling AR/2' rinsing/rough drying being the treatment applied. In Fig. 5.29, the I-V curves of the two different contact schemes for 3 different contact spacings of the c-TLM pattern are shown. A first observation is that the oxidized Ni/Au contacts yield resistances which are among the lowest reported in the literature, as also pointed out in subsec. 5.4.2. Nevertheless, the factor of 3 lower contact resistances of the as-deposited Cr/Au contacts further support the claim that the Cr/Au contacts are the lowest ever reported. From I-V curves of Fig. 5.29 and for two more spacing values, we extracted the resistance values and the TLM plot for each metallization was obtained. The corresponding TLM plot for the as deposited Cr/Au contacts is shown in fig. 5.30. The specific contact resistance (ρ_c) value obtained from this plot is $2.6\text{x}10^{-3}$ $\Omega\cdot\text{cm}^2$, while the corresponding TLM plot of the oxidized Ni/Au contacts yielded a value of $7.0\text{x}10^{-3}$ $\Omega\cdot\text{cm}^2$. These results indicate that the as deposited Cr/Au are better than the oxidized Ni/Au by a factor of almost 3 and are consistent with the results depicted in Fig. 5.29, where one can see that the Cr/Au contact resistance values are lower by the same factor as

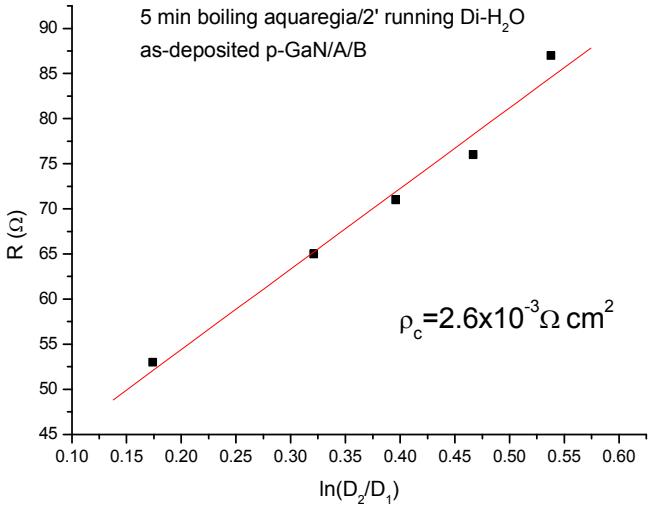
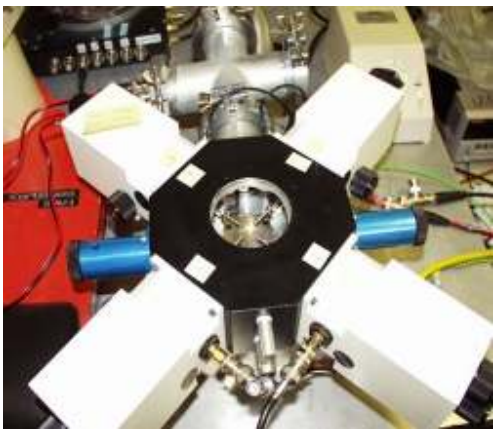


Fig. 5.30 *The corresponding TLM graph of as deposited Cr/Au contacts formed on TDI 11OK275-4.*

compared with the contact resistances in the Ni/Au case. Nevertheless, the ρ_c values of both contacts are in the 10^{-3} $\Omega \cdot cm^2$ range, which is not among the lowest reported in the literature. This point has been shortly discussed in 5.4.

5.5.3 High temperature measurements

In many applications there is need for operation of sensor devices at elevated temperatures. Since nitrides show enhanced thermal stability and are candidate materials for optical sensors, a high temperature operation study of the as deposited Cr/Au contacts on p-GaN is particularly meaningful. For comparison reasons, oxidized Ni/Au contacts were characterized as well. High temperatures I-V measurements were carried out at the R&D center of EADS in Munich. The two different kinds of contacts were formed on the same p-GaN wafer and were the exact same samples as the ones used for comparison of the two different contacts of the previous subsection (Cr/Au: 2.6×10^{-3} Ω cm^2, Ni/Au: 7.0×10^{-3} Ω cm^2). The measurements were performed at a 4 probe station, specially designed for such measurements. A photograph of experimental set up is shown in the top of fig. 5.31. Samples were placed in a vacuum chamber (~ 5×10^{-3} mbar), mounted on a metallic surface, below of which was located the heating element,



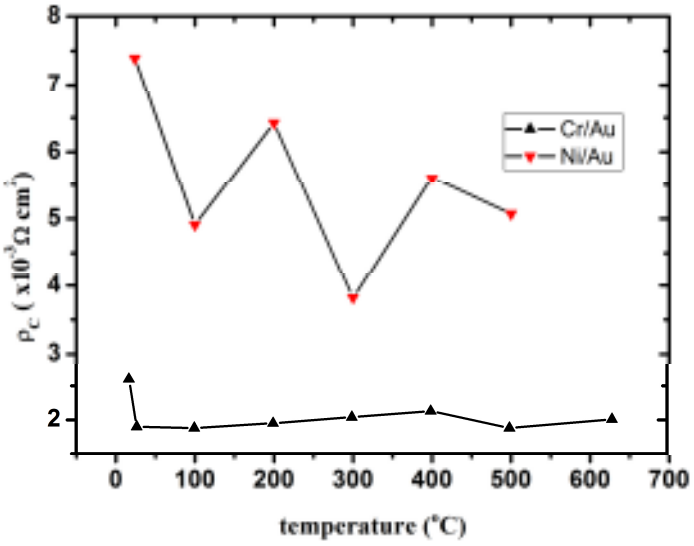


Fig. 5.31 *(Top) Experimental set up for high-temperature I-V measurements. (Bottom) ρc dependence on temperature for Cr/Au and Ni/Au contacts.*

which permitted heating of the samples up to 630˚C. The probes enabled us to measure resistances with various spacing between the contacts of the circular TLM patterns formed on our samples, in order for specific contact resistance values versus temperature to be obtained. For each temperature reached, I-V data were taken after a reasonable period of time (20-30 minutes) for samples' temperature stabilization.

In the bottom of fig. 5.31 are shown the plots of ρ_c values versus temperature, for the two different kinds of contacts. It is obvious that the two contact schemes behave differently with increasing temperature. For the oxidized Ni/Au scheme, the ρ_c value overall decreases with increasing temperature, but non-monotonically. For the as deposited Cr/Au scheme the ρ_c value slightly increases with increasing temperature, but it can be considered almost stable. These observations might be the result of different conduction mechanisms through the interface of the two contact schemes, indicating thermionic-field emission as the dominant current mechanism for Ni/Au and tunneling for the as deposited Cr/Au. It should be noted here that intense degradation of the Ni/Au contacts didn't allow for measurements to be taken at 630˚C, while the Cr/Au contacts proved to be particularly stable and a 5 point TLM graph could be obtained even at 630˚C.

5.5.4 Reproducibility issues

As must have become clear by now, the as deposited Cr/Au contact scheme can potentially serve as a low resistance, robust p-electrode for nitride-based optoelectronics; it can be patterned easily, keeps its mechanical and electrical properties for annealing up to 500°C and beyond, while device process flow can be modified to incorporate the boiling AR surface treatment process prior to metal deposition, as will be seen in chapter 7. However, this low resistance contact scheme was not reproducibly obtained on all p-GaN wafers tested as can be seen in fig. 5.32(a). In this graph, I-V curves of as deposited Cr/Au contacts on different commercial p-GaN wafers are shown, after the AR treatment (5' boiling AR/2' rinsing/rough drying). Since process flow for forming these contacts is identical in all cases, it must be the GaN: Mg layer properties that affect contact resistance. This is further supported by the results of oxidized Ni/Au contacts on the same wafers as shown in fig. 5.32 (b), which followed pretty much the same tendency. Again, since surface treatment is the same for all cases (5' boiling AR/lithography/2' HCl), con-

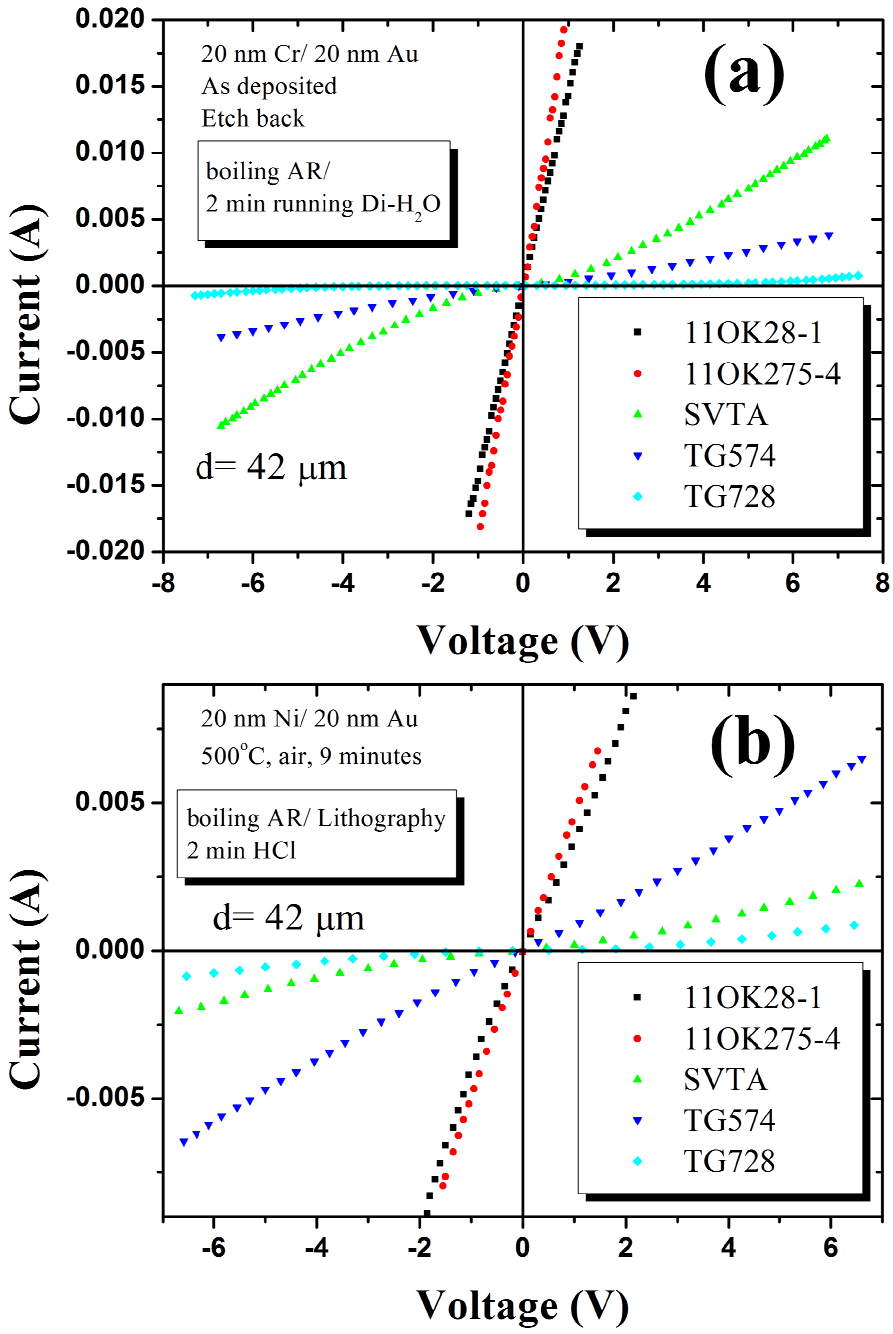


Fig. 5.32 *As deposited Cr/Au (a) and oxidized Ni/Au (b) contacts on different p-GaN wafers.*

tact performance must be affected from wafer properties. Furthermore, the best results of both contact schemes are obtained on the same wafer (11OK275-4) and the same holds for the worst results (TG 728). The observed wafer-dependence of ohmic contacts performance can be understood if one considers the way quantities like doping level, carrier concentration and mobility val-

ues and layer resistivity affect electrical behavior of M/S contacts through the interface barrier formed and the dominating current mechanism.

Towards quest of a low resistance ohmic contact scheme to p-GaN, a systematic work correlating growth details of GaN: Mg crystals and their structural and electrical properties with process flow and final contact behavior is needed. In our case, knowledge of growth details was not feasible since all p-GaN wafers used in this work were commercial and were delivered thermally activated. Even so, a full ohmic contact study could have been feasible if all wafers had similar, or even controllable properties, which was not the case neither. Despite the clear orders for growth of the wafers to be purchased according to the nominal properties of TDI 11OK28-1 or11OK275-4 ones, many very resistive wafers (>10^4 Ω·cm) were delivered to us, with contacts on them (Cr/Au, Pd/Au, oxidized Ni/Au) being far from characterized ohmic. Reliable Hall characterization of wafers wasn't feasible neither despite the painstaking preparation of 5 x 5 mm^2 samples of Van der Pauw geometry etched patterns, due to limitations imposed by the available Hall effect characterization system and high p-GaN layer resistivity. Moreover, there is always the possibility of partial carrier compensation in p-GaN material due to the low hole and the relatively high residual electron concentration levels commonly obtained in both MBE and MOCVD grown nitrides. Magnetic field- and temperature-dependent Hall effect measurements can partly overcome these issues yielding more reliable measurements, however such measurements were not feasible. Apart from measurements that could not be performed, p-GaN wafers were characterized by means of C-V photo-electro-chemical (PEC) etching profiling, XRD and AFM, indicating similar hole concentration levels, while their crystal and surface quality is typical for GaN epilayers grown on sapphire.

The results of the above utilized techniques cannot give a clear and deep understanding of as deposited contact formation on p-GaN. For instance, the measured from AFM surface rms roughness values of wafers cannot be correlated with the obtained behavior of either as deposited Cr/Au or oxidized Ni/Au contacts formed on them, which is also the case if one tries to individually interpret C-V profiling or XRD results alone. But even if combined, no rigid conclusions can be formed apart from general observations, like hole concentration levels ≤ 5 x 10^{17} cm^{-3} (see also discussion in sec. 5.3) and rms roughness values < 1.5 nm seem to favor contact ohmic behavior. Observation of Cr/p-GaN interface with HRTEM alone doesn't help either; in the left side of fig. 5.33 the Cr/p-GaN interface for the TG 728 wafer is shown, while in the right side a magnification of the image depicted in fig. 5.24 (same interface for 11OK 275-4) is shown for com-

parison. Note that TG 728 is the wafer yielding the worst results on both Cr/Au and Ni/Au contacts, while its hole concentration is found to be similar with that of 11OK28-1 and 11OK275-4, as well as its surface rms value, which is similar with that of 11OK28-1 (~ 0.8 nm) and smaller

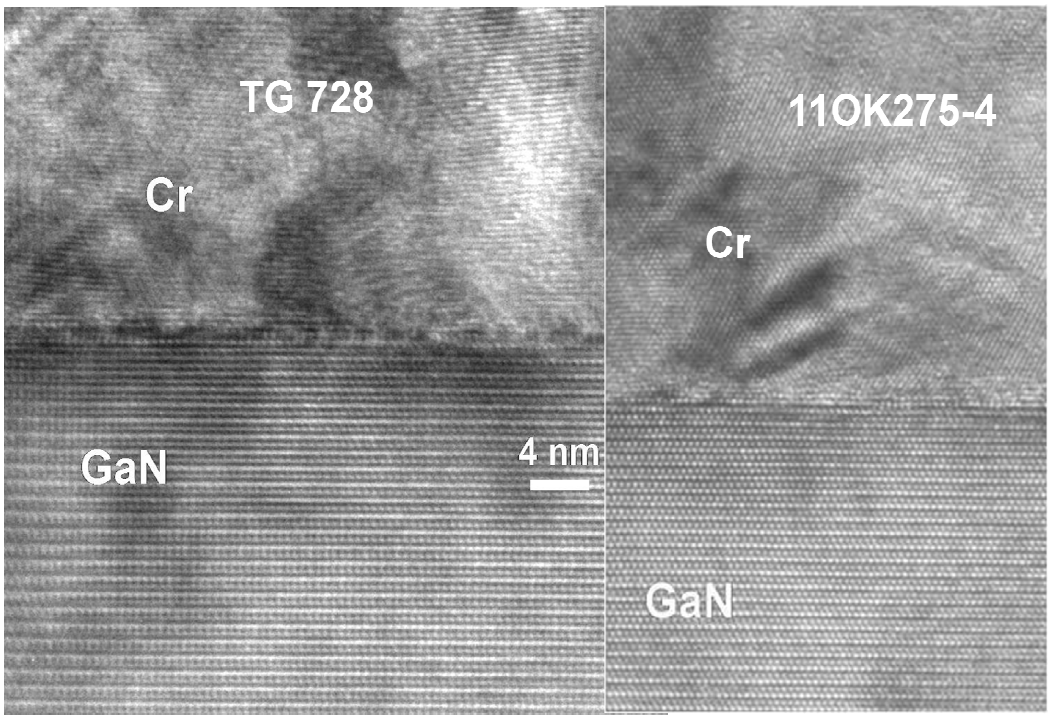


Fig. 5.33 *HRTEM images of the p-GaN/Cr interface for the wafer yielding the worst (left) and the best (right) Cr/Au contacts to p-GaN. Crystal quality of the first metal atomic layers in the right-hand case seems to be superior.*

than that of 11OK275-4. Although an intimate bonding between Cr and p-GaN surface atoms seems to be also the case here (left of fig. 5.33), as is for 11OK275-4 (right), the crystal quality of the first metal atomic layers and of the bulk Cr film seems to be inferior in TG 728 as compared to that of 11OK275-4, especially since the contrast variations of HRTEM images does not seem to be originating from thickness variations along the measured sample. Note that contacts on both wafers were formed with exactly the same procedure in terms of surface treatment (boil. AR/hydration/loading) and deposition conditions (baseline pressure, source material, deposition rate).

The above considerations combined with the fact that any interactions between Cr and p-GaN occur at the Cr/p-GaN interface, make clear that knowledge of surface and interface properties would be a powerful tool towards exploitation of the low resistance Cr/Au contact formation mechanism. As seen in 5.4.2 and 5.5.1 for 11OK28-1 and 11OK275-4, boiling AR surface treatment affects contact performance through the supposed O and other contamination removal from

p-GaN surface, while freshly exposed active sites are passivated by adsorbed H_2O molecules until forth coming Cr deposition, the gettering properties of which, in combination with the catalytic properties of Au, ensure that any residual contamination still present at Cr/p-GaN interface will be absorbed by it leading to short-range epitaxy. As seen from fig. 5.24 and 5.33 such Cr bonding with p-GaN seems to be the case, although not always translated to low contact resistance, while surface composition and properties and the way they are affected by surface treatment still remain unknown. Therefore, utilization of surface characterization techniques is mandatory with X-ray or Ultra-Violet Photoemission Spectroscopy (XPS or UPS) being the most suitable techniques for estimating chemical composition, Fermi level of the surface, as well as the chemical state of surface atoms and adsorbates (see 3.4.2). Unfortunately, by the time XPS characterization of our samples was feasible the two wafers that gave the best results (11OK28-1 & 11OK275-4) had run out. Therefore, it was decided that a typical, in terms of contact performance, MOCVD wafer from fig. 5.32 (TG 574) would be the one studied with XPS. Moreover, it was thought to be very interesting to compare its properties with those of a commercial MBE grown GaN: Mg wafer (SVTA), which is free of Mg-H compensating centers. More about the samples and the results of this study in section 5.6, which is the last of this chapter.

5.6 XPS study of p-GaN surface and p-GaN/Cr interface

As mentioned above and introduced in 3.4.2, XPS analysis is a powerful tool in obtaining composition and electronic properties of the surface. Two quantities that this technique can precisely estimate and can be very useful in the study of ohmic contact formation to p-GaN are Ga: N atomic ratio and surface band bending, with the latter being described by the energy distance of the Fermi level from valence band maximum (VBM) at the surface, denoted as ΔE_F[44]. The first quantity, surface Ga: N atomic ratio is a measure of the surface stoichiometry indicating whether the surface is rich in Ga or N atoms, which as seen so far is important due to the donor- and acceptor-like nature of N and Ga vacancies respectively. The second quantity, ΔE_F, is equally important since it is the initial barrier that has to be "smoothened" upon metal deposition in order for enhanced tunneling to be the case and ohmic behavior to be obtained. Moreover, XPS analysis can yield composition of the surface in foreign species, within the detection limit, and can specify their chemical state. For instance, the existence and nature of O on p-GaN surface can be

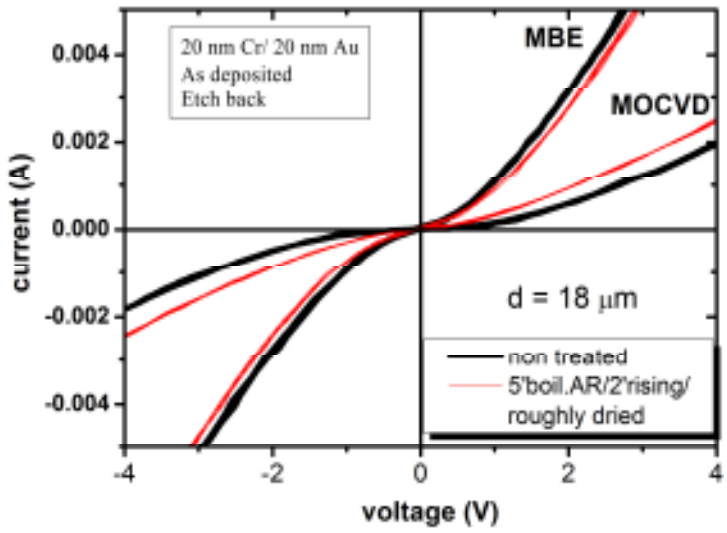


Fig. 5.34 *I-V curves of p-GaN/Cr/Au contacts formed to MOCVD and MBE samples with (red lines) and without (thicker black lines) boiling aqua regia treatment.*

clarified from the combined analysis of Ga3d and O1s core level emission peaks; if O1s peak is detected in the XPS scan and there is no Ga-O bond component into Ga3d emission peak, it is adsorbed O that exists at the surface, whereas it is GaO_x if a Ga-O bond component exists inside Ga3d emission peak. Air contamination levels can be also estimated through C1s emission peak, since C-related are the usual contaminating species of air exposed surfaces.

Knowledge of these quantities in as received p-GaN samples and the way they vary with application of a surface treatment may be able to explain the formation mechanism of the low resistance Cr/Au contacts and the reproducibility issues discussed above. Unfortunately, only two wafers were able to be characterized with XPS and, furthermore, none of them is the one yielding the ~ 100 Ω Cr/Au contacts. Figure 5.34 compares the I-V curves of p-GaN/Cr/Au contacts deposited on the two samples for the same c-TLM spacing, with and without the use of AR. From these curves the overall better electrical behavior of contacts on SVTA wafer (MBE) becomes evident[45]. AR treatment seems to slightly improve contact conductivity in the TG 574 wafer (MOCVD), as opposed to the vast improvement observed after utilization of this treatment in 11OK28-1 and 11OK275-4 wafers. It has to be noted that, AR treatment seems to have the opposite effect in the MBE case, since contact conductivity is rather worse in the treated sample.

On one hand, it seems that the two wafers characterized with XPS are not appropriate for exploring the low resistance Cr/Au formation mechanism as they are both characterized by high layer resistivity values. On the other, TG 574 behaves typically for MOCVD wafer under AR surface treatment in the sense that an improvement, mainly concerning linearity of I-V curves, is observed, even if it is small. Therefore, XPS characterization of the MOCVD sample might shed some light to the formation mechanism of the low resistance as deposited contacts. This effort

can be further enforced by the correlation with results of Cr/p-GaN interface analysis. Moreover, since there is lack of such results in the literature, especially for the MBE p-GaN material, an examination of its surface and comparison of the results with those of MOCVD would be very useful.

5.6.1 Sample preparation

The commercial MOCVD and MBE samples used for this study were both grown on 2'' c-plane sapphire substrates. Their nominal carrier concentration is around $5x10^{17}$ cm^{-3} (after thermal activation for the MOCVD sample) and their nominal thickness is 1 μm. For metal deposition, an e-beam evaporator was used, with the chamber's pre-deposition pressure being around $6.7x10^{-7}$ mbar in all cases. For the electrical characterization of contacts, Cr/Au TLM patterns were formed following the metal etch-back approach after surfaces were treated with boiling AR (5' boil. AR/ 2' rinsing/ rough drying). For XPS characterization, the same procedure was followed for surface treatment of the samples, while special care was given during the surface treatment procedure in order to be able to correlate the results of the two techniques. Despite efforts, loading time in the vacuum chambers of the XPS system remains longer than in the evaporation system, thus XPS samples are exposed in air for longer times after AR treatment.

Concerning the samples preparation for the Cr/p-GaN interface characterization, issues emerged with Cr ease of oxidation. Considering the ~ 9 nm analysis depth of XPS, the deposited Cr layer thickness should be ≤ 5 nm. As soon as a so thin Cr layer is exposed to air, it adsorbs O and oxidizes very quickly, affecting its final thickness and composition. Finally, after some thickness calibration deposition runs and following the idea of protecting Cr with a Au layer (Au can be easily removed by an iodine-based solution prior to sample's fast loading in the XPS vacuum chamber), samples covered with ~ 3 nm thick Cr layer were prepared for Cr/p-GaN interface characterization. Photoelectron spectroscopy measurements were carried out in an ultrahigh vacuum (UHV) analysis chamber (base pressure $5x10^{-10}$ mbar) equipped with a fast specimen introduction chamber. Unmonochromatized MgKα line at a 1253.6 eV photon energy value was used, as well as a hemispherical electron pass energy analyzer of 100.5 eV, giving a FWHM of 1.2 eV for the $Ag3d_{5/2}$ peak.

5.6.2 Comparison of MOCVD and MBE p-GaN surfaces

As mentioned, nature of O contamination in p-GaN surface prior and after surface treatment should be clarified. In fig. 5.35 (a) and (b), the O1s and Ga3d core level peak emission for the MOCVD sample (TG 574) before (upper) and after (lower) the use of AR treatment are shown respectively. In O1s peak (fig. 5.35 (a)), contributions from three different bond states of O are detected each one fitted with a single peak: a) one at 530.9eV corresponding to O-Ga bonds, i.e. GaO_x phases, b) one at 531.8eV corresponding to O-C due to atmospheric contamination (CO, CO_2) and c) on e at 533.0 eV corresponding to O found in -OH and carboxylic groups. In Ga3d peak on the other hand (fig. 5.35 (b)), there are two different contributions detected: one corresponding to Ga-N bonds and another at ~ 1 eV higher binding energy corresponding to Ga-O bonds. The XPS analysis reveals the existence of O on p-GaN surface prior to any surface treatment, however, from the total amount of O detected on the surface only a small contribution can be attributed to Ga-O bonds, as observed in upper fig. 5.35 (a) and (b); it is not the dominant contribution in O1s peak, while its contribution in Ga3d peak is small, as compared to the Ga-N one (the peak located at ~ 3 eV lower binding energy than Ga-N in fig.5.35 (b) is the N2s emission peak). It seems that most of O detected on p-GaN surface is found in C or OH containing compounds like CO, CO_2 and others found in atmosphere. The latter is supported by C1s emission peak, where contributions from C-O, C=O and C-O=O groups were identified as well. Therefore, air contamination in the MOCVD wafer is mainly consisted of compounds containing both C and O, which are adsorbed on p-GaN surface. Same is the picture in the MBE case as can be seen in fig. 5.36 (a) and (b) for O1s and Ga3d emission peaks respectively. Again, the Ga-O contribution is not the dominant one in O1s peak and is much smaller than the Ga-N one in Ga3d peak. Therefore, the same type of contamination found on surface of the MOCVD wafer also exists on the MBE one before surface treatment.

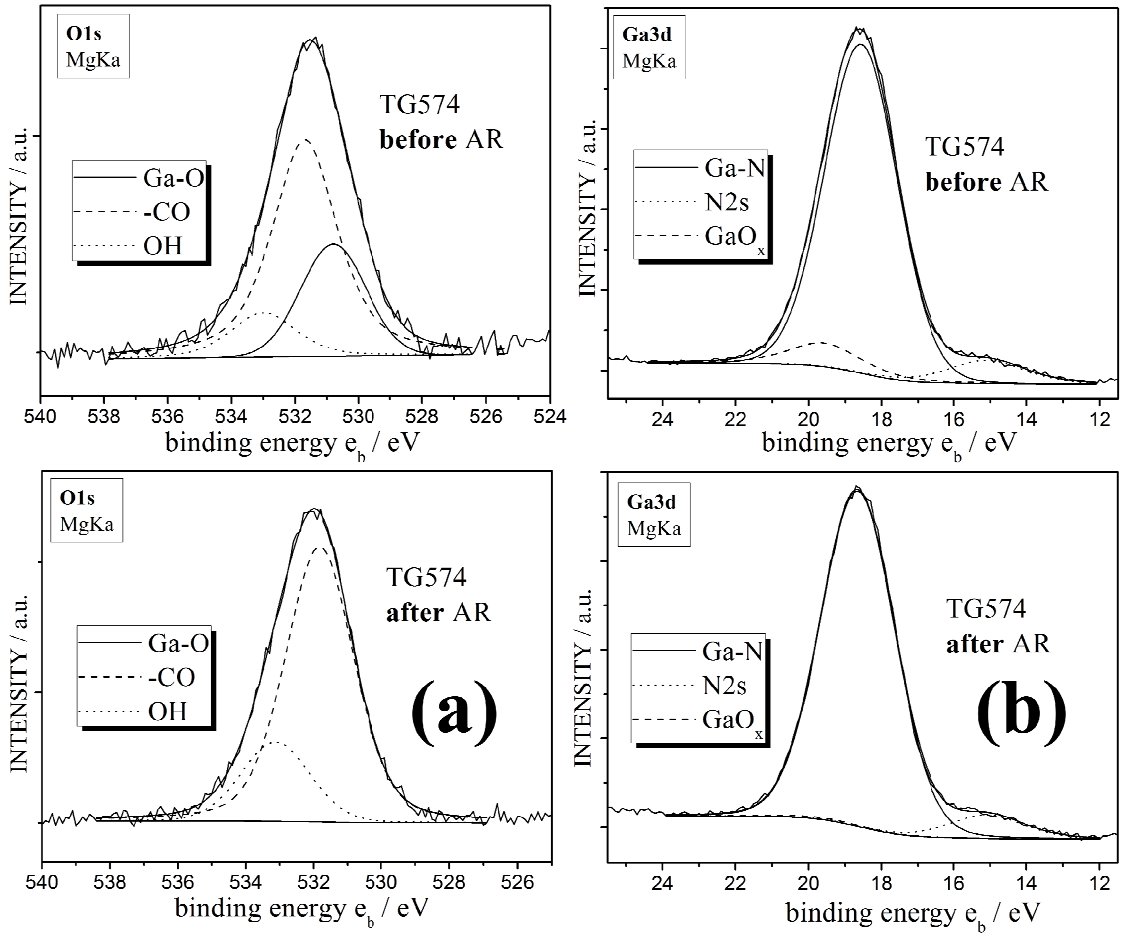


Fig. 5.35 *O1s (a) and Ga3d (b) XPS peaks for the MOCVD sample (TG 574) before (upper) and after (lower) the AR treatment. The Ga-O contributions in both peaks cannot be detected after AR.*

However, if one compares the lower parts of figures 5.35 & 5.36, a different behavior of the two wafers upon AR surface treatment is observed. After boiling AR treatment, Ga-O bond contribution cannot be practically detected in either O1s or Ga3d peaks of the MOCVD sample as opposed to MBE sample, where Ga-O contributions are still detectable, although reduced as can be seen in lower fig. 5.36 (a) and (b). Therefore, it seems that boiling AR is indeed removing GaO_x phases from both surfaces although in the MBE case immersion in boiling AR for 5 minutes didn't prove to be enough for their complete removal, as opposed to the MOCVD case. On the other hand, it might prove that AR cannot remove the remaining oxide phase from the MBE sample. This point calls for further investigation concerning optimized immersion times in boiling AR and/or different combination of chemicals for complete oxide removal from the MBE surface to occur.

Figure 5.37 (a) and (b) shows the XP spectra of N1s peak before and after the AR treatment for the MOCVD and MBE p-GaN samples respectively. For both samples, this peak consists of

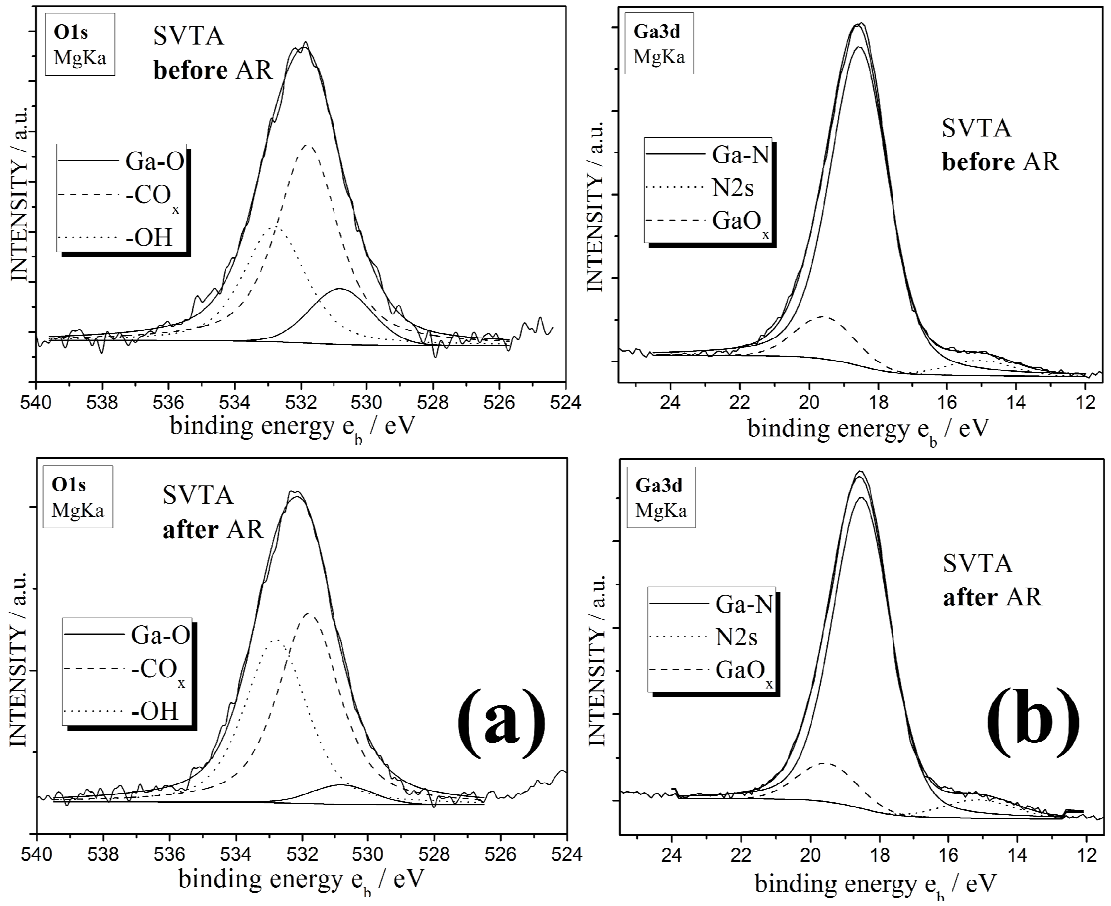


Fig. 5.36 *O1s (a) and Ga3d (b) XPS peaks for the MBE sample (SVTA) before (upper) and after (lower) the AR treatment. The Ga-O contributions can still be detected after AR in both peaks.*

two components: the more intense one corresponds to N-Ga bonds and the weaker one, at 3eV higher binding energy, corresponds to N-O bonds. The chemical state corresponding to this binding energy can be denoted as NO_x, with x<3. It has to be noted that no NO_3^- species were detected either before or after the AR treatment. Before AR treatment (upper spectra in fig. 5.37), the N-O bond contribution is small in both MOCVD and MBE samples. However, a clear enhancement of this bond's contribution in the MOCVD sample after AR treatment is observed (lower spectra in fig. 5.37(a)), whereas this peak remains almost stable in the MBE one (fig. 5.37(b)), as this N-O bond contribution is compared to the N-Ga one in both samples' N1s emis-

sion peaks. N-O bond formation upon the boiling AR treatment is another process, apart from GaO_x removal, which is observed more intensely in the MOCVD sample and makes its behavior diversify from the MBE one. This point will be discussed again below.

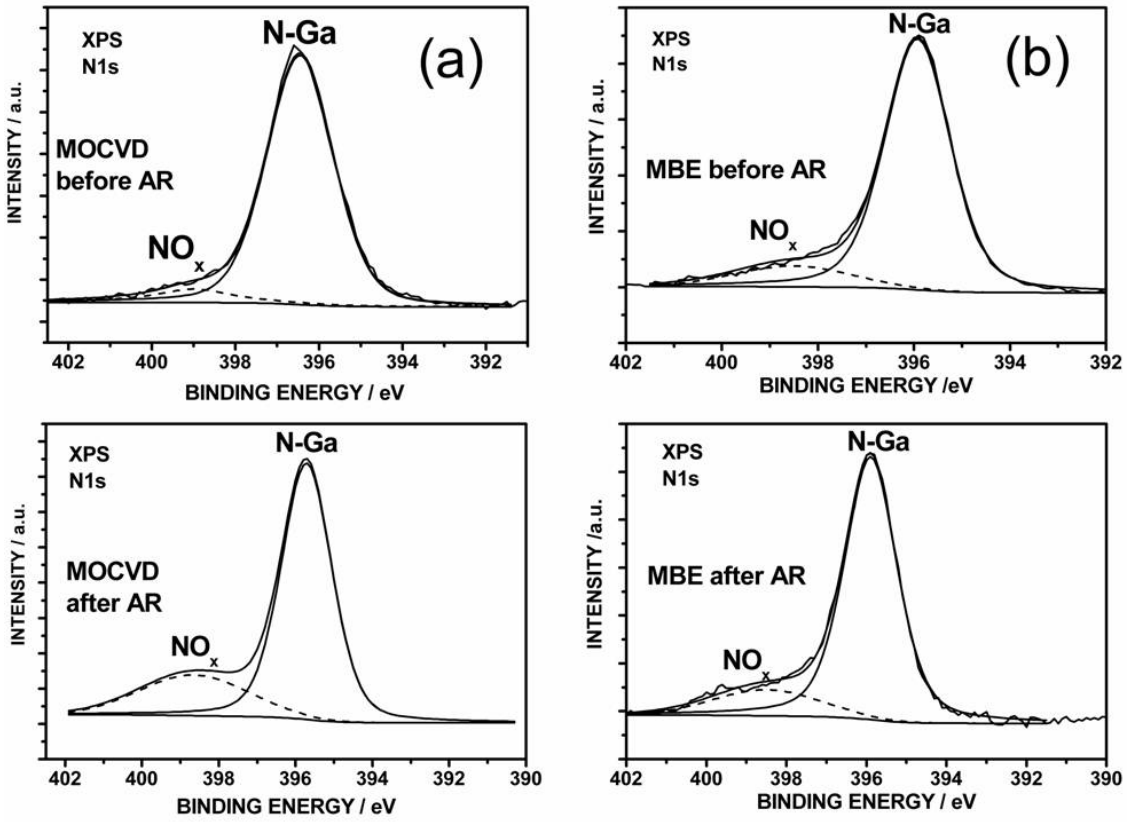


Fig. 5.37 *N1s XP spectra of MOCVD (a)and MBE (b) p-GaN sample before (upper) and after (down) use of boiling aqua regia treatment.*

Assuming that all different elements detected from XPS have uniform concentration inside the analysis volume (defined by the ~ 9 nm depth and the ~ 5x10 mm^2 analysis area), atomic ratio of the various elements can be obtained by integrating the corresponding peaks after subtracting the Shirley-type background, having Ga value as a reference. By area integration of the Ga-N single peak component of the Ga3d and N1s peaks, surface stoichiometry of the two wafers in Ga and N respectively can be obtained. Before the AR surface treatment, the MOCVD material exhibits a Ga: N atomic ratio equal to 1: 0.85, whereas the MBE surface is found to be closer to stoichiometric, since a Ga: N ratio value of 1: 0.91 is obtained in this material. Upon the AR treatment, Ga: N atomic ratio increases in both samples, with the increase being higher in the

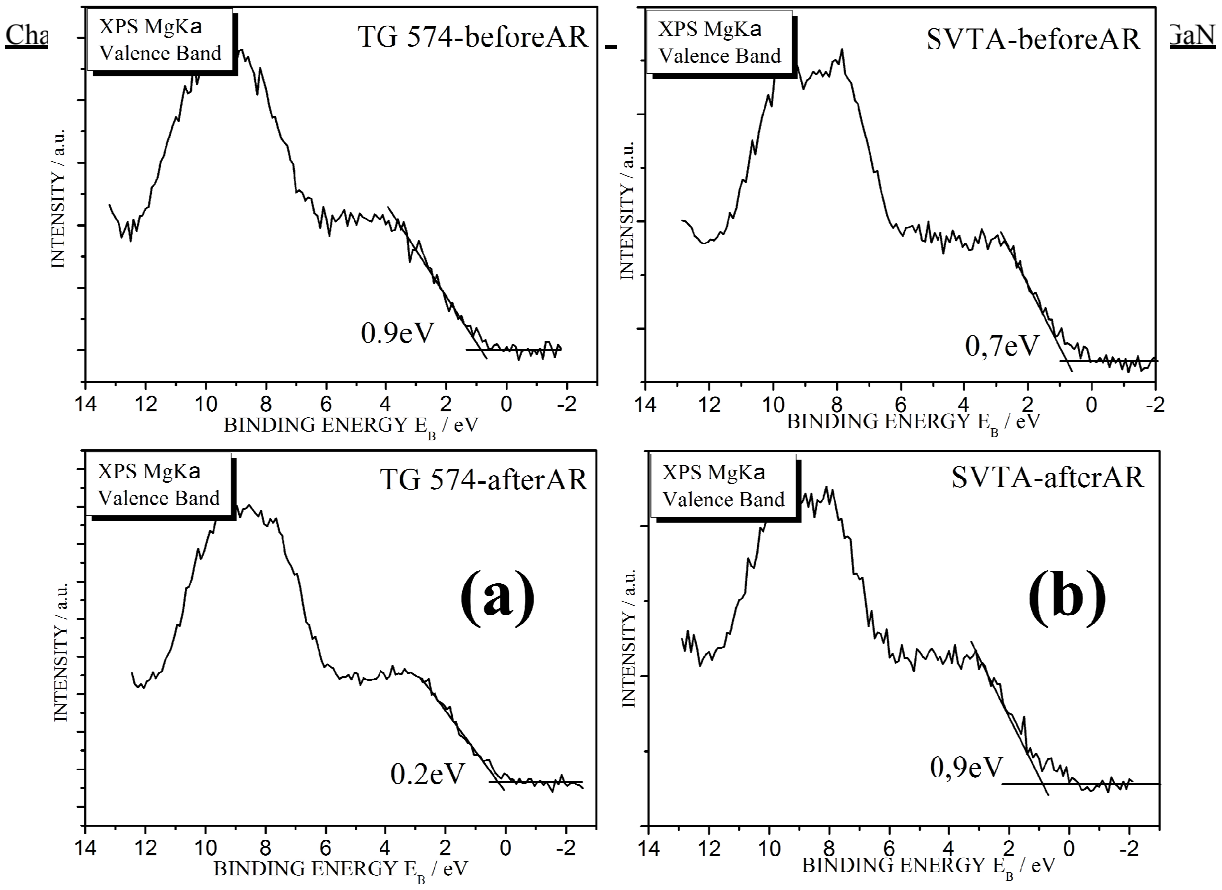


Fig. 5.38 *XP spectra of MOCVD (a) and MBE (b) samples before (upper) and after (lower) AR treatment. A ΔE_F movement of opposite sign is observed for the two samples.*

MOCVD sample (from 1: 0.85 to 1: 0.66), as compared to the MBE case (from 1: 0.91 to 1: 0.85). Therefore, apart from more efficient GaO_x removal from the MOCVD surface, boiling AR treatment seems to also remove more N atoms in this material as compared to the MBE one.

All the above analysis concerning contamination of MOCVD and MBE surfaces, Ga: N ratio value and the way they are affected by the AR treatment should be reflected in Fermi energy level of the surface. For instance, considering the donor-like nature of N vacancies one would expect a Fermi level movement towards mid gap (upward movement) in the MOCVD sample, whereas the same E_F variation, although less intense, is expected in the MBE one. As discussed in 3.4.2, E_F can be expressed via ΔE_F values, which can be determined by samples' XP spectra close to VBM. Such XP spectra are shown in fig. 5.38 (a) and (b) for the MOCVD and MBE samples respectively. From these spectra is evident that the above expected behavior is not observed; ΔE_F of the MOCVD sample decreases by ~ 0.7 eV, while a marginal increase of ~ 0.2 eV is observed in the MBE case. This ΔE_F variation of opposite sign in the two wafers must account for the different p-GaN/Cr/Au contact behavior depicted in fig. 5.34 upon surface treatment.

From the above it is evident that, apart from N loss, other processes take place on MOCVD sample surface, which dominate the Ga: N ratio increase and affect the final position of E_F, in contrast to the MBE sample where the expected behavior is finally observed.

In summarizing the above remarks, a different behavior of the two wafers, in terms of GaO_x phase removal, NO_x formation and E_F movement is observed. In the MOCVD surface, no Ga-O contributions can be detected in neither Ga3d nor O1s corresponding peaks upon surface treatment, while a simultaneous enhancement of the N-O component of the N1s emission peak is observed. Moreover, from the Ga: N ratio increase, it is evident that N atoms are also removed from the MOCVD surface, as is the case for the MBE although in a smaller degree. In the MBE surface, Ga-O contributions can still be detected after the AR treatment in both Ga3d and O1s peaks revealing incomplete removal of native oxide phases from the surface, while the N-O bond component of N1s peak is not affected by AR. It is possible, therefore, that the Ga: N ratio increase in the MOCVD case was partially due to N atoms bonded to O ones and not due to N removal from the surface, which finally resulted in ΔE_F decrease. On the other hand, Ga: N ratio increase is not accompanied by observable enhancement of the NO_x peak in the MBE sample, leading finally to ΔE_F increase in this wafer. The reason for the increased tendency of NO_x formation on the MOCVD surface might be due to larger density of N-related active sites, which in turn means that more crystal and surface imperfections exist on the MOCVD surface[46]. The latter might be able to explain the increased susceptibility of the MOCVD wafer to AR treatment as opposed to the MBE one, which appears to be overall more stable. Nevertheless, boiling AR was found to influence surface properties of the MOCVD wafer, with efficient GaOx phase removal and N-O bonding promotion being two hints towards understanding formation mechanism of the low as deposited Cr/Au contacts.

5.6.3 MOCVD and MBE Cr/p-GaN interfaces

Figures 5.39 (a) and (b) present the XP spectra of Ga3d emission peak for the Cr covered MBE and MOCVD surfaces after AR treatment. By inspecting the two spectra, one can note the symmetric nature of the Ga3d peak in the MBE sample in contrast to the MOCVD case, where the existence of a 'shoulder' at lower binding energies is evident. Consequently, while the photoemission peak of fig. 5.39(a) can be fitted with a single peak centered at 19.1 eV, the photoemission peak in (b) can be fitted only if two peaks are used (each of the same FWHM as the one used to fit the MBE peak): one centered at 19.1eV, which is attributed to Ga-N bond (peak 1), and a second one centered at a 1.4 eV lower binding energy (peak 2), revealing the presence of metallic-like Ga, most probably interacting with metallic Cr to form a Ga-Cr compound[47]. It

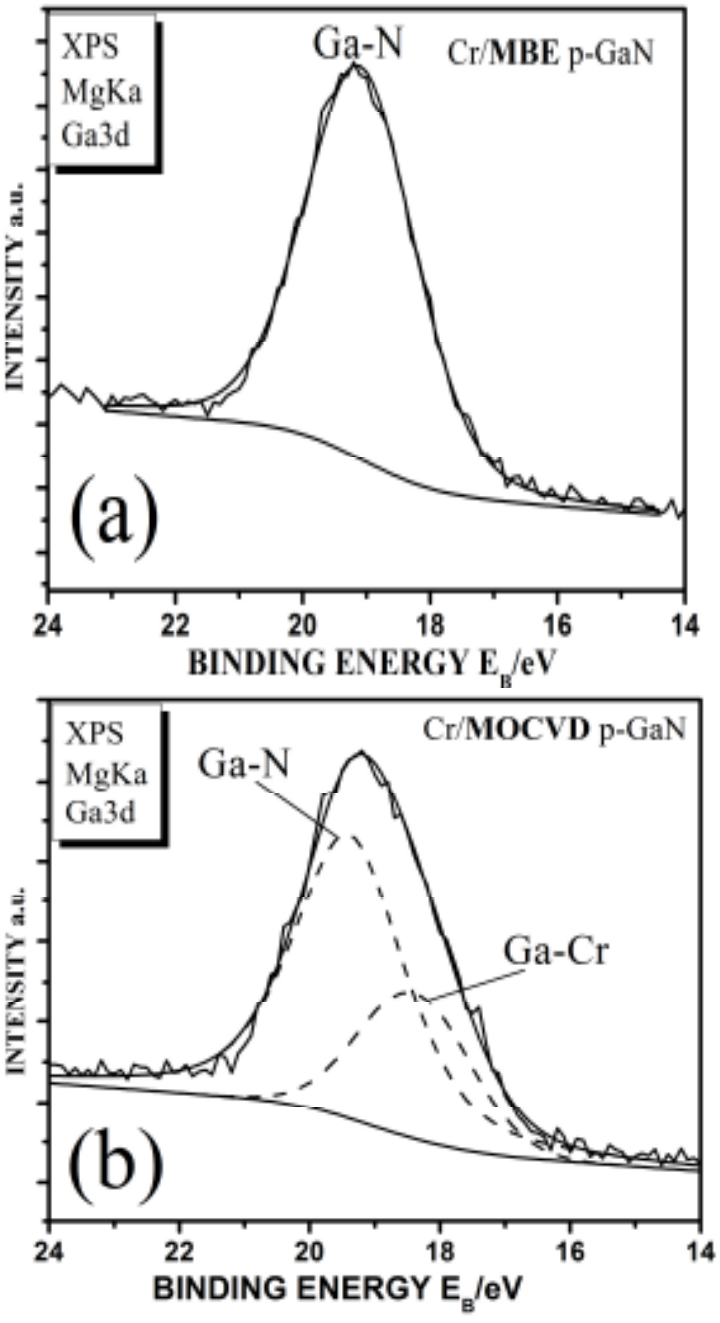


Fig. 5.39 *Ga3d XP spectra of Cr covered MBE (a) and MOCVD (b) p-GaN surfaces. Each fitting curve in (b) has the same FWHM as the one in (a). The asymmetric nature of curve in (b) is clearly seen.*

has to be noted that, this binary phase formation at the MOCVD p-GaN/Cr interface without any heat treatment confirms the high reactivity of Cr.

On the other hand, the Ga-Cr phase is observed only in the MOCVD sample, the surface of which shows increased activity upon AR treatment. As precisely mentioned, the latter removes oxide from our samples surface without removing many Ga atoms (Ga: N ratio increases). As a result, the freshly exposed Ga-related active sites can be very active in forming bonds, either directly with the highly-oriented d-orbitals of Cr atoms, consequently forming the interface Ga-Cr compound, or with other species (for example H_2O molecules from surface treatment or air contamination) which upon Cr layer deposition allow the binary phase formation through Cr gettering properties. Moreover, NOx formation on the MOCVD sample prevents from donor-like states to be introduced at the surface through introduction of N vacancies. In the MBE case, where GaO_x phase is still detected after the AR treatment and Ga: N ratio increase is not accompanied by NO_x phase formation, the Ga-Cr phase is not detected indicating that intimate contact of Cr and surface Ga atoms was not the case. It is clear however, that more work is needed to elucidate this phase formation mechanism.

5.7 Conclusions

In conclusion, the results of a study concerning ohmic contact formation to p-GaN were presented and discussed, with the main remarks being summarized as follows:

First, oxidized Ni/Au contacts on MOCVD p-GaN were studied. The oxidation process was optimized in terms of temperature and duration. Any interface insulating layer present on p-GaN surface prior to deposition inhibits contact performance and has to be removed as pointed out by pre-deposition surface treatment experiments and the results of a two-step deposition and annealing procedure, where enhancement of the insulating interface layer through air annealing of p-GaN/Ni contacts had a devastating effect on contact performance. Overall, oxidized Ni/Au contacts to p-GaN were realized, which can serve as a reference for comparison with results of other metal contacts to p-GaN.

Next, various metals were employed as the contact metal to MOCVD p-GaN. A first finding was that thermal annealing of these as deposited contacts degraded their performance in all cases. Therefore, this study mainly focused on as deposited contacts and in p-GaN surface preparation prior to metal deposition. Moreover, contact performance of as deposited contacts showed no relation to either metal work function or electronegativity differences between metal and p-GaN. To the contrary, the lower resistance contacts were obtained when getter metals are employed as the contact metal. This behavior is attributed to contaminating species adsorbed to the surface, which, if not removed, do not permit direct bonding between metal and semiconductor atoms. Towards this, several pre-deposition surface treatments were tested, with boiling aqua regia (AR) giving the best results in terms of contact resistance, and if combined with Cr/Au deposition, contacts with resistance values as low as 50 Ω can be obtained. However, thorough hydration of the surface after AR and before Cr deposition was found to be necessary for this low resistance contact to be obtained, indicating that H_2O molecules passivate the active sites revealed after AR treatment, preventing re-adsorption of air contaminating species. Cr is a getter metal, able to absorb H (present in MOCVD wafer in the form of Mg-H complexes), O, CO and other contamination from p-GaN surface, while its highly oriented d-orbitals (transition metal) are available for covalent type of bonding with the d-orbitals of Ga dangling bonds and other active sites. This is supported by HRTEM results which indicate local epitaxial growth of Cr on p-GaN. Therefore, the mechanism involved for the low resistance, as deposited Cr/Au contacts to p-GaN

can be summarized as follows: boiling AR is efficient in removing contamination species from the surface, with subsequent hydration being necessary to prevent re-contamination of the surface until Cr deposition. Then, adsorbed H_2O molecules are either desorbed from p-GaN surface during idle time in the vacuum chamber of the deposition system, leaving a large number of active sites for Cr covalent type of bonding with p-GaN surface atoms, or they are absorbed by Cr if still adsorbed on the surface, as is the case for residual O or C contamination

The above proposed mechanism is supported by the results of XPS analysis performed on both MOCVD and MBE p-GaN surfaces, which indicated that O and C related contamination is present on the non treated p-GaN surfaces (both MOCVD and MBE). However, only a small amount of the O related contamination can be attributed to GaO_x in both MOCVD and MBE cases, since the Ga-O bond state contribution is small in Ga3d emission peak and not the dominant in the O1s one, indicating that O related contamination originates from O containing adsorbed species, such as CO, CO_2, -OH etc. Boiling AR is sufficient in removing both Ga-O phases and adsorbed contamination from the MOCVD surface, since no Ga-O contribution in any peak can be detected after AR, whereas still present in the MBE case. Air exposure of AR treated surfaces results in strong re-adsorption of air species in both cases. However, the two types of p-GaN behave differently concerning the influence of AR treatment on surface Fermi energy level, attributed to NO_x ($x< 3$) state formation only in the MOCVD case. Furthermore, examination of the non annealed Cr/p-GaN interface indicated formation of a binary Ga-Cr phase only in the MOCVD case, which might be related with NOx formed during AR treatment and might be able to explain the low resistance, as deposited Cr/Au contact scheme to MOCVD p-GaN.

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CHAPTER 6

Active Region – Quaternary Nitrides

6.1 Internal fields in nitride quantum wells-Quantum Confined Stark Effect

The active region of optoelectronic devices is the region where electrical current is transformed into light and vice versa. For this, spatial confinement of carriers is needed and the way for this to occur is to incorporate quantum wells (QWs) in active regions of LED and LD structures. Modern epitaxial methods, such as MBE and MOCVD, have permitted growth of multilayered heteroepitaxial structures with accurate control of layer composition and thickness, making thus feasible the incorporation of multiple-QWs (MQWs) in the active region of such structures, enhancing in this way emission efficiency and improving performance of LED and LD devices. This is also the case for nitrides, where binary (GaN, AlN, InN), ternary (AlGaN, InGaN, InAlN) and quaternary (InAlGaN) compounds can be grown on GaN/Al_2O_3 substrates by the above mentioned growth techniques, naturally subjected to restrictions related with strain of epitaxial layers and In incorporation in the compounds. Nevertheless, nitride-based heterostructures with abrupt interfaces are feasible, while layer composition, thickness and sequence can influence crystal, electrical and optical properties of the structure, affecting device performance. Therefore, by optimizing structure design and growth, optimized LED and LD devices can be realized.

Nitride LEDs and LDs are characterized by elevated threshold currents, leading to increased operating currents and, as a consequence, reduced device lifetimes. One of the fundamental reasons why nitride optoelectronic devices perform poorly is the presence in the active region of huge polarization fields, of the order of MV/cm[1,2]. It is well known that hexagonal nitrides carry, due to their crystal symmetry, important macroscopic polarizations which can be written in the form $P_{tot}=P_{PZ}+P_{SP}$, where P_{PZ} is the piezoelectric (PZ) polarization which is proportional to the strain applied to the layer, and P_{SP} is the material built-in spontaneous (SP) polarization whose value depends only on the material composition. As a consequence, in most nitride heterostructures there is a non-zero polarization difference ΔP_{tot} at every hetero-interface, generating giant internal electric fields of the order of MV/cm.

Such large fields have profound impact on the optical properties and result in strongly reduced radiative recombination rates and optical gain coefficients through an effect schematically illustrated in fig. 6.1, where a hypothetical GaN/AlGaN QW with (a) and without (b) electric field in the QW layer is sketched. In the absence of internal field, overlap integral of electron and hole wavefunctions is maximized, enhancing radiative recombination rate. However, if an internal field is present inside the QW, the maximum of electron and hole wavefunctions do not spatially coincide due to opposite direction of the force applied on the two kind of carriers, which leads to carrier separation and radiative recombination suppression, as well as a decrease in the transition energy. This effect is the Quantum Confined Stark Effect (QCSE) and apart from crystal defects originating from heteroepitaxy on sapphire substrates is the main reason for the high obtained threshold current values of commercial nitride-based LEDs and LDs. A possible way to reduce or even eliminate internal fields from active region QWs will be discussed in the following section.

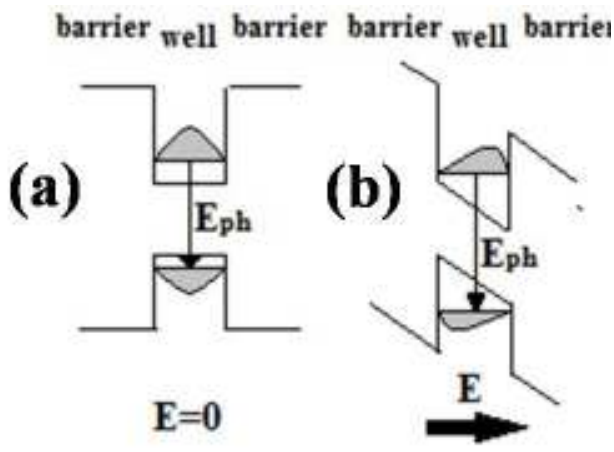

Fig. 6.1 *Schematic illustration of QCSE in QWs.*

6.2 Quaternary nitrides quantum wells-Polarization matching

As seen, the existence of polarization fields inside the QWs of the active region can have a devastating effect on radiative recombination rates and optical gain coefficients, limiting seriously the performance of nitride optoelectronic devices. Polarization fields in nitride heterostructures are eliminated if the condition $\Delta P_{tot}=0$ is satisfied at every heterointerface, under which the polarization field in the heterostructure is strictly zero. As will be discussed below, the only way for the above condition to be achieved in the widely adopted hexagonal c-axis configuration is the utilization of quaternary nitride alloys ($In_xAl_yGa_{1-x-y}N$) in the active region of LEDs and LDs.

Quaternary nitrides (QN) are the alloys consisted of three atoms of the group-III of the periodic table and N. It can be considered as an alloy of the three elemental GaN, AlN and InN binary nitrides with Vegard law giving lattice constant and energy gap of the quaternary alloys:

$$a_{InxAlyGa1-x-yN} = x\, a_{InN} + y\, a_{AlN} + (1 - x - y)\, a_{GaN}$$

$$Eg_{InxAlyGa1-x-yN} = x\, Eg_{InN} + y\, Eg_{AlN} + (1 - x - y)\, Eg_{GaN} - b_{In}\, x\, (1 - x) - b_{Al}\, y\, (1 - y)$$

where b_{Al} and b_{In} are the bowing parameters of Al and In respectively. The bowing parameter of Al has been determined to be ~ 1.0 eV and constant for all Al composition values in the quaternary. For In however, there seems to be a strong dependence of its bowing parameter value on In composition in the alloy, with values up to 4.8 and 9 eV being estimated for <In> ~ 14% and 8% respectively[3]. Nevertheless, the key feature of QNs is the ability to independently define lattice constant and energy gap of the alloy due to the ability of independent <Al> and <In> control, feasible in both MOCVD and MBE growth methods.

In order to better understand the way QN alloys can help eliminate the internal fields present in nitride heterostructures, the SP coefficient of the main binary nitride compounds versus their lattice constant are plotted and shown in Fig. 6.2 (a). Considering a GaN/InAlGaN heterostructure coherently strained on a GaN substrate, it is straightforward to realize from fig. 6.2 (a) that the addition of Al in the quaternary layer generates mainly ΔP_{SP} due to the large difference of the SP coefficient between AlN and GaN, while the addition of In generates mainly ΔP_{PZ} of opposite sign, due to the large increase of the lattice constant resulting in a compressive strain of the layer. Hence, for appropriate combinations of In and Al concentrations in the quaternary alloy

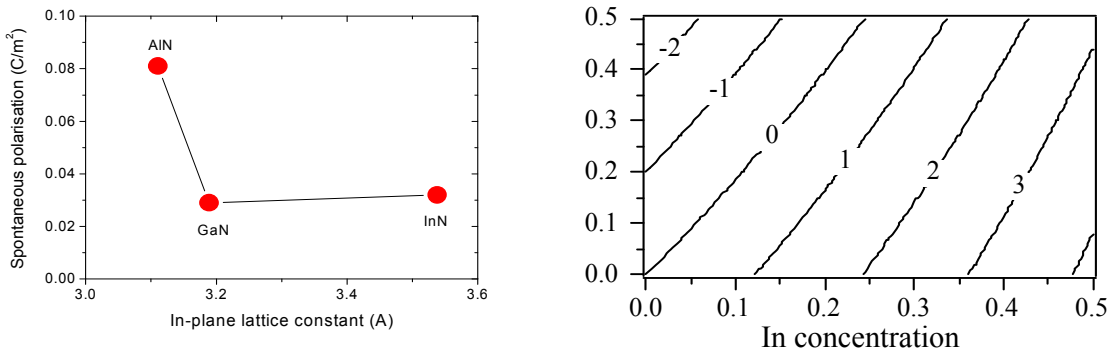

Figure 6.2: *Left (a) spontaneous polarization coefficient versus lattice constant of binary nitrides. Right (b) Iso-electric field curves calculated for a GaN/InAlGaN heterostructure, grown on a GaN substrate, as a function of In and Al concentrations. The electric field values are in units of MV/cm.*

layer it is possible to obtain "polarisation-matched" GaN/InAlGaN heterostructures with zero internal electric field[4,5].

In fig. 6.2 (b), the calculated iso-electric field curves, based on SP and PZ coefficients found in the literature[4] for a GaN/InAlGaN heterostructure grown on a GaN substrate as a function of In and Al concentrations of the quaternary layer are shown. The 0-field curve corresponds to quaternary compositions for which $\Delta P_{tot}=0$ and hence the heterostructure is free of electric field. Moreover, a zero-field condition can be extracted concerning In/Al composition ratio in the alloy for internal-field elimination to occur, which must be close to ½ as can be seen in this graph. Based on such curves, one can design the active region of a nitride LD such that all constituent layers are on a 0-field curve. It remains to be seen if such zero internal field InAlGaN/GaN heterostructures can be grown by MBE.

6.3 Optical characterization results

6.3.1 PL study of QN layers and QWs

All quaternary samples were grown by RF plasma-assisted molecular beam epitaxy (RF-MBE) and details about the growth can be found elsewhere[6]. It has to be noted that, achieving In incorporation in the alloy higher than 10% was not at all trivial, especially since Al has to be in-

corporated as well. This can be attributed to the high desorption rate of InN at temperatures > 600°C, while such temperatures are required for high quality GaN and AlN growth. Also, growth interruptions necessary for substrate temperature lowering when passing from (Al)GaN to InAlGaN layer growth proved to have an effect on QN layer quality. This was the reason for the non-availability of In_xAlGaN with x > 0.1for the initial experiments of this study. Finally, QN growth at the 510-570°C temperature regime was found to be the optimal temperature window for both Al and In incorporation in the alloy, while N flux had been set for stable layer-by-layer growth to be the case. A series of $In_xAl_{0.3}Ga_{0.7-x}N$ /GaN multiple QW samples were grown with x varying between 0 and 0.15 and different layer widths. The alloy concentrations and layer thicknesses were determined by a combination of X-ray diffraction and Rutherford back-scattering experiments on successively grown QN thin film and MQW samples. For comparison reasons, equivalent GaN/AlGaN structures were grown as well, serving as reference structures. The term "equivalent" here means that the bandgap discontinuity between the well and barrier layers are about the same in both structures. For photoluminescence (PL) experiments, a cryostat system with variable temperature down to 17 K, a spectrograph and a UV-enhanced CCD camera for light collection were used. The excitation sources were cw He-Cd and pulsed Nd:YAG lasers emitting at 325 and 266 nm respectively, with pulse width of the latter being 0.5 ns.

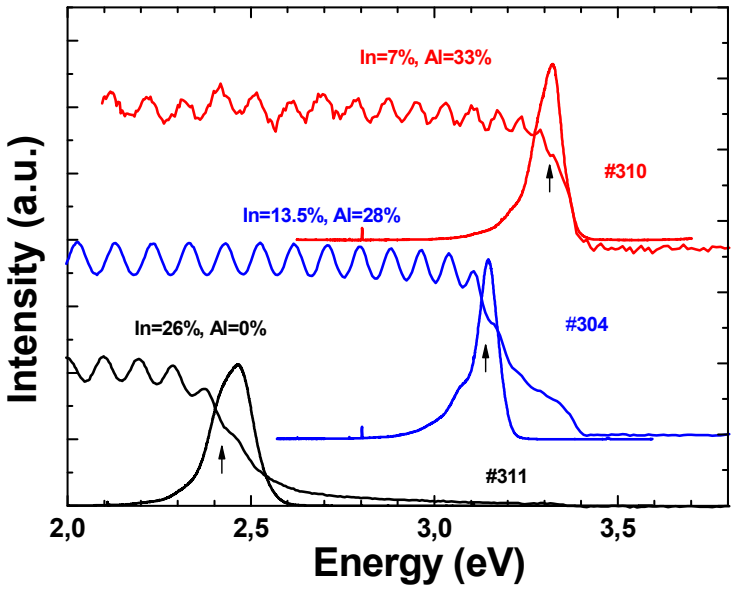

Figure 6.3 *Comparison of T=20K PL and T=300K transmission spectra for three different InAlGaN thin films, whose compositions are indicated in the figure. The upward arrows indicate the energy gap for each film, corresponding to the onset of absorption in the transmission spectrum.*

All QN samples contributed with a corresponding peak in photoluminescence spectra. In order to ascertain the type of transition accounting for this peak, PL must be combined with other techniques due to the complexity of PL spectra, which contain peaks from all possible optical transitions occurring in the sample, depending on the excitation source and detection spectral range. In fig. 6.3, the low temperature PL with room temperature transmission spectra for three

films are compared, whose compositions are indicated in the figure. For each sample, the energy gap at the onset of strong absorption in the transmission spectra is distinguished, marked by an arrow. The near coincidence of the energy gap with the PL emission confirms that InAlGaN films are characterized by strong band-edge emission. Please note that the room temperature PL is red-shifted by about 60meV with respect to the low-temperature peak, which however does not change the above conclusion. Another characteristic of the emission spectra, not fully shown in fig. 6.3, is the absence of any deep-level emission, at least down to 1.9eV**.** It has to be noted the strong dependence of QN bandgap and corresponding PL peak position on In and Al compositions of the alloy, which permits control of QN bandgap by control of alloy composition. This is further supported by the PL spectra of QN thin films of various In and Al compositions shown in fig. 6.4, where emission wavelength ranged from 290 for x, y values of 0 and 0.42 to 430 nm for 0.16 and 0.2 respectively. This is an encouraging result for potential QN use in nitride optoelectronic devices in a wide spectral range for various applications apart from white lightening and dense data storage (sensors, photovoltaics). Another thing to note from fig. 6.4 is that

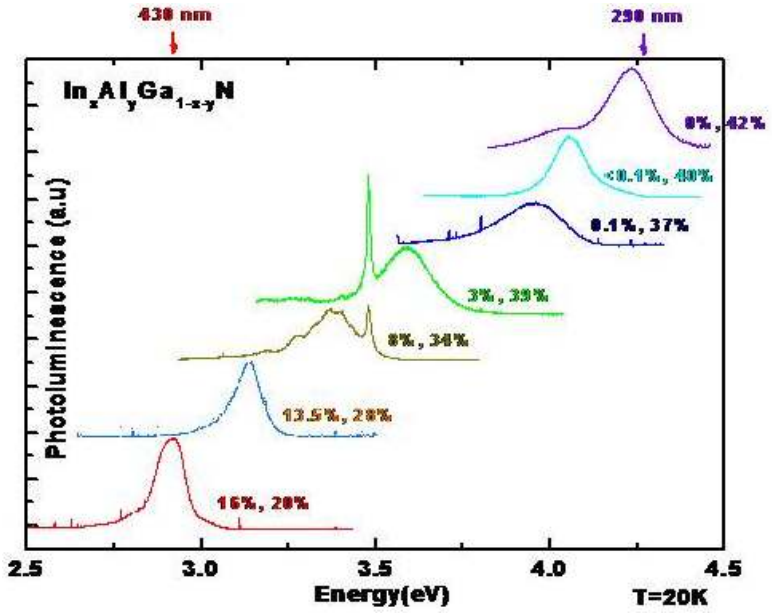

Figure 6.4 *(PL spectra of a series of QN thin films, with various In and Al compositions being determined by RBS and XRD.*

$In_{0.03}Al_{0.39}Ga_{0.58}N$ has larger bandgap than GaN, whereas the opposite occurs in $In_{0.08}Al_{0.34}Ga_{0.58}N$ alloy. The fact that QN constitutes the QW rather than the barrier layer as <In> changes from 3 to 8%, with <Al> being ~ 30%, is related to the large In bowing parameter, an issue that will be discussed in more details below.

Moreover, the PL FWHM values, indicative of the sample crystal quality, of the three samples depicted in fig. 6.3 are 88meV for #310, 65meV for #304, and 127meV for #311. In other words, the narrower PL comes from the ½-In/Al ratio alloy in agreement with the XRD linewidths of the three samples. While the broader PL emission for #311 can be attributed to the partial strain relaxation measured in this sample, it is somewhat surprising that #304 which is coherently strained on the GaN template with a compression of 0.8% exhibits significantly narrower emission than #310 which has near perfect lattice-matching with the GaN template. Since many factors contribute to PL linewidths, clearly more experiments are required to clarify this important issue, although it seems that crystal and optical quality of the films are favoured in the sample with In/Al ratio close to the theoretically predicted "polarization-matching" value of ½ .

The PL intensity variation as a function of temperature gives valuable information on the efficiency of non-radiative (NR) channels in a semiconductor material, and is therefore an impor-

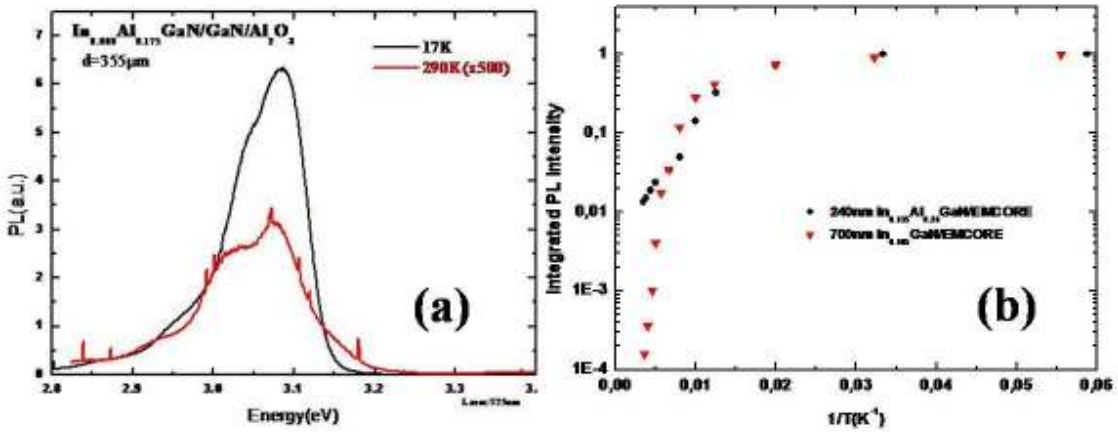

Figure 6.5 *(b)Spectrally-integrated PL intensity versus the inverse temperature for samples #304 (black circles) and #279 (red triangles).The excitation source for the PL spectra of both samples was a cw He-Cd laser line at 325nm.*

tant characterization of its optoelectronic quality. Any deviation from perfect crystal periodicity, like point or any other defect can be considered as NR center. The PL spectra of a QN thin film sample with 9% In and 18% Al taken at two different temperatures are shown in fig. 6.5(a). A reduction of PL intensity as temperature rises from 17 to 290 K by a factor of 1,000 is observed, which is more than satisfying, since QN sample emits even at room temperature indicating that NR processes do not dominate the radiative ones as temperature rises. However, the spectrally-integrated PL peak emission intensity is better to be obtained if safe conclusions concerning NR

centers reduction in QN samples have to be made, since peak intensity alone cannot be so enlightening. The integrated PL intensity as a function of temperature from the InAlGaN film #304, with In/Al ratio close to 1/2 and the ternary InGaN film #279 are compared in fig. 6.5 (b). The InGaN film has a PL peak centred at 3.02eV and a 66meV PL FWHM linewidth, as also has the QN sample #304, therefore a direct comparison of the two sample's optical quality can be made. A main observation from this graph is that the QN-related PL intensity holds much better with temperature as compared to the ternary film, which is a strong indication of reduced NR-channels in the quaternary films of this composition. The above remarks indicate that high quality QN layers can be grown to serve as active region layers of commercial optoelectronic devices operating at room temperature.

After basic PL characterization of QN thin films, a series of QN/GaN QW structures were grown. PL spectra of two samples with 7 periods of $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs differing only in the QW layer thickness, as well as of a thin QN film with same In and Al compositions, are shown in fig. 6.6. A first observation is that the QN layers with <In> and <Al> of 8 and 28% respectively, indeed constitute the QWs of the structure, since the transition energy of the 4 nm InAlGaN/GaN QW is higher than the 8 nm one as theoretically expected. The fact that the 8 nm QW transition energy is lower than the thin film one is a clear manifestation of the QCSE in the 8 nm InAlGaN/GaN QWs, which effect is more intense with increasing QW thickness as predicted from theory. From fig. 6.6, the PL energy position E_{PL} of the two QW structures can be extracted and used for estimating the internal field in this family of QWs. The field-measurement method consists of comparing the PL peak energies of different-width QWs with energy level calculations using the internal field as a variable parameter. The method necessitates good knowledge of the 3D energy gap of the QW material and of the QW widths. Hence, it can be a particularly straightforward method in the limit of binary QWs and large fields. In our case,

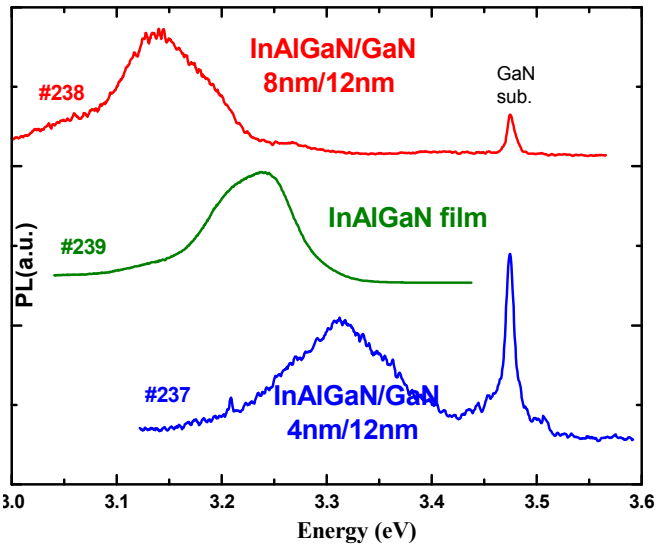

Fig. 6.6 *PL spectra of QN QWs of 4 and 8 nm thickness. For comparison PL from a thin QN film of same composition is shown as well.*

however, of very low fields and the presence of an alloy in the QW, one has to pay special attention to limit down any fluctuation in the alloy composition from one QW sample to another. This is the reason why the QW samples of fig 6.6 were fabricated successively the same day in order to avoid any possible drift of the growth conditions from one day to another and keep the alloy composition in the two samples as identical as possible. It has to be noted that layer thicknesses were again determined by combination of RBS and XRD results.

After the PL peak energy position E_{PL} is extracted from fig. 6.6, the e_1h_1 QW transition energies can be estimated by using the phenomenological equation $e_1h_1=E_{PL}+0.6\Gamma_{inh}$, where Γ_{inh} is the FWHM PL linewidth[7]. In fig. 6.7, the calculated curves corresponding to $\Delta P/\varepsilon\varepsilon_0$ values of

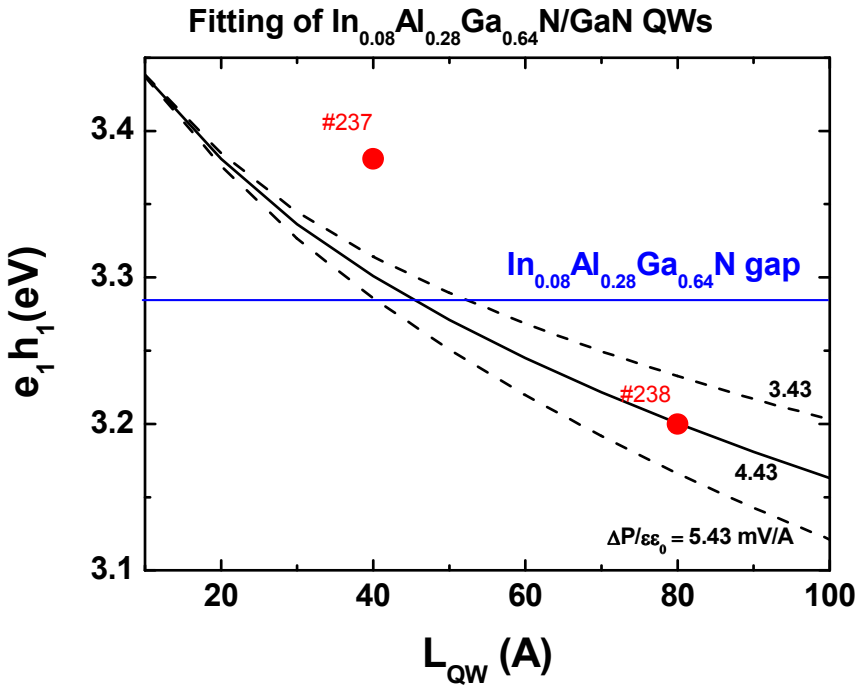

Figure 6.7 *Calculated e_1h_1 energies in $In_{0.08}Al_{0.28}Ga_{0.64}N/GaN$ QWs as a function of well width for various values of internal electric field and comparison with experimental results (red circles).*

3.43, 4.43 and 5.43 mV/Å are shown, as well as the two experimental points extracted from fig. 6.6. As evident from fig. 6.7, the curve that best reproduces the obtained experimental results is the curve corresponding to $\Delta P/\varepsilon\varepsilon_0$=4.43 mV/Å, which is equal to 2.65 mV/Å (=0.265 MV/cm). Despite the non-zero value of the internal field in the QN QWs, it is almost 4 times lower than equivalent (as described above) $GaN/Al_{0.15}Ga_{0.85}N$ QWs, with internal field of the latter estimated to be ~ 1.0 MV/cm[8,9]. Therefore, the possibility of reducing internal electric fields in the active region of optoelectronic devices with utilization of QNs is evident.

As a further verification of reduced internal fields inside QN QW structures, the dependence of QN PL emission on excitation beam power was investigated. PL spectra under various excitation power values of $In_{0.08}Al_{0.28}Ga_{0.64}N/GaN$ and equivalent $GaN/Al_{0.15}Ga_{0.85}N$ QWs are shown in fig. 6.8 (a) and (b) respectively. The excitation power is expressed via the neutral density (ND) filters used to decrease the excitation beam's intensity, with no effect on the beam's spectral distribution, since no absorption occurs inside the ND filters. Excitation power has an effect on carrier concentration levels inside QWs. It has to be noted that carriers are usually excited above the QW maximum, however fast carrier relaxation at the QW ground state (e_1 state for electrons, h_1 for heavy holes) takes place. Excess carriers inside the QW can compensate a

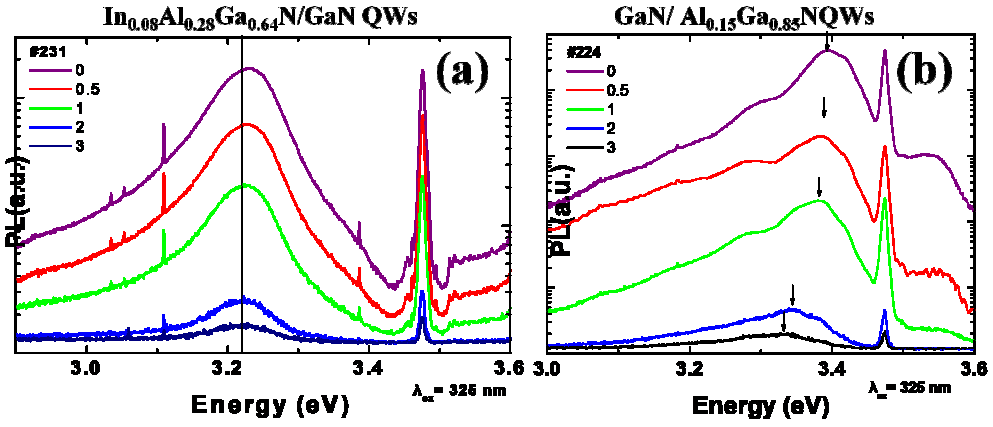

Figure 6.8 *Calculated e_1h_1 energies in $In_{0.08}Al_{0.28}Ga_{0.64}N/GaN$ QWs as a function of well width for various values of internal electric field and comparison with experimental results (red circles).*

non-zero internal field if present, i.e. can compensate QCSE if occurring in a QW. The clear blue-shift of the GaN/AlGaN QWs (~ 50 meV) PL peak energy position observed in fig. 6.8 (b) is therefore indicative of QCSE compensation in the QWs via excess carrier concentration with increasing excitation power and of internal fields present inside GaN/AlGaN QWs. To the contrary, the blue-shift observed with increasing excitation power in the $In_{0.08}Al_{0.28}Ga_{0.64}N/GaN$ QWs is much lower (~ 5 meV) as compared with the GaN/AlGaN case. This is a clear indication of reduced QCSE compensation in the QN case, i.e. indication of reduced internal fields. Despite the fact that In/Al content of InAlGaN layers is not close to the "ideal" ½ value (> 1/3), the results of fig. 6.8 indicate that internal fields are reduced by a factor of almost 4 in the InAlGaN/GaN QWs as compared to equivalent GaN/AlGaN ones.

6.3.2 Field compensated InAlGaN/GaN QWs

A major result of the previous section was that InAlGaN/GaN QWs with ~8% of In and ~28% of Al showed a strongly reduced internal electric field (~0.25MV/cm) in the InAlGaN layer due to improved polarization matching between the InAlGaN and GaN layers[10]. This internal field was about a factor of 4 smaller than that in GaN/$Al_{0.15}Ga_{0.85}N$ QWs. In order to go beyond that preliminary result and reduce even further the internal electric field, InAlGaN/GaN heterostructures with a higher In/Al content ratio in the quaternary layer, which according to some theoretical predictions should be close to ½, should be clearly grown.

As a next step, a series of $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs was grown under different growth conditions in order to optimize the PL linewidth of the QW emission. Reducing the inhomogeneous linewidth of the QW emission is considered vital for laser operation of these QWs since it enhances the optical gain for a given excitation level. In fig. 6.9, the PL spectrum of a sample

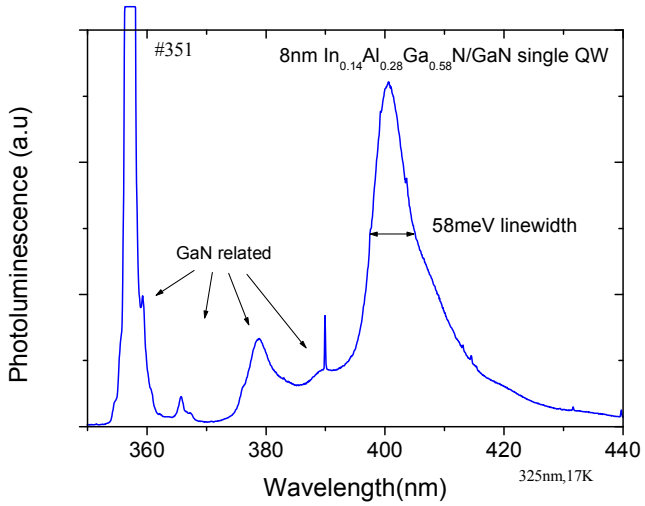

Figure 6.9 *T=20K PL spectrum from a single 8nm-thick $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QW sample #351.*

containing a single 8nm-thick $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QW is plotted. A well-defined peak at ~400nm associated with the QW emission is observed, with the ~58meV PL peak FWHM linewidth being considered rather narrow. () which compares favorably with the smallest PL linewidth observed by us in $In_{0.14}Al_{0.28}Ga_{0.58}N$ thin films (~64meV). Usually in QWs with an In-containing alloy, the effects of interface roughness and In-segregation tend to increase the inhomogeneous PL linewidth beyond that observed in the bulk. In other words, the result of fig. 6.9

seems to suggest that growth conditions of $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs are optimized enough such that the above effects do not play any significant role.

To seek further evidence for the optical quality of the $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs, integrated PL intensity as a function of temperature for three different QW samples: the MQW sam-

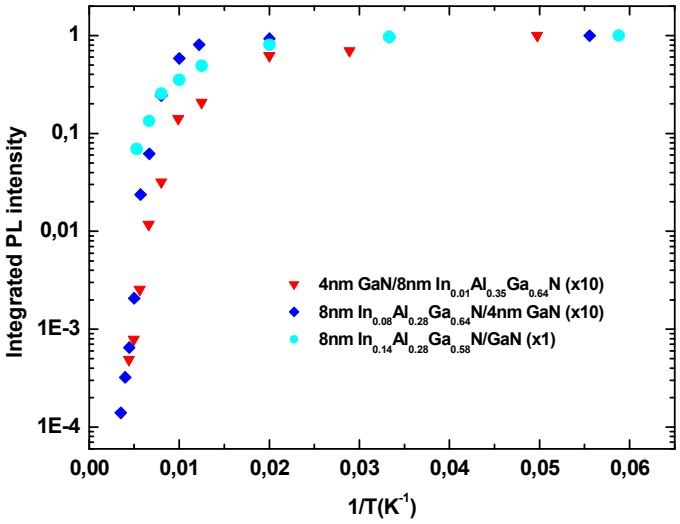

Figure 6.10 *Spectrally-integrated PL intensity versus the inverse temperature for the QW samples #214 (red triangles) with a very large internal field, sample #231 (blue rhombi) with a moderate field, and sample #351 (cyan circles) with an expected nearly-zero field. The excitation source for the PL spectra of all samples was a cw He-Cd laser line at 325nm.*

ple #214 with ten 4nm-thick GaN/$In_{0.01}Al_{0.35}Ga_{0.64}N$ QWs having a very large ~2MV/cm internal field in the GaN QW, the MQW sample #231 with ten 8nm-thick $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs having a moderate 0.25MV/cm field in the InAlGaN QW, and the single QW sample #351 with one 8nm-thick $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QW whose internal field is expected to be nearly zero are compared in fig. 6.10. A first observation from this graph is that the PL intensity of sample #351 holds much better with temperature in agreement with expectations, since the radiative to NR recombination processes lifetimes ratio, which controls the temperature dependence of PL intensity, minimizes for low or zero internal field values.

In order for an estimation of the internal field in $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs, which as pointed out in the introduction should be smaller than the 0.25MV/cm value obtained in $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs, the same procedure as in the previous section is followed. In Fig. 6.11, two $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QW samples of 4 and 8nm QW width, again fabricated successively the same day in order for the two samples to be as identical as possible, are compared. In each sample the PL peak associated with the respective QW is identified, and from its energy po-

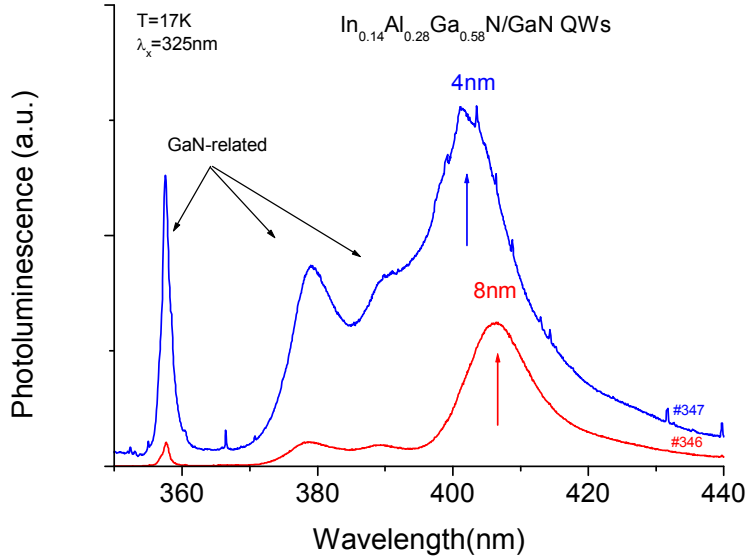

Figure 6.11 *PL spectra from two single $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QW samples #346 (8nm) and #347 (4nm).*

sition E_{PL}, the e_1h_1 QW transition energy is estimated by using the phenomenological equation $e_1h_1=E_{PL}+0.6\Gamma_{inh}$, where Γ_{inh} is the PL FWHM linewidth.

In fig. 6.12, the thus determined e_1h_1 values for the two samples are compared with the calculated e_1h_1 curves as a function of well width for different values of the internal electric field. Again QW layer thickness was determined by combined RBS and XRD analysis. From the com-

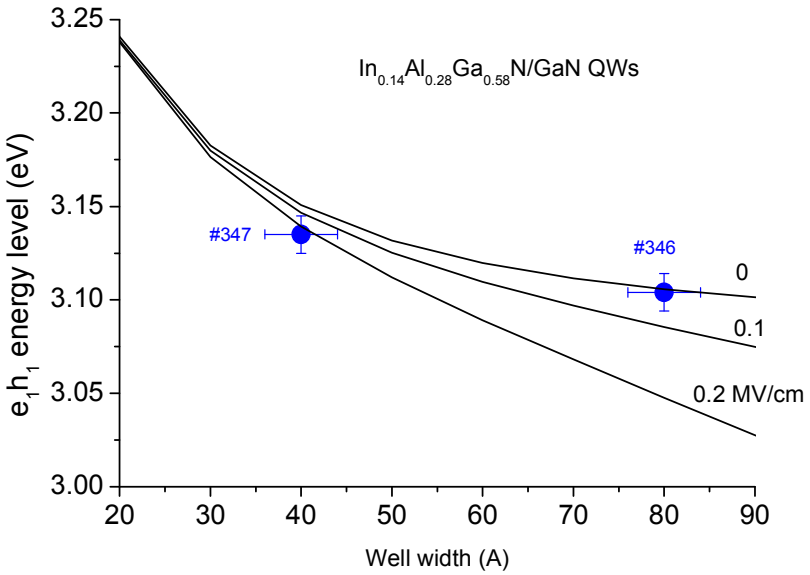

Figure 6.12 *Calculated e_1h_1 energies in $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs as a function of well width for various values of internal electric field and comparison with experimental results (blue circles).*

parison, it becomes evident that the curve that best reproduces the e_1h_1 energy difference (31meV) between the 4 and the 8nm $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs is rather the 0-field curve! For instance, the 0.2MV/cm curve predicts more than 90meV in e_1h_1 difference.

The above result can be unambiguously interpreted as a strong indication of the fact that, increasing the In-content from 8% to 14% brings the $In_xAl_{0.28}Ga_{0.72-x}N$/GaN heterostructure closer to, if not exactly at, the "perfect" polarization-matching condition. Within the accuracy of the experimental determination of the internal field, the $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs can be considered as "zero-field" QWs.

6.3.3 Optical pumping

Encouraged by the reduced internal fields in the $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN heterostructure, a number of quaternary laser structures with these QWs as the active medium were fabricated, in order to examine their lasing properties. Unfortunately, laser structures with InAlGaN QW layers of In/Al ratio close to ½ was not possible to be obtained due to issues related to In incorporation in the alloy, which inhibited growth of QN layers of higher than 8% <In> at this phase of the study. Several reference laser structures with GaN/$Al_{0.15}Ga_{0.85}N$ active QWs have been fabricated

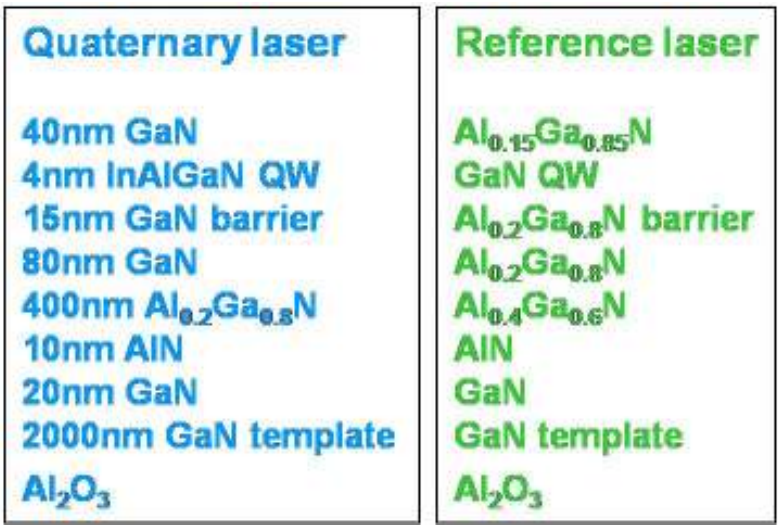

Figure 6.13 *Typical laser structures with InAlGaN/GaN and GaN/AlGaN (reference) MQW active region for optical pumping experiments.*

as well. The dimensions of the cladding layers and the separate confinement region were adjusted to provide efficient wave-guiding with a good confinement factor. Typical laser structures grown for optical pumping experiments are shown in fig. 6.13. The MQW section consisted typically of three $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs embedded in a GaN waveguide. The GaN/AlGaN reference laser structures looked very similar, with the replacement of the InAlGaN/GaN QWs by GaN/$Al_{0.15}Ga_{0.85}N$, the GaN waveguide by $Al_{0.20}Ga_{0.80}N$, and the $Al_{0.20}Ga_{0.80}N$ cladding layer by $Al_{0.40}Ga_{0.60}N$. Optical cavities were then formed on both sample surfaces by utilizing the chloride-based RIE process especially optimized for these experiments employing two-layer PR etch-mask. At the end of the process, the thickness of left-over PR etch-mask was ~ 350 nm, which as seen in section 4.4 is not sufficient for material protection. This fact was later appointed and remedied after optimization of PR etch-mask formation presented in chapter 4.

In fig. 6.14, the results from optical pumping experiments performed at T=300K on a quaternary (#247) and a reference laser structure (#253) are shown, each containing three 4nm-wide active QWs as shown in fig. 6.13. The spectra in fig. 6.14 were obtained from 0.4x0.8mm pads,

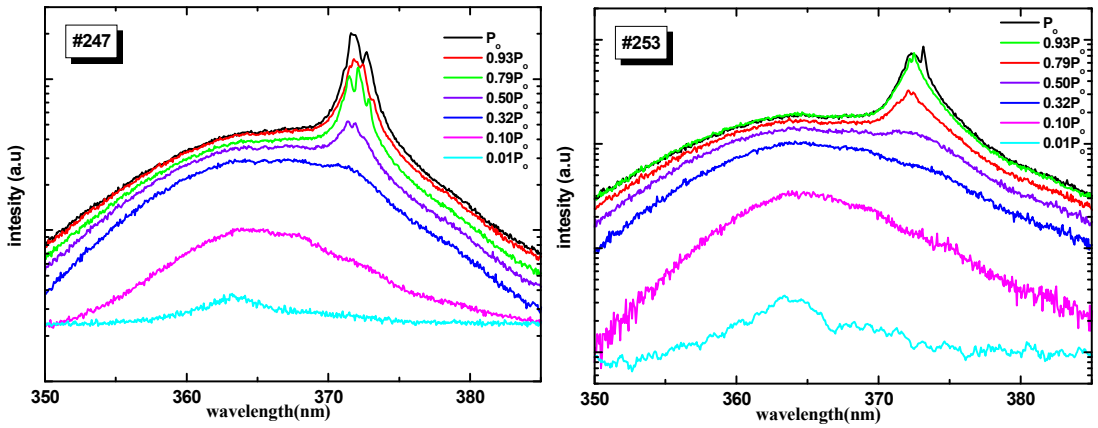

Figure 6.14 *Room temperature optical pumping spectra showing lasing in a quaternary (#247) and a reference (#253) laser structure. In the quaternary InAlGaN/GaN structure lasing begins for optical power between $0.32P_0$ and $0.5P_0$ while for the reference GaN/AlGaN structure between $0.5P_0$ and $0.79P_0$.*

by focusing down to a 0.1mm-diameter spot a 266nm frequency-quadrupled solid state-pumped YAG laser with 0.5ns pulsewidth, 7.6kHz repetition rate and 5mW average power. The maximum transient optical power density that reaches the sample (i.e. after losses in the beam path) is estimated to be around ~10MW/cm^2, and the corresponding photon density per pulse is ~$7\cdot10^{15}$cm^{-2}. Cylindrical focusing of the same laser did not induce lasing in the same samples.

For lasing detection, an optical fiber placed as parallel to the sample's surface as possible, facing at the mesa sidewall, was used in order to favour collection of edge emission. For both samples, sharp lines above a certain threshold power density started to appear, which are indicative of laser action in the active region. A near coincidence (within 0.6nm) of the lasing wavelengths λ_L of the two samples is observed, even though in #253 the lasing occurs from three GaN QWs in an $Al_{0.20}Ga_{0.80}N$ waveguide, whereas in #247 from three $In_{0.08}Al_{0.28}Ga_{0.64}N$ QWs in a GaN waveguide. It has to be noted that for the quaternary sample the threshold power density is between $0.32P_0$ and $0.5P_0$, i.e. distinctly lower than for the reference structure, where lasing appears between $0.5P_0$ and $0.79P_0$.

Even though the threshold power density for both samples is quite high, the quaternary laser structure is characterized by reduced threshold power density for laser action to occur as compared to the reference one. It has to be noted that mesa sidewall roughness was more intense in sample #247 as ascertained by means of SEM and, as a consequence, NR channel density is higher in this sample. Unfortunately, optical pumping of laser structures formed with the optimized mesa formation procedure of chapter 4 was not feasible. Nevertheless, this reduced threshold value for the quaternary sample can be explained in light of reduced internal fields in the active region of the laser structure. In this light, it is safe to expect that QN incorporation in the active region of electrically-driven optoelectronic devices (LDs and LEDs) will benefit laser threshold density values and device performance in general. The above, combined with optimized mesa formation procedure (chapter 4) and low resistance device electrodes (chapter 5), makes feasible the realization of nitride-based optoelectronic devices for commercial use.

6.3.4 Time-resolved PL

Time-resolved PL decay measurements in a selected set a quaternary QW samples with a varying degree of field compensation were run as a further verification of internal field compensation possible with InAlGaN QWs. As a reminder, such measurements can help for determining the QW decay times, i.e. the time needed for carrier recombination in a radiative way (section 3.3.2). As expected, a reduction of the QW PL decay time with decreasing internal field is clearly observed in fig. 6.15, accomplished by adjustment of InAlGaN QW thickness and composition

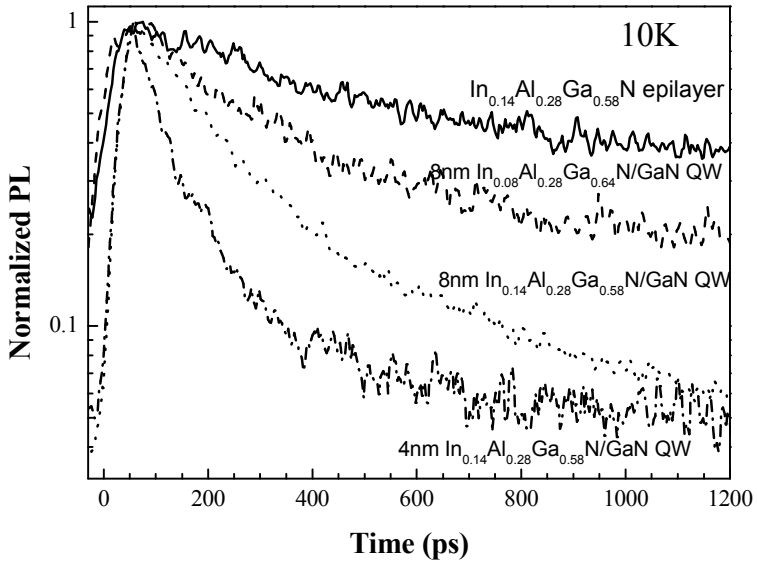

Figure 6.15 *PL decay curves of InAlGaN/GaN QW samples with a varying degree of field compensation.*

closer to the "ideal" In/Al ratio value of ½. By inspecting the graph, decay times of a few hundred of ps are obtained for InAlGaN/GaN QWs at low temperatures, which can turn into a few ns at room temperature. Despite the fact that these decay times are relatively high, they still are 1-3 orders of magnitude lower as compared to those of equivalent GaN/AlGaN QWs[11,8]. Moreover, combined analysis of the decay time and PL intensity versus temperature indicates that low temperature QW PL comes from localized excitons, which begin to delocalize at about 100K. However, present InAlGaN/GaN QW samples suffer from significant non-radiative channels, exhibiting at room temperature non-radiative times of a few tens of ps. One possible explanation for the efficient non-radiative channels in the InAlGaN/GaN QWs is the relatively low growth temperatures (~520^{o}C) of InAlGaN by MBE, which may introduce point defects. Preliminary results suggest that RTA is a promising method to improve PL efficiency of InAlGaN/GaN QW samples. Nevertheless, the significantly reduced PL decay times in quaternary QWs as compared to GaN/AlGaN is a promising result for improved nitride-based optoelectronic device performance, with optimizing further the crystal quality of MBE grown structures being the goal of future work.

6.4 Conclusions

A series of InAlGaN thin films and InAlGaN/GaN QWs of various In and Al compositions were grown on c-axis sapphire substrates. The QN related emission is attributed to strong band-edge recombination, as ascertained from PL and transmission spectra, while PL characterization indicated a strong dependence of QN band gap value on its composition. For the $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs, a reduction of internal-fields by a factor of 4 as compared to equivalent GaN/AlGaN QWs was estimated after fitting of our experimental results with theoretically calculated curves indicating an internal-field value of 0.265 MV/cm. Following the same procedure, the corresponding internal-field value for $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs was estimated to be close to zero as expected from theoretical calculations, which predict zero internal-field in case of In/Al composition ratio close to ½. The reduced internal-fields inside the QN QWs are also indicated by temperature-, power-dependent and time-resolved PL characterization, while optical pumping of laser structures composed of QN QWs in the active region show reduced power threshold values as compared to equivalent GaN/AlGaN structures. The above results indicate that it is possible to obtain lower threshold LEDs and LDs if InAlGaN alloys are incorporated in the active region of such devices.

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CHAPTER 7

Nitride-based devices - LEDs and a novel sensor

7.1 Light Emitting Diodes

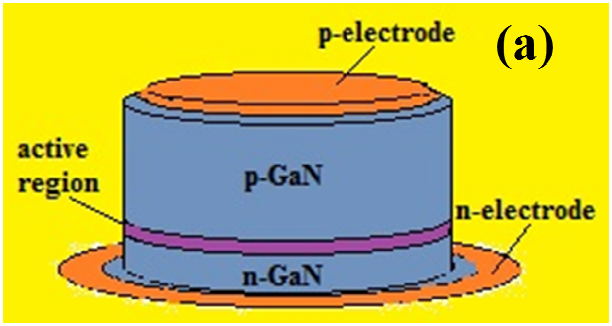
Device realization is the procedure where all technological solutions proposed by the studies conducted in the individual fields are combined and implemented. Towards this, all issues studied so far can lead to improved device characteristics. Although optoelectronic devices with state-of-the-art operation characteristics are difficult to be obtained if drastic improvement in crystal quality of grown structures is not achieved, a comparative study of device performance by employing the technology developed in this thesis is always feasible, as it constitutes the ultimate proof-testing. In this light, while optimizing dry-etching procedure and searching for an alternative low resistance p-GaN ohmic contact, LEDs were fabricated on two wafers provided to us by TopGaN. Despite the proven ability of QN incorporation in the active region of p-i-n diode structures for LEDs and LDs with improved operation characteristics as was shown in chapter 6, the active region of the commercial LED structures provided to us consists of $In_xGa_{1-x}N/In_yGa_{1-y}N$ QWs with bright emission, which is necessary for LEDs realization.

7.1.1 Processing

A schematic of a typical, circular-shaped p-i-n diode as the ones fabricated here is shown in fig. 7.1(a). The p-electrode is formed on the top of the mesa, while the n-electrode is of ring geometry and surrounds the device active area for uniform carrier injection inside the active region of the device, where carrier radiative recombination occurs and. In our case it consists of 5 InGaN QWs and is pointed in the schematic of fig. 7.1(a) as well. The two available LED structures are similar apart from the p-GaN contact layer. In TG 206, the structure of which is shown in the schematic of fig. 7.1(b), p-GaN is ended with a Mg overdoped cap layer, while TG 787 does not have such an overdoped and its nominal thickness is ~ 500 nm as opposed to the ~ 300 nm of TG 206.

A typical full process flow for p-i-n LED device realization is comprised of 5 steps. First, the mesa is formed in order for the device active area to be defined, followed by p- and n- layer ohmic contact formation as the second and third steps respectively. After contact formation, the device can be electrically probed for I-V and RT EL characterization to be performed. The fourth step is dielectric film deposition, which covers the whole device area apart from openings created on the contact metal pads for subsequent deposition of a thick Au interconnect layer. The last two steps allow packaging of devices for environmental protection during operation and storage to be the case, and are mandatory if low temperature EL characterization is to be performed.

In detail, the process flow followed for LEDs fabrication on TG 206 and TG 787 is: a) mesa definition, b) p-type contact and c) n-type contact formation. Mesas of circular shape and various diameters (5-200 μm) were formed by employing the



20 nm GaN:Mg overdoped
300 nm GaN:Mg
20 nm AlGaN:Mg
5 MQW InGaN/GaN:Si
3 μm GaN:Si
1.6 μm GaN
sapphire

(b)

Fig. 7.1 *(a) Schematic of the LEDs fabricated here. (b) Structure of TG 206 wafer.*

optimized, chloride-based RIE process (see chapter 4) using and two-layer photoresist as the etch mask, with more than 1.5 μm PR left, which as seen in 4.4 should be thick enough to protect material underneath. Then, samples having oxidized Ni/Au and as-deposited Cr/Au contacts were prepared for both LED structures. The deposited Ni/Au full p electrodes were formed with e-beam evaporation, lift-off and subsequent annealing at 500˚C for 9 minutes in air. The as-deposited Cr/Au full p electrodes were formed by metal deposition and etch-back, while sample was subjected to boiling AR treatment prior to deposition. After p electrode formation, Ti/Al/Pt/Au deposition followed in all samples for n electrode formation. These contacts were ohmic as deposited, therefore no post deposition annealing was performed, which may be resulting in higher resistance n-electrode than annealed ones. Nevertheless, this study aims in comparing the influence of different p-GaN contact schemes on electrical behavior of LEDs. Moreover, in TG 787 the as deposited Cr/Au contact scheme was also compared with Indium Tin Oxy-Nitride (ITON) material, which have began to attract interest as a candidate p-GaN contact due its high transparency in UV[12]. Also, TG 787 wafer was not delivered thermally activated, thus the three different p-electrodes were formed on two kind of samples differing in the p-GaN activation procedure: the first was activated at 700°C in vacuum for 10 min using RTA, while the second was activated in the MBE chamber at 700°C for 30 min.

7.1.2 Results

A special feature of the TG 206 structure is the Mg overdoped GaN layer that caps the structure, as mentioned earlier which is expected to give better electrical behavior to the device if oxidized Ni/Au contacts were formed on top of it, due to the processes involved during the oxidation of this contact. Upon forward bias, hole injection in the active area of the device was achieved and intense violet radiation was readily obtained as can be seen in fig. 7.2 (a), where a photograph of a 200 μm diameter LED operating under electrical probing. Note that the latter is possible even for the 50 μm diodes without packaging as is apparent from this photo, while for probing smaller diameter diodes, packaging is mandatory. Also, one can notice that emission from top side is blocked by the thick metal p-electrode. This can be remedied if a grid or ring geometry p-electrode is formed on top of mesa, permitting for a larger portion of light to escape from the top. However, contact resistance is increased with decreasing contact area, making the choice of the electrode geometry depend on the final application. The room temperature electroluminescence (EL) spectrum of a 200 μm diameter diode with as deposited Cr/Au p-electrode of grid geometry is shown in fig.7.2 (b), where one can see the dominant emission peak at ~ 385

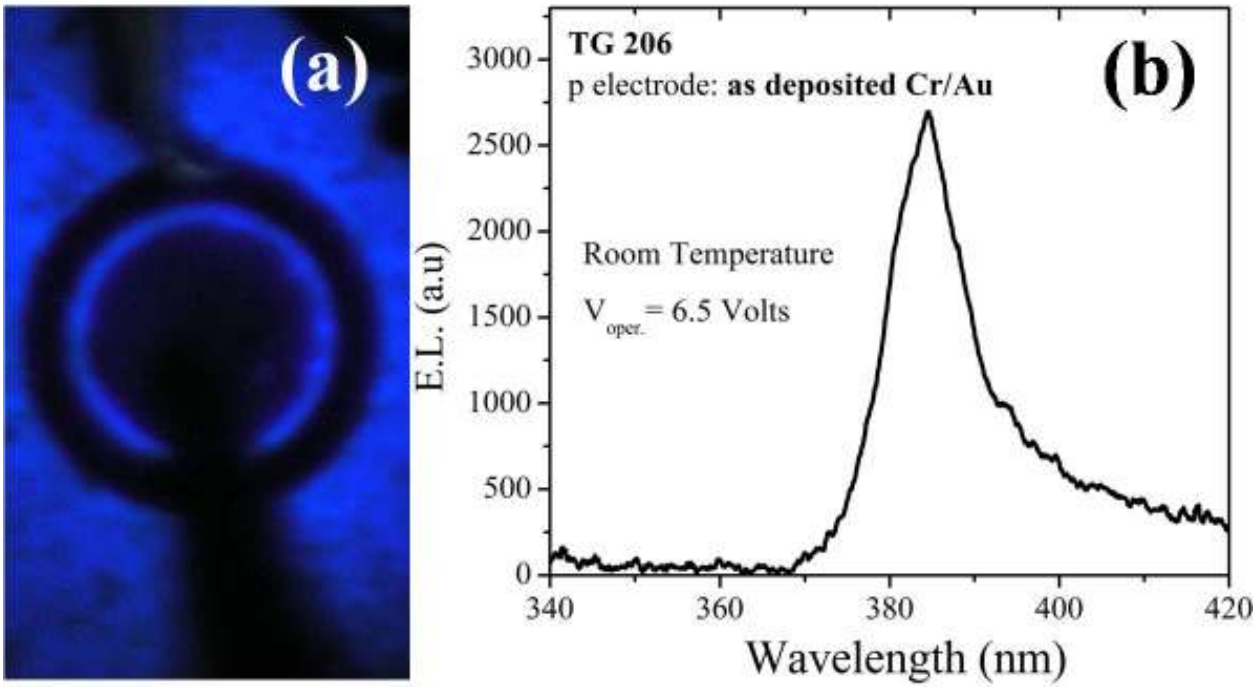


Fig. 7.2 *(a) Emission from a 200 μm diameter LED, where the top p- and bottom, ring n-electrode being clearly seen. (b)Room temperature EL spectrum of a 200 μm diameter LED with as deposited Cr/Au contact as the p electrode. The observed blue emission can be explained by camera's spectral response, since emission is violet as also seen in (b).*

nm.

Corresponding I-V curves of 200 μm diameter diodes with oxidized Ni/Au and as deposited Cr/Au p-electrodes are shown in fig. 7.3. The lower turn-on voltage of diodes with Ni/Au electrode as compared to those with Cr/Au is evident from this graph, while same is the picture for the 100 and 50 μm diameter diodes. Note that p-type electrode is the only difference between the two kinds of diodes. Therefore, the observed difference of ~ 2 Volts in turn-on voltage must be attributed to the different electrode and the processes that accompany each one's formation mechanism. Oxidation of p-GaN/Ni/Au system has a positive effect on electrical properties of p-GaN material through enhanced H removal as discussed in 5.3, with this system being less sensitive to p-GaN material quality as discussed in 5.5.4. On the other hand, performance of the as deposited p-GaN/Cr/Au system seems to strongly depend upon covalent type of bonding between Cr and p-GaN surface atoms and the local epitaxial nature of Cr film, as also discussed in 5.5.4. TG 206 is capped with an overdoped Mg layer, which is expected to have affected crystal quality and homogeneity of surface/ near-surface region of p-GaN, in turn inhibiting performance of the Cr/Au system and LED performance in general[3]. On the other hand, the overdoped Mg layer seems to favor the oxidized Ni/Au system, mainly through improvement of electrical and structural properties of p-GaN layers occurring during air annealing. Unfortunately, the TG 206 sample provided to us for LED fabrication was less than 1/8 of a 2" wafer; therefore a deeper study for Cr/Au contact and LED performance optimization with this structure was not possible. However, it has to be noted the superior behavior of Cr/Au contacts under reverse bias conditions, where diode's breakdown was not observed for voltages up to -18 V, as opposed to the –9 V typically observed for oxidized Ni/Au.

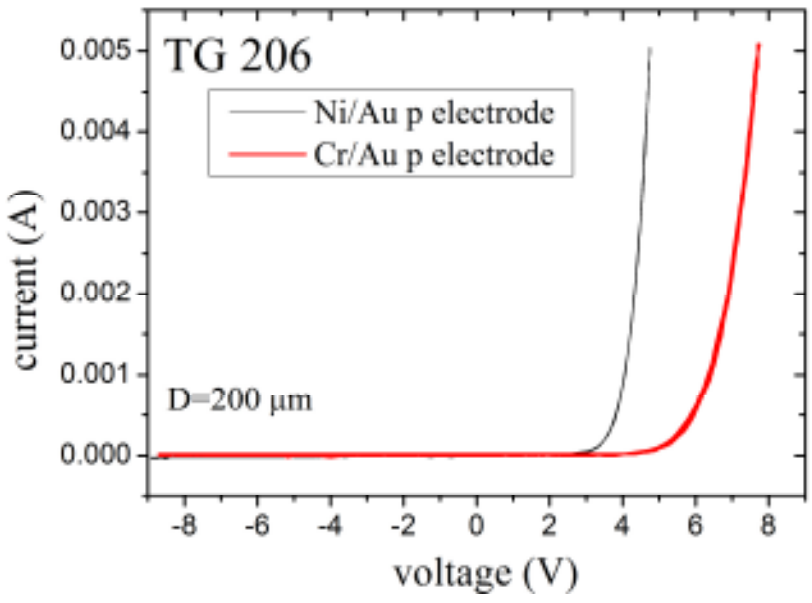


Fig. 7.3 *I-V curves from diodes having Ni/Au and Cr/Au p electrodes. The diodes' diameter was 200 μm. There is a difference of 2 Volts in turn-on voltage.*

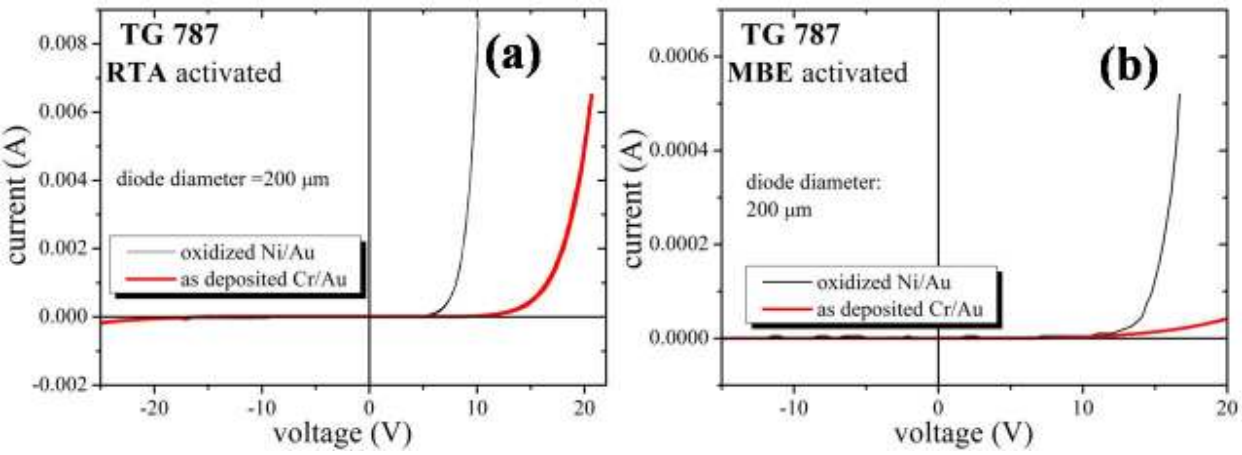


Fig. 7.4 *Characteristic I-Vs from 200 μm diameter LEDs with Cr/Au and Ni/Au p-electrodes in case of RTA (a) and MBE (b) GaN:Mg activation. The better performance of Ni/Au electrodes is attributed to the top Mg overdoped layer.*

Next, LEDs having oxidized Ni/Au and as-deposited Cr/Au p-electrodes were fabricated on two kinds of samples from the same LED wafer TG 787, differing in the activation process as mentioned in the previous subsection. Initially, emission was obtained for diodes of both electrodes and activation processes. In Fig. 7.4 (a) and (b), the I-V curves of 200 μm diameter diodes for the RTA and MBE activated samples are shown respectively. A first observation is that, I-V results of the MBE activated LEDs were worse as compared to the RTA activated ones for similar p-electrodes. This might be suggesting that more sufficient p-GaN activation occurs inside the RTA chamber with its lower vacuum levels and the higher levels of O concentration than in the MBE one where activation takes place in a 5 orders of magnitude higher vacuum ambient. Clearly, LEDs with Ni/Au p-contacts have the best electrical characteristics in terms of turn on voltage as compared to Cr/Au ones. However, the high turn on voltage values of ~6V and ~12V for Ni/Au and Cr/Au contacts respectively indicate that p-GaN activation seems to have been incomplete even in the RTA case. Thus, all samples were subjected to an additional 5 minute vacuum RTA at 700°C in order to improve I-V characteristics of processed LEDs. For LEDs with oxidized Ni/Au contacts this vacuum annealing had devastating results on their performance, since no diode with this electrode emitted afterwards, most likely due to its degradation. On the other hand, I-V characteristics of diodes with Cr/Au electrode were much improved after this annealing, with turn on voltage decreasing by almost 10 V as shown in fig. 7.5 (a) for the sample initially activated with RTA, although still worse than of diodes with Ni/Au electrode before the second annealing. The opposite is the case for diodes on samples initially activated with MBE as

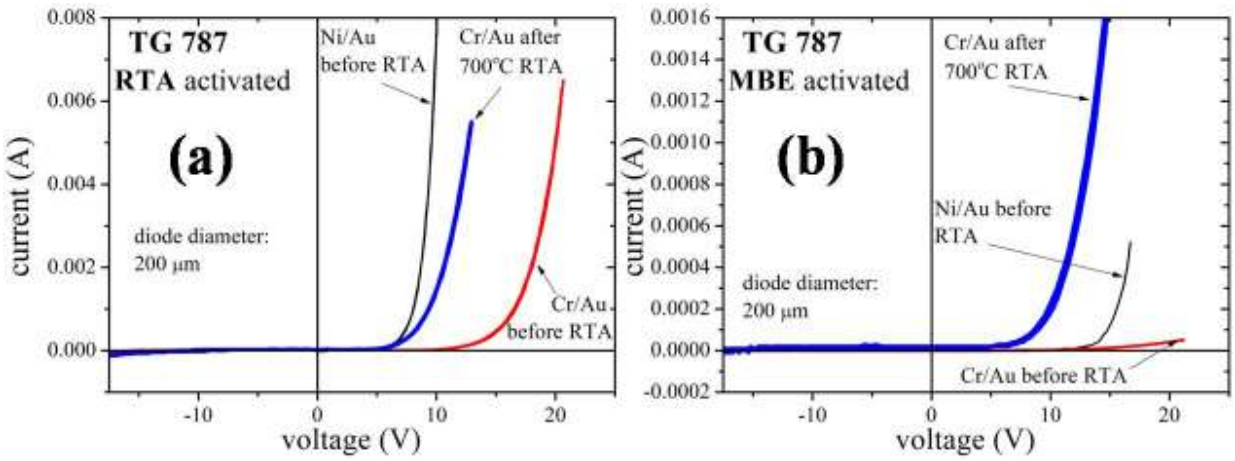


Fig. 7.5 *Characteristic I-Vs from 200 μm diameter LEDs with Cr/Au and Ni/Au p-electrodes in case of RTA (a) and MBE (b) GaN:Mg activation after the additional 700°C annealing. A vast improvement of diodes with Cr/Au contacts is evident.*

can be seen in fig. 7.5 (b), where diodes with Cr/Au electrode after the vacuum annealing are better than Ni/Au were initially. Note that in both (a) and (b) of fig. 7.5, the corresponding I-V curves of diodes with Ni/Au electrode before annealing are shown as well for comparison reasons.

On one hand, the beneficial effect of the 700°C annealing on the performance of LEDs only with Cr/Au p-electrodes might be explained by the combination of further p-GaN activation, which increases hole concentration, and the increased thermal stability of the Cr/Au contact scheme (see 5.5.3) as opposed to the oxidized Ni/Au one, which structurally degrades very easily at temperatures above 500°C. Therefore, it might be electrode degradation responsible for LEDs failure in the Ni/Au electrode case after the700°C annealing. On the other hand, this annealing might have enhanced formation of conducting phases (Cr-Ga or Cr-Ga-N) at the interface, which as seen in fig. 5.39, can improve contact and, in turn, LED performance. Either alone or in combination, the above mentioned facts might be responsible for the totally different behavior of LEDs with different p-electrode upon the 700°C vacuum annealing.

7.1.3 Conclusions

A comparative study of the standard oxidized Ni/Au and as deposited Cr/Au contacts as p-electrodes of LEDs was attempted in this section. In a structure optimized for oxidized Ni/Au

contacts (TG 206), LEDs with Cr/Au p-electrodes were inferior as compared to those with oxidized Ni/Au ones, since a difference in turn-on voltage of ~ 2 V was observed, with a possible explanation being, Mg overdoping-induced p-GaN degradation at the surface/ near-surface region on one hand and, on the other, the beneficial effect of oxidation on electrical properties of Ni covered p-GaN layers. Nevertheless, same was the picture for a structure without the top Mg overdoped layer (TG 787) for both activation processes followed, although RTA activation seems to be more efficient, since LEDs on samples activated in this way showed much better electrical characteristics. Towards complete activation, all samples were subjected to an additional vacuum annealing, which resulted in failure of LEDs with oxidized Ni/Au p-electrodes as opposed to the vast improvement observed in those employing as deposited Cr/Au as the p-electrode. The latter seems to be a good candidate for serving as the p-electrode in nitride-based optoelectronics, since all diodes with this p-GaN contact readily emitted. Moreover, the turn-on voltage difference between LEDs having Cr/Au contacts and oxidized Ni/Au has decreased (even changed sign in the MBE activation case, fig. 7.5 (b)), while diode breakdown was not observed for reverse bias values up to -20 V. Clearly, p-GaN activation process is important for ohmic contact formation and LED performance.

7.2 HEMT on LED sensor for unique sensing applications

III-Nitride-based devices have been rapidly spreading over different fields of applications during the last years. Apart from their use as material for Light Emitting Diodes (LEDs) and High Electron Mobility Transistors (HEMTs), their unique surface properties have made possible the realization of electrolyte- or solution-gate HEMTs and have opened the way for their use in chemical and bio-sensing applications[4,5]. Moreover, the mature growth methods and processing technology of nitrides can give heterostructures with well controlled layer thicknesses and compositions. In this way, new sophisticated devices can be realized for unique sensing applications.

AlGaN/GaN HEMT sensors are based on the gating effect caused by electrostatic interaction between the polar nitride surface and the species, which come in contact with the surface and

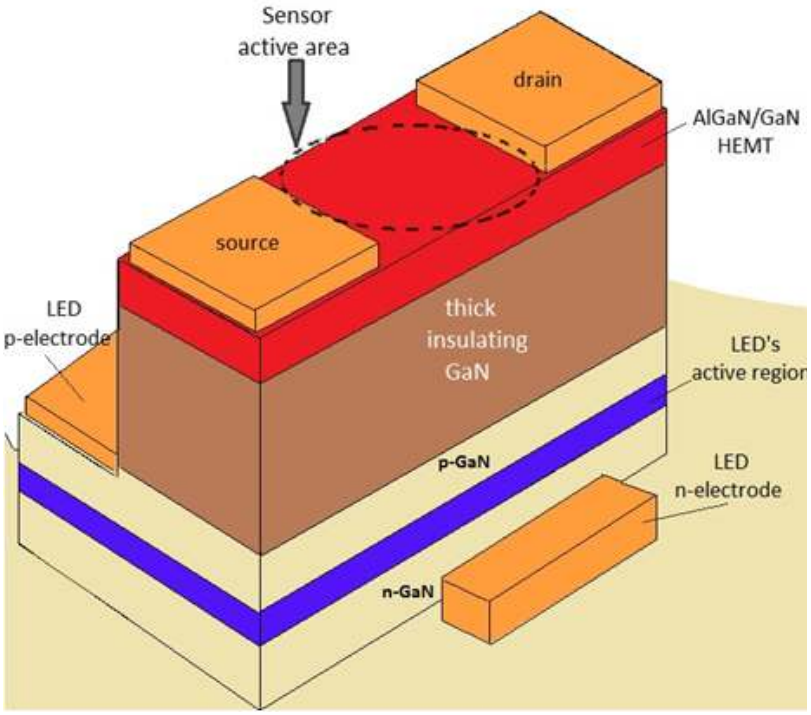


Fig. 7.6 *Schematic of an asymmetric geometry sensor device is shown. In this device geometry, the LED p-electrode is on one side of the HEMT. The active area pointed in the schematic, is the area to be contacting the chemical and/or biological substances.*

finally attach to it, such as ions, radicals or even biological molecules[6,7]. For some sensor applications though, it might be beneficial to use light to catalyze a certain biological or chemical sensing action. The basic idea is the ability to electrically detect, via a HEMT, an important biological or chemical process occurring on the bare GaN surface of the HEMT, which is initiated, enforced or catalyzed by the illumination of light (LED). Therefore, the co-existence of a sensing element (HEMT) and a light source on the same chip might be a powerful tool for unique chemical and biological sensing applications. Toward this end, the most cost- and space-efficient approach is to employ lithographic techniques for the monolithic integration of the two individual devices. A schematic of a device structure, which comprises an LED and a HEMT structure, is shown in fig. 7.6. A thick insulating layer must be inserted in between of the two separate structures for electrical isolation. This can permit the two parts of the sensor device to operate individually. The illuminating wavelength can vary from UV to green, depending on the composition of the quantum wells in the LED active area, while the HEMT's characteristics and sensing ability depend on the growth and composition of the transistor's layers[8]. Therefore, one can tailor material properties and device characteristics to tune the sensor device according to the sensing needs. Nevertheless, there are many technological issues need to be considered, such as growth of the whole structure, processing and light extraction, in order to realize a working device such as the one shown in fig. 7.6.

In the rest of this section, the monolithic integration of an LED with a HEMT for potential sensing use is presented. The main aspects of the design and realization of the device are pre-

sented and discussed. Finally, results about the operation characteristics of the device by means of electrical characterization are presented.

7.2.1 Design

For the realization of the sensor device, growth of the structure and process flow should be considered. Processing of the sensor device is initiated by designing the devices and the corresponding photolithography masks needed for sample patterning at each process step. The processes necessary for realization of the sensor device are: 1) first mesa for HEMT area definition and LED p-GaN layer revealing, 2) second mesa for LED area definition and LED n-GaN layer revealing, 3) HEMT source and drain electrodes formation, 4) LED p-electrode formation, 5) LED n-electrode formation, 6) dielectric deposition and formation of openings for subsequent interconnect metal deposition, 7) interconnect metal pad formation and 8) full coverage with a passivation layer and formation of openings on interconnect metal pads for wire bonding and on HEMT active area for sensing to be possible. It has to be mentioned that the last step is incorporated to ensure sensor device stability and avoid any possible corrosion of device and its parts from the substance tested. Nevertheless, sensing and packaging should mainly be the case, therefore, the only open-to-air areas of the device are the interconnect pads and the sensing area (cyan areas in fig. 7.7). This complicated multi-step process flow can be somehow simplified if one considers that Ti/Al based contacts are utilized for both HEMT source (S) and drain (D), as well as LED n-electrodes, allowing for one-step patterning and metal deposition of these electrodes. Finally, a set of 7 masks was designed for the processing of the HEMT-on-LED sensor devices: 1) first mesa, 2) second mesa, 3) LED p-electrode, 4) HEMT S, D and LED n-electrode, 5) openings on dielectric layer, 6) interconnect metal and 7) openings on passivation layer. As in the LEDs case of the previous section, realization of the first four steps are enough for electrical characterization of the sensor devices to occur.

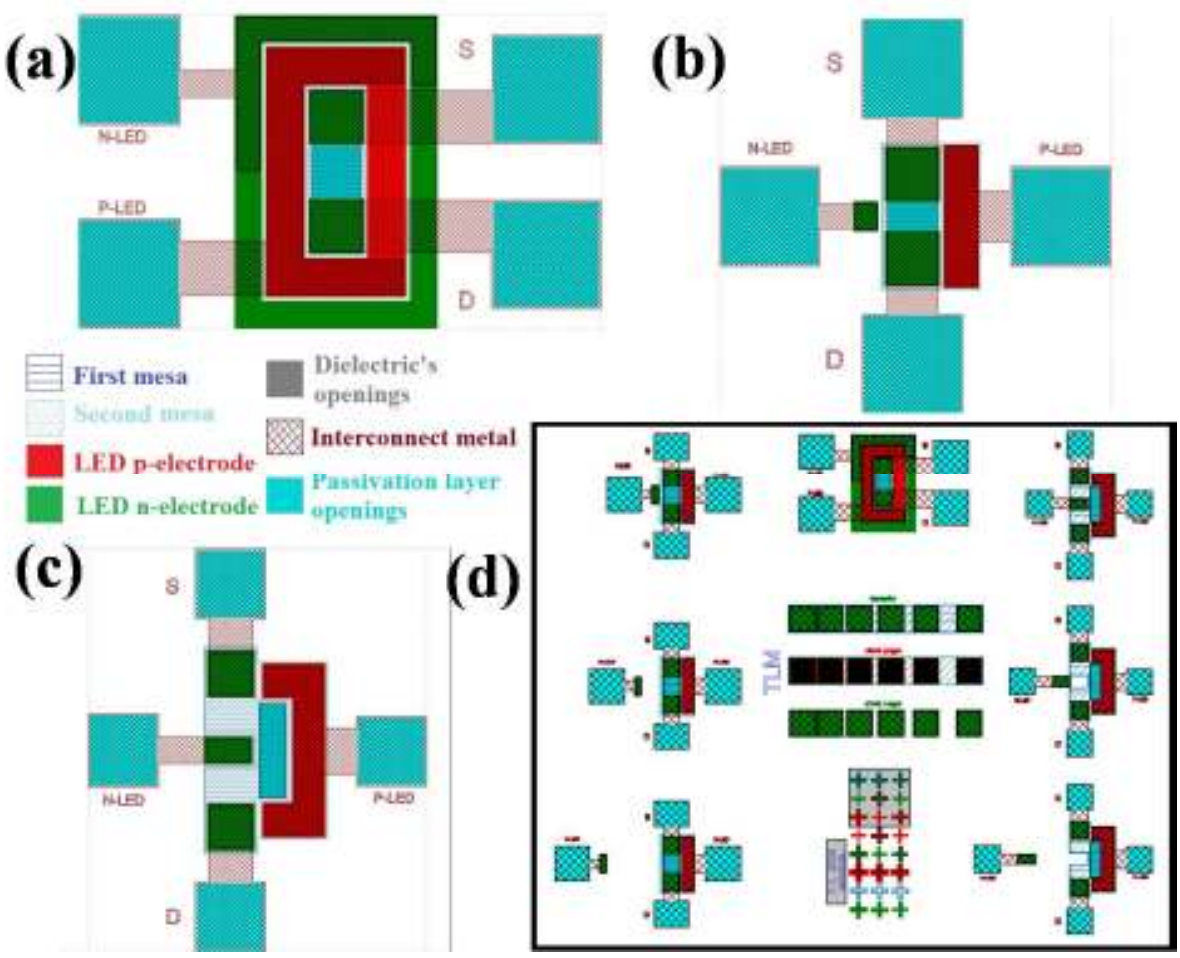


Fig. 7.7 *Symmetric (a), asymmetric (b) and π-geometry (c) devices. A full period with all available device geometries and sizes are shown in (d).*

Concerning design of the devices, rectangular shapes as the one depicted in the schematic of fig. 7.6 were chosen. The most basic device geometry incorporated in the design is the symmetric one depicted in fig. 7.7 (a), which has LED n- and p-electrodes fully surrounding the HEMT. The second geometry is the asymmetric one depicted in fig. 7.7 (b) and is the one resembling the most to the device schematic of fig. 7.6. The symmetric device geometry is expected to promote more uniform carrier injection in LED active region and better electrical behavior due to the larger area of the full-rounded LED electrodes, especially of the p one. However, carrier recombination is expected to occur mostly in the QWs beneath the p-electrode, since electron mobility is much higher in the n layer than that of holes in the p layer of the LED. In this light, the asymmetric devices are expected to permit light emission closer to HEMT active area, i.e. the sensor active area. Based on the need of enhanced light extraction closer to the active area of the transistor, the idea of also incorporating devices of π geometry was realized, with this device geometry

shown in fig.7.7 (c). Also, trying to take into account the much higher mobility of electrons, three devices of the asymmetric and π geometry were finally incorporated, having the LED n-electrode at three different distances from the p one. Due to dimension issues though, it was not practically feasible to take this effect into full account. Finally, each mask period contains 7 devices (3 asymmetric, 3 with π geometry and 1 symmetric), as well as linear TLM patterns for the transistor and LED's n and p ohmic contacts. A schematic of one period is shown in fig.7.7 (d). Which geometry serves the sensing purposes better, remains to be evaluated after actual sensing experiments.

Concerning growth, the HEMT structure was grown on top of the LED structure TG 787 discussed in the previous subsection. HEMT structure consists of a 220 nm thick $Al_{0.29}Ga_{0.71}N$ barrier capped with a 2 nm GaN layer. This AlGaN/GaN HEMT structure is optimized for utilization in anion potentiometric sensors[9]. For electrical isolation a GaN insulating layer of 1 μm thickness, was grown in between of the two structures. Prior to MBE overgrowth, p-GaN was activated with the MBE process discussed previously (700°C for 30 minutes in UHV). A schematic of the structure is shown in fig. 7.8. Characterization of the overgrown structure by means of electrochemical C-V profiling revealed the existence of 2-D electron gas at the AlGaN/GaN interface, indicating that MBE growth of the HEMT structure on top of the MOCVD grown LED one was successful. This was also obtained in a totally MOCVD grown structure (same structure as above), as well as PL emission from the LED structure. Overall, from growth point of view the HEMT-on-LED structure, with the two structures electrically isolated, seems to be achievable.

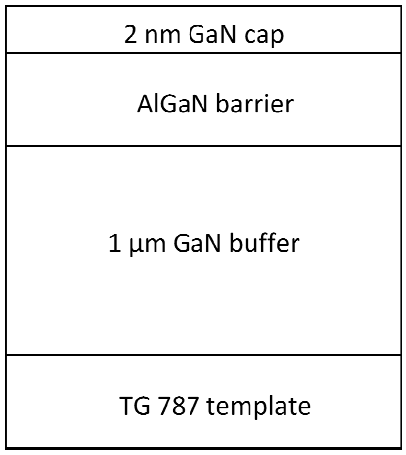


Fig. 7.8 *Schematic of the overgrown HEMT structure.*

7.2.2 Device realization

The first process flow employed for realization of the sensor devices is as follows: a first etching process of ~ 1.4 μm depth was performed to define the transistor's area and reveal the LED's p-type layer for metal contacting. Next, a second etching step of ~ 0.6 μm followed to

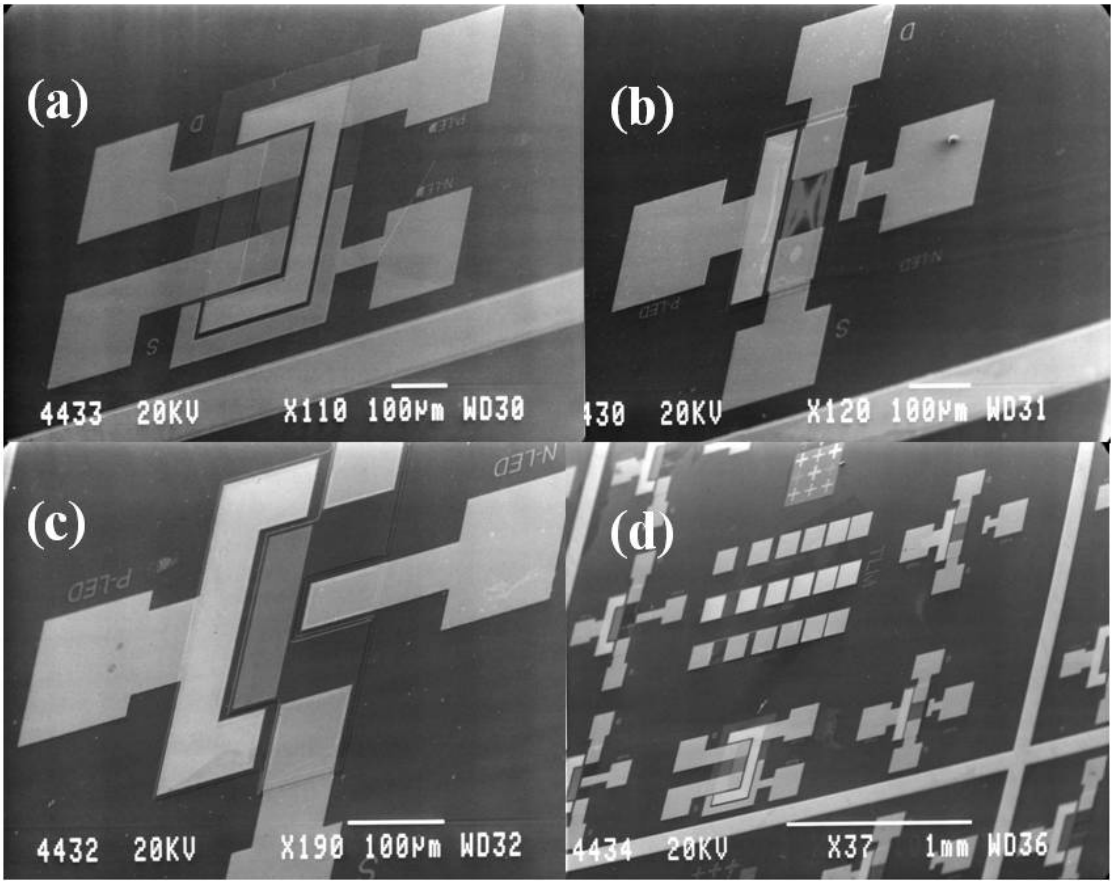


Fig. 7.9 *SEM pictures of realized symmetric (a), asymmetric (b) and π-geometry (c) devices, as well as of a full period (d).*

define the LED area and reveal the n-type layer. Both mesas were performed with a conventional RIE system, using chlorine-based chemistry and two-layer photoresist as the etch mask, following the process optimized in chapter 4. In situ control of the etching depth was achieved by using a laser interferometry system, which is crucial especially in the first mesa step. In both etching steps the PR left after RIE was more than 1.5 μm, in order for the sensor's active area underneath to be protected from ion damaging[10]. Then, ohmic contact metals were deposited; Ni/Au as the p-electrode of the LED and Ti/Al/Ni/Au as the n-electrode of the LED and S- and D-electrodes of the transistor. The oxidized Ni/Au contact scheme was chosen as the p-electrode of the LED, based on two previous observations: a) oxidation might be beneficial for p-GaN layer's conductivity enhancement and b) sensitivity of as deposited Cr/Au contacts on surface quality of p-GaN, which must be affected after RIE. Therefore, the p-electrode formation preceded that of n-electrode, since oxidation might harm Ti/Al/Ni/Au contacts if already deposited. The above considerations hold even if as deposited Cr/Au contacts are used, since a long pre-deposition boiling

AR surface treatment will be required. After deposition of Ti/Al/Ni/Au, contacts were not thermally treated, as opposed to the standard 750°C vacuum annealing procedure for n-GaN, S and D contacts to become ohmic. Whether this annealing step is necessary or not for the operation of sensor device will be discussed below in more details. Next, a 0.3 μm thick SiN dielectric layer was deposited with the PECVD method, which was subsequently patterned and etched with RIE to form openings on the metal pads and the active area of the transistor. After this step the sample was patterned for a thick Au layer deposition to form interconnect pads. Scanning Electron Microscope (SEM) pictures of almost fully processed symmetric, asymmetric and π geometry sensor devices are shown in fig. 7.9 (a), (b) and (c) respectively, while a period with all available device geometries can be seen in fig 7.9 (d). For realistic sensing experiments as mentioned earlier, there is the ability to cover the entire surface with polyamide, or any other layer that remains intact to the chemical substances to be tested, and create openings only in the active area of the transistor and the interconnect pads for probing and wire bonding, respectively. The results of this process flow on electrical properties of the HEMT and LED parts of the sensor device will be discussed below, as well as alternative process flows.

7.2.3 Process Flow optimization-Results

A main objective of sensor performance evaluation is the ability for independent operation of the LED and HEMT parts of the device. This was the case as readily observed, which permitted for separate electrical characterization of the two parts of the device. Typical I-V curves of the LED part of asymmetric and π- geometry devices are shown in fig. 7.10 (a) and (b) respectively, realized following the above described process flow. As a reminder, there are three available distances of the LED n-electrode from the mesa sidewall (see fig. 7.7(a)) in these two device geometries, i.e. distance of the n-electrode from LED active region. As evident from these plots, the n-electrode distance does seem to affect diode performance of both geometries, with devices having the n-electrode 330 μm far from mesa sidewall of the device showing better electrical behavior than those with n-electrode placed at 30 or 130 μm far. Therefore, it seems that the large difference between mobility of electrons and holes can be, even partially, balanced by the larger distance of the n-electrode from the LED active region as compared to the one of the p-

electrode (3 μm from mesa sidewall). I-V curves of all different geometries are shown in fig. 7.10 (c), with asymmetric and π-geometry curves corresponding to devices with the most remote n-electrodes. Among the three, I-Vs from π-geometry devices are somewhat better than those of symmetric and clearly better than those of asymmetric geometry. This observation confirms the importance of p-GaN contact geometry to the diode performance, where the larger p-electrode width and area through which holes are injected into the active region area of the π-geometry as compared to that of asymmetric devices makes the difference. The basic difference, concerning the p-electrode, between the two geometries is the contact. The reasons why symmetric device I-Vs are not the best among the three are still not well understood. Overall, the rather moderate LED performance in terms of high turn-on and relatively low reverse breakdown voltage values is evident in all cases. However, the LED structure on top of which HEMT structure was overgrown is the TG 787 of the previous section with p-GaN activated inside MBE, where the best obtained turn-on voltage value was ~ 6 Volts in the best cases. Moreover, LEDs intensively emitted in the violet as can be seen in fig. 7.11, where a biased π-geometry device emitting is depicted. This is an inspiring result, if one considers that the LED p-electrode is formed on plasma exposed p-

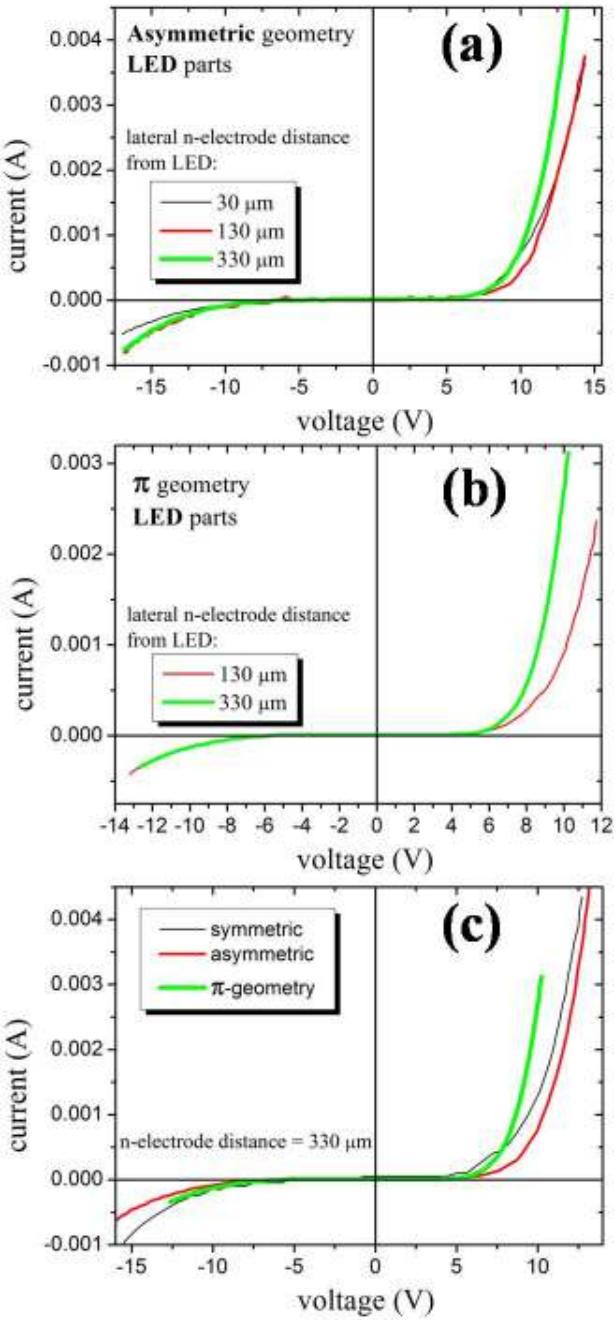


Fig. 7.10 *Characteristic I-Vs from the LED parts of asymmetric (a), π-geometry (b) devices for the three different n-electrode distances from active region. The best results are obtained for the most remote n-electrode. I-Vs from all geometry devices (c).*

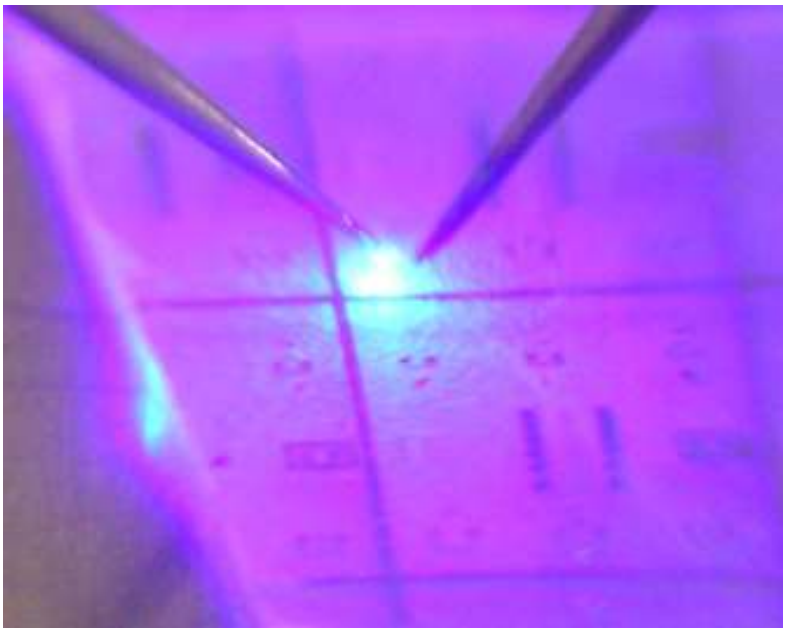


Fig. 7.11 *LED part of the sensor device emitting under forward bias. Violet emission can be readily observed. The camera used here is not the same with the one used in fig. 7.2.*

GaN surface during RIE, which might result in a surface suffering from N deficiency (hole compensating centers), etch byproducts coverage and possible lattice defects, affecting the contact and device performance. Note here that, p-GaN surface exposure to plasma occurs during the first etching step and cannot be avoided. Moreover, fig. 7.11 indicates that a large fraction of the light emitted must be illuminating the sensor's active area, fulfilling the initial expectations for potential use of such devices as integrated chemical sensors that use UV light.

Concerning the HEMT part of the devices, typical I-V curves from all the different device geometries are shown in fig.7.12. From that plot one can see the abnormal shape of I-V curves indicative of the rather bad HEMT performance. Since a 2-D electron gas has been detected at the AlGaN/GaN interface it must be another reason for the obtained HEMT performance. Actually, this result was rather expected since the typical procedure for forming Ti/Al/Ni/Au ohmic contacts to GaN involves thermal annealing at ~ 740°C. This is also supported by

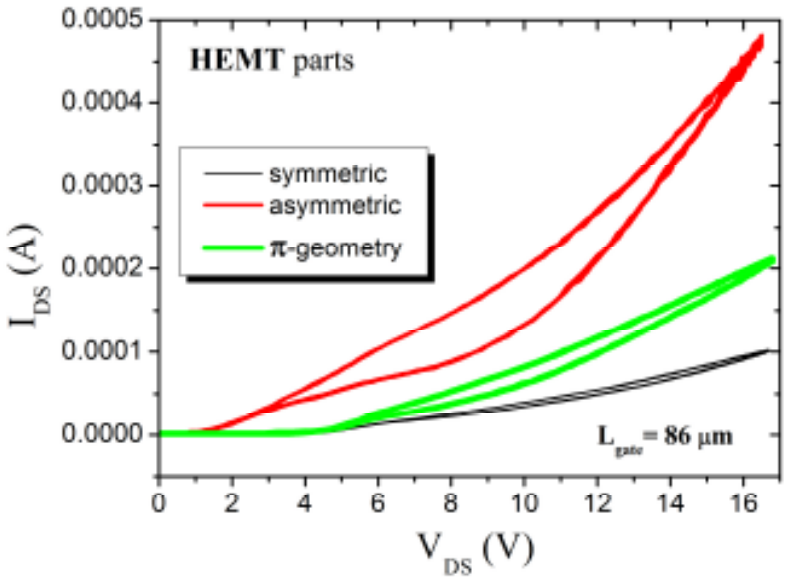


Fig. 7.12 *The poor quality of the HEMT parts of the sensor devices fabricated following the first process flow is apparent.*

TLM measurements, through which the non ohmic character of the S and D electrodes was ascertained. It has to be noted that, the same contacts were ohmic as deposited in the n-GaN case, as was also the case for the LEDs of section 7.1. Upon annealing of the devices at 740°C HEMT contacts became ohmic and a clear improvement in HEMT performance was observed. However, annealing had a devastating effect on the LED part of the devices, since no UV emission was able to be obtained by any device after annealing. The reason for this might be the oxidized Ni/Au contacts to p-GaN, since there are issues with their thermal stability, which can lead to LED failure as also observed in subsection 7.1.2. On the other hand, the same results were obtained when as deposited Cr/Au contacts were used as the p-electrode; in most cases LEDs stopped emitting after the 740°C annealing, with the few devices that both HEMT and LED parts operating most probably being related to circumstantial Cr-Ga phase formation. Unfortunately, the existence of such intermetallic phase at the Cr/p-GaN interface was detected after this study had been conducted, thus no systematic work towards this direction was done. Nevertheless, the above described process flow initially employed needs to be optimized.

Numerous experiments followed for optimizing process flow of the sensor devices in order for both parts of their to be satisfyingly operating. All different combinations in the deposition sequence of LED n- (HEMT S-, D-) and p-electrode were tried, as well as the time when the 700°C annealing step is applied. Finally, the depicted in fig. 7.13 (a) and (b) I-V curves for LED and HEMT parts of the devices respectively were obtained. The process flow followed for these results is: after the two mesa steps a long boiling AR step is utilized for removing any surface insulating layer possibly comprised of adsorbed air contaminating species and/or etch byproducts. Then, the Ti/Al/Ni/Au metal scheme was deposited followed by a 700°C annealing for HEMT S- and D-electrodes to become ohmic (instead of a 740°C). Next, the sample was patterned for LED p-electrode metal deposition, with samples being subjected to a 60” boiling AR surface treatment step prior to metallization. It has to be noted that, no emission from LEDs could be obtained if oxidized Ni/Au are used as the p-electrode in the above process flow, with oxidation being the last step. From fig. 7.13 (a), the rather good quality of the diodes is evident, in terms of both turn-on and breakdown voltage values, with the π-geometry device achieving a lower turn on voltage value (~ 4.5 Volts), as compared to the asymmetric one (~ 5.5 Volts). I-Vs from symmetric devices were not included in this graph, due to poor electrical characteristics and the fact that these devices were not emitting. From fig. 7.13 (b), a clear improvement of the HEMT part performance in this process flow can be observed, as compared to the one depicted in fig. 7.12 for the first process flow. Nevertheless, one can see that the quality of the transistor is

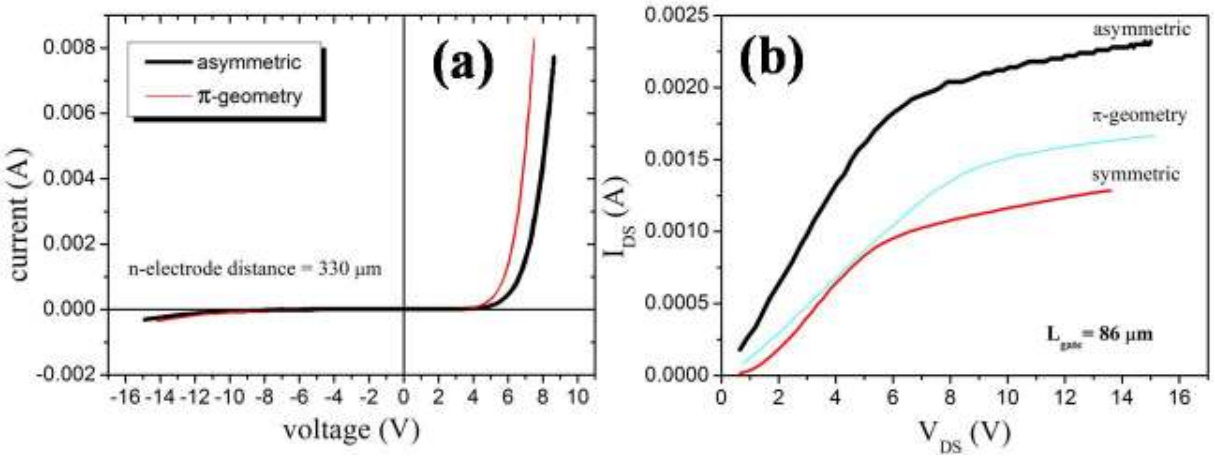


Fig. 7.13 *Characteristic I-V curves of the LED (a) and HEMT (b) part of the devices fabricated with the optimized process flow.*

still moderate, which can be partly attributed to the fact that the S and D metal contact resistance might not be as low as if annealed at 740°C. However, this may not be an obstacle, considering that anion and/or pH sensitive HEMTs utilize the linear part of the transistor I-V. It has to be mentioned that an alternative process flow that yields similar results as the ones depicted in fig. 7.13 is the following: first, the Ti/Al/Ni/Au contact scheme is deposited on bare surface corresponding to HEMT S-, D- and LED n-electrodes and after the LED n-electrodes are removed (by covering S- and D- electrodes using the 1st mesa photo mask and subsequent immersion in HF to remove metals from LED n-electrodes), the 700°C annealing takes place. Then, the two mesa steps follow and after post-RIE immersion in boiling AR, the p-electrode metals are deposited. In case of Ni/Au contacts, oxidation takes place before LED n-electrode formation, whereas if as deposited Cr/Au contacts are used, no annealing step is performed. Finally, as deposited Ti/Au can be used as the n-electrode, which were ohmic as ascertained from TLM measurements. Note that this process flow is the only among the ones followed that oxidized Ni/Au contacts can be used as the LED p-electrode and emission to be the case.

7.3 Conclusions

A comparative study of the standard oxidized Ni/Au and as deposited Cr/Au contacts as p-electrodes of LEDs was attempted in this section. In a structure optimized for oxidized Ni/Au contacts (TG 206), LEDs with Cr/Au p-electrodes were inferior as compared to those with oxidized Ni/Au ones, since a difference in turn-on voltage of ~ 2 V was observed, with a possible explanation being, Mg overdoping-induced p-GaN degradation at the surface/ near-surface region on one hand and, on the other, the beneficial effect of oxidation on electrical properties of Ni covered p-GaN layers. Nevertheless, same was the picture for a structure without the top Mg overdoped layer (TG 787) for both activation processes followed, although RTA activation seems to be more efficient, since LEDs on samples activated in this way showed much better electrical characteristics. Towards complete activation, all samples were subjected to an additional vacuum annealing, which resulted in failure of LEDs with oxidized Ni/Au p-electrodes as opposed to the vast improvement observed in those employing as deposited Cr/Au as the p-electrode. The latter seems to be a good candidate for serving as the p-electrode in nitride-based optoelectronics, since all diodes with this p-GaN contact readily emitted. Moreover, the turn-on voltage difference between LEDs having Cr/Au contacts and oxidized Ni/Au has decreased (even changed sign in the MBE activation case, fig. 7.5 (b)), while diode breakdown was not observed for reverse bias values up to -20 V. Clearly, p-GaN activation process is important for both ohmic contact formation and LED performance.

Moreover, a novel nitride-based sensor, monolithically integrating an LED and a HEMT, is designed and realized. A study concerning process flow optimization resulted in achieving operation of both LED and HEMT parts of the devices in a satisfying level, with the first showing good performance and intense light emission, while the second needs further optimization. On the other hand, which device characteristics need to be improved will be pointed out by actual sensing experiments, as well as which process flow is better to be followed. Considering the complexity of the structure and the multi-step nature of process flow, the fact that both parts of the devices satisfyingly operate and can be individually controlled, is very inspiring and opens the way for our novel, integrated sensor device to be tested in actual sensing experiments and, depending on the results, to be patented and commercialized.

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CHAPTER 8

Conclusions

8.1 Nitrides dry etching

An optimized dry-etching procedure for optical cavity formation on nitrides was developed. Mesas with practically vertical sidewalls of roughness < 100 nm were achieved after combined optimization of etch-mask preparation and RIE process. Sidewall roughness and slope of the final mesas were found to be strongly dependent on the starting PR pattern's sidewall roughness and slope, provided that the chloride-based RIE process is mild enough as to not introduce any additional sidewall roughness, while the chemical compponent of etching should be suppressed in order for verticality to be the case. Moreover, an oxygen plasma ashing process can further reduce sidewall roughness of the starting PR patterns, which can be important if a non optimized lithography procedure is used for PR etch-mask patterning. This optimized procedure can yield sidewalls of comperable roughness as the one of a cleaved facet of a nitride-based structure on SiC substrate.

Towards sufficient material protection during RIE, chlorobenzene treatment or post-bake of the PR etch-mask patterns have not significantly improved PR endurance under chloride-plasma conditions. Nevertheless, we have developed a two-layer PR approach, with which it is possible to have more than 1.5 μm PR etch-mask left-over after RIE. This PR thickness should be sufficient to completely protect the underneath material from RIE damage.

8.2 Ohmic contacts to p-type GaN

First, oxidized Ni/Au contacts on MOCVD p-GaN were studied. The oxidation process was optimized in terms of temperature and duration. Any interface insulating layer present on p-GaN surface prior to deposition inhibits contact performance and has to be removed as pointed out by pre-deposition surface treatment experiments and the results of a two-step deposition and annealing procedure, where enhancement of the insulating interface layer through air annealing of p-GaN/Ni contacts had a devastating effect on contact performance. Overall, oxidized Ni/Au contacts to p-GaN were realized, which can serve as a reference for comparison with results of other metal contacts to p-GaN.

Next, various metals were employed as the contact metal to MOCVD p-GaN. A first finding was that thermal annealing of these as deposited contacts degraded their performance in all cases. Therefore, this study mainly focused on as deposited contacts and in p-GaN surface preparation prior to metal deposition. Moreover, contact performance of as deposited contacts showed no relation to either metal work function or electronegativity differences between metal and p-GaN. To the contrary, the lower resistance contacts were obtained when getter metals are employed as the contact metal. This behavior is attributed to contaminating species adsorbed to the surface, which, if not removed, do not permit direct bonding between metal and semiconductor atoms. Towards this, several pre-deposition surface treatments were tested, with boiling aqua regia (AR) giving the best results in terms of contact resistance, and if combined with Cr/Au deposition, contacts with resistance values as low as 50 Ω can be obtained. However, thorough hydration of the surface after AR and before Cr deposition was found to be necessary for this low resistance contact to be obtained, indicating that H_2O molecules passivate the active sites revealed after AR treatment, preventing re-adsorption of air contaminating species. Cr is a getter metal, able to absorb H (present in MOCVD wafer in the form of Mg-H complexes), O, CO and other con-

tamination from p-GaN surface, while its highly oriented d-orbitals (transition metal) are available for covalent type of bonding with the d-orbitals of Ga dangling bonds and other active sites. This is supported by HRTEM results which indicate local epitaxial growth of Cr on p-GaN. Therefore, the mechanism involved for the low resistance, as deposited Cr/Au contacts to p-GaN can be summarized as follows: boiling AR is efficient in removing contamination species from the surface, with subsequent hydration being necessary to prevent re-contamination of the surface until Cr deposition. Then, adsorbed H_2O molecules are either desorbed from p-GaN surface during idle time in the vacuum chamber of the deposition system, leaving a large number of active sites for Cr covalent type of bonding with p-GaN surface atoms, or they are absorbed by Cr if still adsorbed on the surface, as is the case for residual O or C contamination

The above proposed mechanism is supported by the results of XPS analysis performed on both MOCVD and MBE p-GaN surfaces, which indicated that O and C related contamination is present on the non treated p-GaN surfaces (both MOCVD and MBE). However, only a small amount of the O related contamination can be attributed to GaO_x in both MOCVD and MBE cases, since the Ga-O bond state contribution is small in Ga3d emission peak and not the dominant in the O1s one, indicating that O related contamination originates from O containing adsorbed species, such as CO, CO_2, -OH etc. Boiling AR is sufficient in removing both Ga-O phases and adsorbed contamination from the MOCVD surface, since no Ga-O contribution in any peak can be detected after AR, whereas still present in the MBE case. Air exposure of AR treated surfaces results in strong re-adsorption of air species in both cases. However, the two types of p-GaN behave differently concerning the influence of AR treatment on surface Fermi energy level, attributed to NO_x ($x< 3$) state formation only in the MOCVD case. Furthermore, examination of the non annealed Cr/p-GaN interface indicated formation of a binary Ga-Cr phase only in the MOCVD case, which might be related with NOx formed during AR treatment and might be able to explain the low resistance, as deposited Cr/Au contact scheme to MOCVD p-GaN.

8.3 Active region-Quaternary nitrides

Optical properties of a series of InAlGaN thin films and InAlGaN/GaN QWs of various In and Al compositions have been explored. The QN related emission is attributed to strong band-

edge recombination, as ascertained from PL and transmission spectra, while PL characterization indicated a strong dependence of QN band gap value on its composition. For the $In_{0.08}Al_{0.28}Ga_{0.64}N$/GaN QWs, a reduction of internal-fields by a factor of 4 as compared to equivalent GaN/AlGaN QWs was estimated after fitting of our experimental results with theoretically calculated curves indicating an internal-field value of 0.265 MV/cm. Following the same procedure, the corresponding internal-field value for $In_{0.14}Al_{0.28}Ga_{0.58}N$/GaN QWs was estimated to be close to zero as expected from theoretical calculations, which predict zero internal-field in case of In/Al composition ratio close to ½. The reduced internal-fields inside the QN QWs are also indicated by temperature-, power-dependent and time-resolved PL characterization, while optical pumping of laser structures composed of QN QWs in the active region show reduced power threshold values as compared to equivalent GaN/AlGaN structures. The above results indicate that it is possible to obtain lower threshold LEDs and LDs if InAlGaN alloys are incorporated in the active region of such devices.

8.4 LEDs and a novel sensor

A comparative study of the standard oxidized Ni/Au and as deposited Cr/Au contacts as p-electrodes of LEDs was attempted in this section. In a structure optimized for oxidized Ni/Au contacts, LEDs with Cr/Au p-electrodes were inferior as compared to those with oxidized Ni/Au ones, since a difference in turn-on voltage of ~ 2 V was observed, with possible explanations being Mg overdoping-induced p-GaN degradation at the surface/ near-surface region on one hand and, on the other, the beneficial effect of oxidation on electrical properties of Ni covered p-GaN layers. Nevertheless, Cr/Au seems to be a good candidate for serving as the p-electrode in nitride-based optoelectronic devices, since all diodes with this p-GaN contact readily emitted. Moreover, the turn-on voltage difference between LEDs having Cr/Au contacts and oxidized Ni/Au has decreased (even changed sign in diodes with GaN:Mg layer activated in UHV), while diode breakdown was not observed for reverse bias values up to -20 V. Clearly, p-GaN activation process is important for both ohmic contact formation and LED performance.

Moreover, a novel nitride-based sensor, monolithically integrating an LED and a HEMT, is designed and realized. A study concerning process flow optimization resulted in achieving operation of both LED and HEMT parts of the devices in a satisfying level, with the first showing

good performance and intense light emission, while the second needs further optimization. On the other hand, which device characteristics need to be improved will be pointed out by actual sensing experiments, as well as which process flow is better to be followed. Considering the complexity of the structure and the multi-step nature of process flow, the fact that both parts of the devices satisfyingly operate and can be individually controlled, is very inspiring and opens the way for our novel, integrated sensor device to be tested in actual sensing experiments and, depending on the results, to be patented and commercialized.