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EXPERIMENTAL AND THEORETICAL STUDY OF 3C-SILICON CARBIDE NANOWIRE FIELD EFFECT TRANSISTORS

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List of abbreviations

3C-SiC	3 Cubic Silicon Carbide
CMOS	Complementary Metal-Oxide- Semiconductor
MOSFET	Metal-Oxide- Semiconductor Field-Effect Transistor
CNTs	Carbon Nanotubes
NWs	Nanowires
GAA	Gate-All Around
VLS	Vapor–Liquid–Solid
CVD	Chemical Vapor Deposition
MBE	Molecular Beam Epitaxy
CBE	Chemical Beam Epitaxy
FEOL	front-end-of-line
BEOL	back-end-of-line
FEDs	Field Emission Displays
SNAP	Superlattice NAnowire Pattern
TEM	Transmission Electron Microscopy
UHV	Ultra High Vacuum
OAG	Oxide-Assisted Growth
NWL	Nanowire Lithography
SOI	Silicon on Insulator
NIL	NanoImprint Lithography
UV	Ultra-Violet
HEMTs	High Electron Mobility Transistors
MOCVD	Metal Organic Chemical Vapor Deposition
SB	Schotkky Barrier
FE	Field Emission
SEM	Scanning Electron Microscopy
AFM	Atomic Force Microscopy
NEGF	Non Equilibrium Green's Function

UMS	Uncoupled Mode Space
CMS	Coupled Mode Space
BTE	Boltzmann Transport Equation
SR	Surface roughness
rms	root mean square
SS	Subthreshold Slope
DOS	Density of States
PH	Phonon
XRD	X-ray Diffraction
PL	Photoluminescence
EELS	Electron Energy Loss Spectroscopy
EDS	Electron Diffraction Spectrum
RTA	Rapid Thermal Annealing
EBL	Electron-Beam Lithography
SAED	Selective Area Electron Diffraction

Abstract in French

Récemment, la croissance et la caractérisation de nanostructures à une dimension (nanofils, nanotiges, nanotubes) de semiconducteurs à large bande interdite sont largement étudiées à cause de leurs applications potentielles en nanoélectronique, capteurs, batteries et cathodes à émission de champ. L'approche nanofil autorise une géométrie coaxiale de canal / diélectrique de grille, ce qui est idéal pour la réduction des dimensions et le contrôle électrostatique. Parmi les matériaux à large bande interdite, le SiC-3C présente de fortes valeurs de conductivité thermique, champ de claquage, vitesse de dérive des électrons, module de Young et dureté mais également une excellente stabilité chimique et physique. Par conséquent, on s'attend à ce que les nanofils à une dimension en SiC-3C, réalisés par la technique "top-down" ou "bottom-up", génèrent une nouvelle famille de dispositifs haute performance offrant des avantages supplémentaires par rapport à la technologie « classique » Si.

Ce manuscrit est divisé en 3 parties principales. Le premier chapitre donne une vision générale de la croissance des nanofils, de leurs propriétés et des dispositifs associés. L'étude théorique est présentée dans le deuxième chapitre, dans lequel est détaillé le fonctionnement des transistors à effet de champ à base de nanofil SiC-3C ou nanoFET (Field Effect Transistors, FETs) en régime de transport balistique ou en régime de diffusion. Plus précisément, des simulations numériques de nanoFETs à géométrie «gate-all-around » (GAA) à base de nanofils SiC-3C et Si sont présentées. Une description entièrement quantique du transport est adoptée pour les très courtes dimensions. Une résolution self-consistante des équations de Poisson et Schrödinger dans le formalisme des fonctions de Green hors équilibres (non equilibrium Green's functions, NEGF) a été utilisée. Une comparaison directe entre les performances des dispositifs Si et SiC-3C donne quelques éclaircissements sur les différentes propriétés de transport des deux matériaux. Dans le troisième chapitre, la réalisation et la caractérisation électrique des nanoFETs SiC-3C sont présentées. La dernière partie de ce manuscrit est dédiée à la simulation des caractéristiques électriques des nanoFETs élaborés (SiC-3C et Si) en utilisant le logiciel Silvaco. Un ajustement précis des données expérimentales permet d'obtenir la densité de porteurs dans le canal et leur mobilité, d'estimer la qualité de l'interface nanofil/diélectrique, et d'étudier l'effet de la diminution de la concentration de porteurs, de la hauteur de barrière Schottky au niveau des contacts et de la qualité de l'interface sur les performances des dispositifs.

Abstract in English

Recently, the growth and characterization of one-dimensional (1D) nanostructures (nanowires, nanorods, nanotubes) of wide-band-gap semiconductors have been extensively studied due to their potential for applications in nanoelectronics, sensors, batteries, and field emission displays (FEDs). The nanowire (NW) approach allows for a coaxial gate-dielectric channel geometry that is ideal for further downscaling and electrostatic control. Among the wide band-gap materials, 3C-SiC exhibits high values of thermal conductivity, breakdown electric field, electron drift velocity, Young's modulus and hardness as well as excellent chemical and physical stability. Therefore, 3C-SiC semiconductor nanowires, grown either with top-down or bottom-up techniques, are expected to generate a new family of high-performance nanowire devices as an add-on to mainstream Si technology.

This thesis is divided into three main parts. In the first chapter, an introduction to nanowire growth, properties and devices is presented. Our theoretical work follows in chapter two, where a study of 3C-SiC nanowire-based FETs (NWFETs) operating either in ballistic or in dissipative transport regime is indicated. More precisely, we introduce numerical simulations of gate-all-around (GAA) 3C-SiC and Si NWFETs using a full quantum self-consistent Poisson-Schrödinger algorithm within the non-equilibrium Green's functions (NEGF) formalism. A direct comparison between Si and 3C-SiC device performances sheds some light on the different transport properties of the two materials. In the third and forth chapter, the nanowire growth, the fabrication and the electrical characterization of 3C-SiC NWFETs is presented. The last part of the thesis is devoted to the simulation of the electrical behaviour of the experimental NWFETs (both 3C-SiC and Si NWFETs) by using the Silvaco simulation tool. The accurate fitting of the experimental data, allows us to calculate the nanowire carrier concentration and mobility, and estimate the nanowire/dielectric interface quality as well as to study the effect of carrier concentration lowering, Schottky barriers height at contacts and the interface quality on the device's performance.

Περίληψη

Η ανάπτυξη και ο χαρακτηρισμός νανοδομών μιας διάστασης (1-Δ) όπως νανονήματα, νανοκολόνες ή νανοσωλήνες ημιαγωγών υψηλού χάσματος έχουν πρόσφατα εκτενώς μελετηθεί εξαιτίας των πιθανών εφαρμογών τους στη νανοηλεκτρονική, σε αισθητήρες, μπαταρίες και οθόνες εκπομπής πεδίου. Η χρήση νανονημάτων επιτρέπει ομοκεντρική γεωμετρία διηλεκτρικού πύλης και καναλιού του τρανζίστορ η οποία είναι ιδανική για την περαιτέρω σμίκρυνση των διαστάσεων της διάταξης και καλύτερο ηλεκτροστατικό έλεγχο των φορέων. Ανάμεσα στους ημιαγωγούς υψηλού χάσματος, το καρβίδιο του πυριτίου (3C-SiC) έχει μεγάλο συντελεστή θερμικής αγωγιμότητας, μεγάλη τιμή ηλεκτρικού πεδίου κατάρρευσης και μέτρου ελαστικότητας, μεγάλη ταχύτητα ολίσθησης ηλεκτρονίων καθώς και εξαιρετική χημική και φυσική σταθερότητα. Επομένως, νανονήματα 3C-SiC, κατασκευασμένα ακολουθώντας τεχνικές είτε από «πάνω προς τα κάτω» ή από «κάτω προς τα πάνω», αναμένεται να δημιουργήσουν μια νέα οικογένεια ηλεκτρικών διατάξεων οι οποίες θα χρησιμοποιηθούν ως πρόσθετες/επέκταση στην υπάρχουσα τεχνολογία πυριτίου.

Η παρούσα διδακτορική διατριβή χωρίζεται σε τρία κύρια μέρη. Στο πρώτο κεφάλαιο παρουσιάζεται μια εισαγωγή στην κατασκευή γενικά νανονημάτων και στις βασικές ιδιότητές τους καθώς και σε διατάξεις βασισμένες σε αυτά. Η θεωρητική μας μελέτη εν συνεχεία ακολουθεί στο δεύτερο κεφάλαιο, όπου τρανζίστορ βασισμένα σε νανονήματα 3C-SiC λειτουργούν είτε στην βαλλιστική περιοχή ή στην περιοχή όπου υπάρχει σκέδαση φορέων. Πιο συγκεκριμένα, παρουσιάζουμε αριθμητικές προσομοιώσεις τρανζίστορ περιμετρικής πύλης βασισμένα σε νανονήματα 3C-SiC και πυριτίου (Si) χρησιμοποιώντας έναν κβαντικό αλγόριθμο βασιζόμενο σε αυτό-συνεπή λύση των εξισώσεων Poisson και Schrödinger υπό τον φορμαλισμό εξισώσεων Green εκτός ισορροπίας (NEGF). Μια άμεση σύγκριση ανάμεσα σε διατάξεις 3C-SiC και πυριτίου επισημαίνει τις βασικές διαφορές των δύο ημιαγωγών όσον αφορά στην ηλεκτρική τους συμπεριφορά. Το τρίτο και τέταρτο κεφάλαιο αναφέρονται στην ανάπτυξη των νανονημάτων, στην κατασκευή των τρανζίστορ και στον ηλεκτρικό χαρακτηρισμό τους. Στο τελευταίο μέρος της διδακτορικής διατριβής παρουσιάζουμε την προσομοίωση των πειραματικών μας αποτελεσμάτων χρησιμοποιώντας το λογισμικό προσομοίωσης Silvaco. Η ακριβής προσομοίωση μας επιτρέπει να υπολογίσουμε τη συγκέντρωση και την ευκινησία των φορέων στα νανονήματα, και επίσης να εκτιμήσουμε την ποιότητα της διεπιφάνειας ανάμεσα στα νανονήματα και το διηλεκτρικό υλικό, καθώς και να εντοπίσουμε την επίδραση της μείωσης της συγκέντρωσης των φορέων, του ύψους φραγμού στις επαφές πηγής και απαγωγού καθώς και της ποιότητας της διεπιφάνειας στην απόδοση του τρανζίστορ.

Summary

Low-dimensionality materials and especially one-dimensional (1D) have stimulated great interest due to their importance in basic scientific research and potential technological applications. Their low dimensionality -associated with new quantum size effects- has provided new ways to develop nanoscale electronics, optoelectronics and in general nanostructures. On the other hand, Silicon Carbide (SiC) is widely investigated due to its physical properties like the wide band-gap, the high breakdown field strength, the high value of thermal conductivity, the high saturation carrier drift velocity and the stability in high temperature as well as in corrosive environments. The combination of these properties with the advantages of nanowires can result in devices operating at high temperature (and/or high operating voltage) with unique performance.

Before the realization of the present thesis, only one experimental study on SiC NW FETs had been reported presenting a poor device performance. Moreover, none theoretical study concerning the electrical transport properties of 3C-SiC nanowires had been performed. Therefore, the main aim of the present thesis was to perform a complete experimental and theoretical study of SiC NWFETs.

The first thesis chapter is a bibliography review and it is divided into three main parts (section 1.2, 1.3 and 1.4). After a brief introduction (section 1.1), the next two parts (section 1.2 and 1.3) are addressing important steps toward the implementation of semiconductor nanowire devices. The first of these parts (section 1.2) describes various aspects of nanowire growth and of the control of their properties. This is followed by the second part (section 1.3) discussing the development and optimization of new, nanowire-based devices mainly focusing on field effect transistors. We briefly cover the importance of characterizing and extracting important physical properties in order to evaluate and optimize nanowire growth and processing of devices based on them. Potential devices based on nanowires then need to be appropriately characterized, which is briefly described. In part three (section 1.4), we focus on 3C-SiC nanowires growth, properties and their applications. Again, the main device application is a nanowire-based transistor, which is the central subject of focus of this thesis. In section 1.4, we summarize the various published results from other research groups as an introduction to our theoretical and experimental work, which will be presented in chapter 2, 3 and 4.

Our theoretical work described in chapter two was started by investigating on a theoretical level the advantages of SiC-based NWFETs. Our SiC calculations are based on an initial code dedicated to Si NWFETs. This code was appropriately modified in order to describe the

behavior of SiC. This study had as target to reveal which would be the ultimate performance of SiC-based NWFETs once the technology-related issues would be resolved. As the dimensions are scaled down, the increasing importance of physical phenomena like quantum tunneling, reflections through metallic/semiconducting barriers and through channel potential barriers and strong quantum confinement have drawn the interest of a full quantum description of carrier transport. Hence, device numerical simulations based on the self-consistent solution of the Schrödinger and Poisson equations are envisaged in order to correctly model these physical effects and give a valuable analysis and prediction of the device performance (section 2.2). We use three different simulation techniques in order to describe the electrical transport properties of 3C-SiC and Si NWFETs operating at distinct electrical transport regimes. Depending on the channel length (L_G) a transistor operates in ballistic, quasi-ballistic and diffusive electrical transport regime. When $L_G<\ell$, where ℓ is the mean free path in the semiconductor (the distance between two collisions-scattering events), then we do not expect any scattering along the channel (only scattering at the source/channel and drain/channel interfaces), in other words we have ballistic conduction. In this regime, by excluding the effect of scattering, we expect to observe the upper limit of device performance. Mobility theory estimates a mean free path value for Si and 3C-SiC around 10 nm. The experiments predict even shorter lengths, around 2-3 nm due to the presence of acoustic phonon scattering. In ballistic transport regime, we use a Poisson/Schrödinger self consistent solution within the NEGF formalism (section 2.3). Our NWFETs are Triple-gated and have channel length varying from 5 to 15 nm and a cross section side 3 and 4 nanometers.

On the other hand, ultimately scaled experimental NWFETs, mainly based on Si nanowires, operate in quasi ballistic regime. When the channel length is comparable with the mean free path, the transport is not pure ballistic. Due to the increased effect of both surface roughness and phonon scattering, we have a deviation from the ideal transport conditions of ballistic carriers. For this dissipative transport regime, we used a similar simulation scheme as for the case of ballistic transport, and moreover we included a quantum treatment of scattering effects (both surface roughness and phonon scattering) (section 2.4.2). For this kind of simulations, we implemented a Gate All Around (GAA) device geometry and we chose the length of the nanowire to be equal to 20 nm and the cross section side at 5 nm.

Our experimental 3C-SiC NWs (as they will be presented in chapter three) have length of few micrometers and diameter from 40 to 90 nm. These dimensions are far away from the ballistic transport regime conditions ($L_G>\ell$) allowing us to use a drift-diffusion model to describe this diffusive transport regime. To address this large dimension issue, we solve the continuity equation

self-consistently with the Poisson equation and we calculate the current through the drift diffusion model (which is an approximation of Boltzmann transport equation) (section 2.4.1). The simulated devices have a length from 200-750 nm and cross section side of 10 nm. Again this calculation shows the ultimate performance for the large dimension SiC-based NWFETs. As a general conclusion of our theoretical work, we could say that SiC based devices are quite competitive to Si ones. Despite the slightly worst electrical performance of SiC NW devices, SiC NW could be used to targeted applications such as high temperature or high operating voltages devices.

The experimental work is presented in chapter three and four. In chapter three, we present our efforts on SiC nanowire growth (section 3.2) starting either from CNTs or Si NW and converting them to SiC by exposing them in Si or C respectively. In chapter four we describe the process for the transistor fabrication (section 4.2) and finally present the electrical characterization of devices based on SiC nanowires received from our collaborators (section 4.3). We analyzed the behaviour of NWFETs based on two different types of 3C-SiC nanowires, a) nanowire grown without catalyst in a convective furnace and b) nanowires grown in a home-made CVD system based on Vapor Liquid Solid (VLS) method (with catalyst assistance). Structural characterization of the nanowires, which includes SEM, TEM, XRD and Raman spectroscopy, is presented and reveals that both types of nanowires have similar quality in terms of crystal orientation ([111]), defects density, stacking faults etc. The initial substrate of a typical device was a highly doped Si wafer with a dielectric layer on top of it (usually SiO_2). To electrically contact the nanowires, a two-step electron-beam lithography and a lift-off process were required. Back-gated 3C-SiC NWFETs were fabricated and the electrical characterization revealed electron conduction through the nanowires. Devices with either ohmic or Schottky contacts were observed leading to two different operation modes. Transistors with ohmic-like contacts manifest very weak gating effect and the device switching off is not achievable even for high negative gate voltages due to the high electron concentration along the nanowire. In contrast, the Schottky barrier (SB) at Source (S)/ Drain (D) regions acts beneficially for the FET performance by significantly suppressing the off current. At higher positive gate voltages, the Schottky barriers tend to be transparent leading to high (compared to ohmic case) transconductance and I_{ON}/I_{OFF} ratio, 3.88 nS and $2.81 \cdot 10^3$, respectively. In the case of unintentionally highly doped nanowires, where the direct effect of the gate voltage on the accumulated carriers is negligible, SB-NWFET presents improved performance by suppressing the off current and indirectly modulating the drain current through the control of Schottky barriers transparency at source and drain regions. Both types of nanowires led to similar device electrical behaviour. The similar NW quality explains the almost identical performance of the devices based on differently grown 3C-SiC nanowires.

Two-dimensional Silvaco simulation package is incorporated in order to fit the experimental output and transfer characteristics (section 3.5.1). The custom drift diffusion model which was previously described (section 2.4.1), has not been used due to its long required calculation time as well as due to the fact that doping and interface defects could not be included in the simulations. The fitting process allows us to estimate, a) the quality of the nanowire/dielectric interface, b) the carrier concentration and mobility along the nanowire in both types of nanowires, catalyst free grown and catalyst based nanowires. Beside this, the various shapes of experimental I-V characteristics, such as completely linear, non-linear symmetric, non-linear asymmetric were simulated by adjusting the SB at source and drain regions. Possible origins for the different values of SBs from contact to contact are proposed.

For cross checking our Silvaco-based fitting of experimental results, we also investigated the application of Silvaco simulation tool in Si nanowire FETs (4.4.2). More particularly, experimental FETs based on Boron-implanted Si nanowires were prepared. This subject could be very interesting for SiC NWs since implantation is a common technique of doping and its application could be obligatory in the case of SiC NW fabricated by conversion of Si NWs. These experiments incited us to investigate our SB SiC NWFETs which, as exposed above, presented the best electrical characteristics. Both the process steps of device fabrication and the device operation are simulated using Silvaco simulation tool. Again, an agreement, in terms of electrical characterization, between Silvaco and experiment is observed.

In conclusion, a combined theoretical and experimental study of SiC NW based FETs was presented. Theory predicted that SiC NWFETs are competitive to corresponding Si ones in terms of electrical performance (both in ballistic and quasi-ballistic regime), and therefore experimental SiC NW FETs could be realized and used, as an add on to Si mainstream technology, to some targeted applications such as high temperature and/or high operating voltage FETs. In the experimental part, two different SiC nanowire growth techniques were used. The first route was to convert CNTs to SiC and the other to grow Si NWs and convert them to SiC. Back gated NWFETs, based on nanowires received from our collaborators, were prepared and electrical characterization revealed two distinct device operation modes depending on the nature of the source and the drain contacts (ohmic or Schottky Barrier (SB) like). In the case of unintentionally highly doped nanowires, SB-NWFET presents improved performance by suppressing the off current and indirectly modulating the drain current through the control of Schottky barriers transparency at source and drain regions.

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Citations to published work

International Journals

1. **K. Rogdakis**, E. Bano, L. Montes, M. Mikhael Bechelany, D. Cornu and K. Zekentes, "Schottky barrier 3C-SiC nanowire field effect transistor", *Submitted to Nanotechnology* (2010)
2. **K. Rogdakis**, S. Poli, E. Bano, K. Zekentes and M. G. Pala , "Phonon and surface roughness limited mobility of gate-all-around 3C-SiC and Si nanowire FETs", *Nanotechnology* **20** 295202, (2009)
3. S. K. Lee, S. Y. Lee, **K. Rogdakis**, C. O. Jang, D. J. Kima, E. Bano, K. Zekentes, "Si Nanowire p-FET with asymmetric source-drain I-V characteristics", *Solid State Communications* **149**, 461-463, (2009)
4. S.Y. Lee, C. O. Jang, D. J. Kim, J. H. Hyung, **K. Rogdakis**, E. Bano, K. Zekentes and S. K. Lee, "Fabrication of Ion-implanted Si Nanowire p-FETs", *J. Phys. Chem. C* **112** 13287–13291, (2008)
5. **K. Rogdakis** S. Y. Lee, M. Bescond, S. K. Lee, E. Bano and K. Zekentes, "3C-SiC nanowire FET: An experimental and theoretical Approach", *IEEE Transactions on Electron Devices* **55** 1970-1976, (2008)
6. **K. Rogdakis**, M. Bescond, E. Bano and K. Zekentes, "Theoretical comparison of 3C-SiC and Si nanowire FETs in ballistic and diffusive regimes", *Nanotechnology* **18** 475715, (2007)

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9. **K. Rogdakis**, S. Y. Lee, D. J. Kim, S. K. Lee, E. Bano and K. Zekentes, "Effect of Source and Drain contacts Schottky Barrier on 3C- SiC nanowire FETs I-V characteristics", *Materials Science Forum* vols. 615-617 235-238, (2009) *–presented in ECSCRM (2008)*
10. **K. Rogdakis**, S. Poli, E. Bano, K. Zekentes and M. G. Pala, "Backscattering coefficient in 3C-SiC gate-all-around nanowire FETs", *will be published in IEEE Xplore library, presented in IEEE NANO conference,* (2009)

Chapter one: Bibliography review on nanowire growth and related devices

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Chapter one: Bibliography review on nanowire growth and related devices

During the last half century, a dramatic downscaling of electronics has taken place, a miniaturization that the industry expects to continue for at least a decade. In this chapter we present efforts to use one dimensional semiconductor nanowires grown either with top-down or bottom-up techniques in order to bring new, high-performance nanowire devices as an add-on to mainstream Si technology. The nanowire approach offers a coaxial gate-dielectric channel geometry that is ideal for further downscaling and electrostatic control, as well as heterostructure-based devices on Si wafers. Devices based on such materials are, however, still in an embryonic stage from an industrial point of view. Whether they will really have an impact on future post- CMOS technology depends on more factors than just superior single-device performance. From the history of the semiconductor industry, we have learned that only those technologies that can be integrated and scaled up for large hierarchical systems will survive and have impact.

This chapter is divided into three main parts (section 1.2, 1.3 and 1.4). After an introduction (section 1.1), the first two parts (section 1.2 and 1.3) are addressing important steps toward the implementation of semiconductor nanowire devices. The first part (section 1.2) describes various aspects of nanowire growth, understanding and ultimately controlling their properties. This is followed by the second part (section 1.3) discussing the development and optimization of new nanowire-based devices mainly focusing on field effect transistors. We briefly cover the importance of characterizing and extracting important physical properties in order to evaluate and optimize nanowire growth and processing. Potential devices that can benefit from being built around nanowires then need to be identified and characterized, which is briefly described. In part three (section 1.4), we present the work published by other groups on 3C-SiC nanowires growth, properties and their applications. Again, the main device application is a nanowire-based transistor, which is the central subject of focus of this thesis.

1.1 Introduction

The rapid development of integrated circuit technology is primarily due to MOSFET downscaling trends that have continued to the present day. However, silicon-based MOS

technology is expected to face fundamental limits in the near future, and therefore, new types of nanoscale devices are being aggressively investigated. The manufacture of silicon based chips is based on a, so called, “top down” approach whereby the materials used to make the devices are first deposited on the chip and then structured using optical (or electron-beam) lithography and etching. In this way, a large number of layers can be built up to connect the transistors that are constructed from the topmost part of the single crystal silicon wafer. An alternative to the “top down” method is the use of self-organization in which large complex structures are constructed from smaller building blocks, e.g., molecules. This approach is referred to as “bottom up” and includes molecular self-assembly and the generation of uniform crystalline structures such as carbon nanotubes (CNTs) and nanowires (NWs).

Recently, various semiconductor NW devices have drawn much attention because of their possible use in future electronics and optoelectronics applications. Continued MOSFET scaling has led to the study of non-planar FET geometries that can provide better short channel control than conventional planar FETs. In particular, gate-all-around (GAA) or surround gate FETs with a thin NW channel can provide superior electrostatic characteristics that will allow continued scaling beyond what is possible with planar technology (providing also the possibility of a 3-D chip configuration).

Semiconductor NWs represent unique materials for exploring new emergent phenomena at the nanoscale [1.1]. In the physics of nanoscale structures, quantum effects play an increasingly prominent role. Quantum wires have demonstrated interesting electrical transport properties that are not seen in bulk materials. This is because, in quantum wires, electrons could be quantum-confined laterally and thus could occupy discrete energy levels that are different from the energy bands found in bulk materials. Due to low electron density and low effective mass, the quantized conductivity is more easily observed in semiconductors, e.g., Si and GaAs, than in metals. In addition to the opportunity to describe the new physics demonstrated by nanowires, much effort has been devoted for fabricate high-quality semiconductor nanowires by employing different techniques due to the importance of semiconductor materials to the electronics industry. The most popular technique used to fabricate semiconductor artificial structures with feature sizes in the sub-100 nm range is the e-beam lithography [1.2], which involves tedious processes of photo-resist removal, chemical or ion-beam etching and surface passivation, etc. On semiconductor nanostructures, etching processes always lead to significant surface damage and roughness, and thus surface states are introduced to the nanostructures. Such damage may not be serious for the structures in the micrometer range. However, structures with dimensions in the nanometer range are very sensitive to the surface states or the impurities induced by fabrication processes. One-dimensional (1D) nanostructures formed

‘‘naturally’’ (self-organized growth) without the aids of ex situ techniques, such as chemical etching, are desirable not only in fundamental research but also in future nanodevice design and fabrication. Most bottom-up approaches are statistical by nature and are lacking the fidelity of top-down fabrication. On the other hand, bottom-up approaches for making nanoscale devices circumvent some of the fabrication challenges and the high cost of equipment that are associated with established top-down CMOS processing. Acquiring and maintaining such big-ticket infrastructure that is prone to becoming obsolete at a rapid rate is out of bounds to most universities and even too many corporations. Therefore, there is a great need to focus on bottom-up fabrication methods for NW-based devices since they enable a wider range of academic institutions, laboratories, and corporations to participate and contribute to the growth of NW related electronics devices.

A well-known self-organized growth mechanism for preparing nanowires is the vapor–liquid–solid (VLS) process (also known as metal catalytic growth [1.3]). This technique can produce freestanding crystalline nanowires of semiconductor and metal oxide materials with fully controlled nucleation sites and diameters from pre-formed metal catalysts. Since the 1960s, semiconductor whiskers grown by this technique [1.3] have been extensively studied. In recent years, various new techniques have been developed to realize 1D nanostructures, such as laser-assisted chemical vapor deposition (CVD) [1.4], oxide-assisted CVD (without a metal catalyst) [1.5], thermal CVD [1.6], metal-catalyzed molecular beam epitaxy (MBE) [1.7] and chemical beam epitaxy (CBE) [1.8]. Although the number of various kinds of 1D nanostructures fabricated via different techniques increases dramatically every year, our understanding of the basic process of 1D nanostructure formation has not reached maturity. How to fabricate desired 1D nanomaterials with tailored atomic structures and how to integrate functional nanostructures into devices are still challenging issues for materials scientists. For 1D semiconductor nanomaterials to have wide practical applications, however, many areas require further pursuing. Integration on Si is essential for nanowires to be of interest for large-scale electronic applications.

Among the different materials considered for growing NWs, silicon has been studied extensively due to its compatibility with conventional CMOS technology. Si NWs with diameters as small as one nanometer have been grown successfully. Ge NWs are also of particular interest due to their higher carrier mobility. NW-based transistors have also been demonstrated using a number of other materials, chief among these are ZnO, SnO, SiC, InP, GaN, other III–V compounds, and conducting polymers [1.9]. Quantum confinement effects make modeling of NW transistors a complex problem [1.10]. While there are many studies in the literature on the modeling of NW transistors based on non-equilibrium Green’s functions or Monte Carlo approaches, the physics

related to the operation of NW transistors needs to be well articulated so that simple compact models, including ballistic transport and realistic subband parameters, can be developed for circuit design using SPICE-like simulators.

Special field of applications (e.g. amplifiers used in wire-less telecommunications), demands devices with high power and high temperature operation and as a consequence the usage of wideband-gap semiconductors is urgent. Recently, the growth and characterization of one-dimensional nanostructures (nanowires, nanorods, nanotubes) of wideband-gap semiconductors have been studied due to their potential for applications in nanoelectronics, sensors, batteries, and field emission displays (FEDs) [1.11-1.13]. Among the wideband-gap materials, SiC presents high thermal conductivity, high breakdown electric field, high electron drift velocity, high Young's modulus and hardness, high melting temperature, excellent oxidation and corrosion durability, high strength at elevated temperatures, good thermal shock resistance and excellent chemical and physical stability (table 1.1). The native oxide is silicon dioxide, which makes SiC more compatible with Si technology. SiC NWs combine the above properties of 1D material with that of SiC and electronic devices based on SiC NW are expected to present concrete advantages in terms of dissipated power, stability and high voltage operation in comparison to their Si (Ge) counterparts.

Table 1.1 Properties of SiC compared to other semiconductors.

	Si	GaAs	4H-SiC	6H-SiC	3C-SiC	GaN	Diamant
E_g (eV)	1.1	1.4	3.36	3.02	2.4	3.4	5.5
V_{sat} (cm s^{-1})	1 10^7	0.8 10^7	2 10^7	2 10^7	2.5 10^7	1.5 10^7	2.7 10^7
E_c (V m^{-1})	0.4 10^6	0.4 10^6	4 10^6	4 10^6	3 10^6	5 10^6	10^7
μ (cm^2/Vs)	1100	6000	800	370	1000	900	2200
σ_{therm} (WK^{-1} cm^{-1})	1.5	0.5	4.9	4.9	4.9	1.3	20

1.2 One-dimensional material growth and basic properties

Most semiconductor NWs are produced using the VLS growth method that has been generalized and expanded to a host of semiconductor materials by Lieber's group. VLS NWs require a metal nanoparticle to seed NW growth, and NWs are often prepared as a powder or as a

surface-supported film. While some parameters, such as the concentration of dopants or the NW length, are difficult to be controlled, novel materials, such as core-shell or branched NWs, can be prepared. In the first part of this section, we will review the bottom up nanowire growth methods, which are based on VLS mechanism, the oxide assisted growth (OAG) and the template assisted method. Both the alumina-template and the VLS-synthesized NWs can be prepared with an alternating and controllable stoichiometry along the long axis of the NW. After that, we will refer to growth techniques, which follow the top-down process such as, the superlattice nanowire pattern transfer method (SNAP) and nanoimprint. Most NWs are studied for their electronic (or optoelectronic) properties. In the last part, we present the basic properties of nanowires, including electrical, thermal and properties due to their 1D structure and quantum confinement and summarize the general conclusions.

1.2.1 Vapor phase synthesis

Introduction

Among all vapor-based methods, those employing the VLS mechanism seem to be the most successful in generating large quantities of nanowires with single crystalline structures. This process was originally developed by Wagner & Ellis to produce micrometer-sized whiskers in the 1960s [1.3], later justified thermodynamically and kinetically, and recently re-examined by Lieber, Yang, and other researchers to generate nanowires and nanorods from a rich variety of inorganic materials [1.14.1.15]. Several years ago, Yang et al. used in situ transmission electron microscopy (TEM) techniques to monitor the VLS growth mechanism in real time [1.18]. A typical VLS process starts with the dissolution of gaseous reactants into nanosized liquid droplets of a catalyst metal, followed by nucleation and growth of single-crystalline rods and then wires. The one-dimensional growth is induced and dictated by the liquid droplets. The growth direction should correspond to the lowest energy facet of the crystal being grown. This is the most common case for nanowire growth. The collector (catalyst seed)/crystal interface forms on the close packed low energy planes of the crystal. For example in Diamond and Zinc blende crystal structures these are under most conditions the {111} planes and preferred growth directions are the <111> directions and for Wurtzite crystals the similar <0001> direction is most common. Exceptions to this general trend have been reported. These exceptions can be grouped depending on why the nanowires do not

grow perpendicularly to the lowest energy facet [1.16]. For example, the growth direction has a strong diameter dependence that the smallest-diameter nanowires grow primarily along the (110) or (100) direction, whereas larger nanowires grow along the (111) direction [1.15]. There is also the possibility to have a lack of mobility of the collector (catalyst seed). The nanowire then grows in the direction of the original interface [1.17].

Vapour Liquid Solid mechanism

The VLS mechanism is based on metal catalysts. Each liquid droplet serves as a virtual template to limit the lateral growth of an individual wire. The metal clusters play a very important role in determining the final size and position of nanowires grown on the substrate. This feature of VLS growth process provides a method for controlling the size and position of nanowires by controlling the size and position of the metal catalyst. In this paragraph, the main steps of nanowires growth based on VLS mechanism are schematically described. The main steps are described schematically below in figure 1.1:

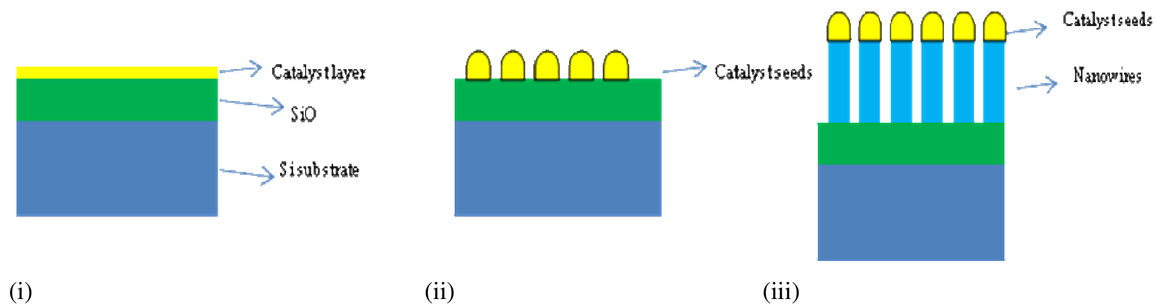

Figure 1.1 VLS mechanism steps: i) before the metal catalyst deposition, a thermal oxide is developed on the substrate. The oxide (SiO_2) has mainly an insulating role, ii) the thermal annealing allows the formation of the catalyst seeds. The molecules of the catalyst shrink under high temperature and a catalyst seed appears. iii) The VLS mechanism allows a eutectic melt formation and thus a preferential site for gas absorption. The nanostructure grows by precipitation from the catalyst interface.

The core of the VLS mechanism is the introduction of a liquid-solid interface in vapor phase-based growth, which breaks the symmetry of the isotropic crystal, making it to grow in a 1D structure. A metal particle (Au, Pt, or Ni) is utilized to form a liquid alloy with the material from the substrate or with material supplied in the vapor phase. At a certain temperature, the composition of this alloy will be in equilibrium. When more growth material is supplied at this temperature, the

alloyed particle becomes supersaturated, which results in nucleation and growth. The metal particle will not be consumed during growth and can therefore be seen as a catalyst for 1D growth. The diameter of the wire is dictated by the size of the liquid particle and remains essentially unchanged during the entire growth (this is not true for all cases, see next section: Pressure effect-MBE experiments). The major requirement on the metal in VLS growth is that it must form a liquid solution with the growth material at the growth temperature, and be able to create a super-saturation acting as driving force for crystallization of the nanowire material. This can be achieved if the metal and the growth material form a eutectic compound. The liquidus line ("melting temperature line") will have a minimum at a certain composition in a binary phase diagram for a eutectic compound. This minimum is called the eutectic point.

Pressure effect- MBE experiments

Until recently, researchers thought that metal seeds size remains essentially unchanged during the entire process of VLS based nanowire growth. Hannon et al. [1.19] reported in situ observations, under an electron microscope, of the growth of silicon nanowires in ultra-clean conditions. They showed that, under the ultra-clean, high-vacuum conditions of their special electron microscope, larger droplets grow at the expense of smaller ones. These smaller droplets then shrink away, preventing any further nanowire growth from them. This effect, known as Ostwald ripening, is named after Wilhelm Ostwald (1909 chemistry Nobel laureate) who explained the effect as resulting from a decrease in total surface energy that occurs when atoms are transferred by diffusion processes from smaller to larger crystals [1.20]. Such an energy-minimizing diffusion transfer requires the efficient transport of atoms between neighbouring gold droplets. This cannot occur through gaseous diffusion above the silicon wafer because of the extremely low vapor pressure of gold; equally, the transport of gold atoms through the bulk of the silicon is also negligible. Hannon et al. argued convincingly that the mode of transport is surface diffusion, which requires not only a high diffusivity of gold on the silicon surface, but also a high solubility of gold on the surface or in a thin surface layer. This would fit with what we know about the growth of silicon nanowires by MBE. This is a technique based on the VLS method, but in which silicon is supplied not as a gas but as a directed beam of atoms. Molecular-beam epitaxy usually requires an ultra-clean environment, and here the transport of silicon as well as that of gold occurs through diffusion on the silicon surface, not through the gas [1.20].

A tiny amount of oxygen, as it is present under most technological growth conditions but not in the ultra-clean, high-vacuum environment used in their experiments might efficiently block the diffusion path of gold on the silicon surface. This would render the gold droplets independent of each other, as has been assumed for the past 40 years. Today, the oxygen content of silicon wafers is exactly specified for the best possible gettering performance. Analogously, the indirect conclusion from the fact that Hannon and colleagues [1.19] observe an effect under highly controlled, low-vacuum conditions that is not observed under less severely controlled conditions could be that a little added oxygen impurity ,although not too much , is beneficial for silicon nanowire growth.

In another study by Schubert et al. [1.20], Si nanowhiskers in the diameter range of 70 to 200 nm were grown on (111)-oriented silicon substrates by MBE. The experimentally observed radius dependence of the growth velocity of the nanowhiskers is opposite to what is known for VLS growth based on CVD and can be explained by ad-atom diffusion on the surface of the whiskers. In the case of the CVD method as we referred previously, small droplets of metals like gold are forming low-temperature eutectic liquids with silicon acting as a seed for the whisker growth. The silicon is preferentially incorporated via the liquid silicon–metal droplet. It is characterized by silicon whisker growth at the whisker/droplet interface by the incorporation of Si atoms coming from the liquid droplet. However, the whisker growth by MBE has a strong surface-related Si diffusion component, which leads to a larger growth rate for nanowhiskers with a smaller radius. This is just opposite to what is well established in the case of CVD-grown nanowhiskers. One has to take into account that they investigated the MBE growth via a gold/silicon eutectic. The use of other metals/silicon eutectic systems might show a different behaviour.

1.2.2 Thermal evaporation

Nanowire production in large quantities is required in order to be realistic the usage of NW devices as alternatives to standard Si technology. Several growth strategies have been proposed to achieve large-scale Si NW growth, most of them still requiring the presence of a metal catalyst to promote 1D nucleation as we already presented in the previous sections. With process temperatures usually exceeding 1000 °C, metal catalysts are mixed to the Si precursor vapor either by thermal evaporation or laser ablation. There is a need, however, to avoid the metal contamination potentially

arising from the residual catalyst particles. Removing the catalyst post growth may require complex and expensive purification treatments.

Nanowires and some interesting morphologies of nanostructures such as nanoribbons, nano-tetrapods and comb-like structures can be grown by a simple method of thermal evaporation of solid source materials avoiding the usage of metal catalyst.

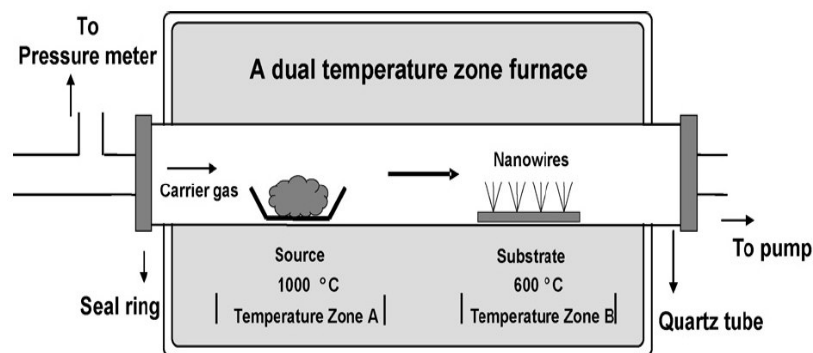

Figure 1.2 A simple experimental setup of the thermal evaporation method for synthesizing ZnO nanostructures. The source material is ZnO or a mixture of ZnO and carbon. Different forms of the ZnO nanostructures, e.g., nanowires and ribbons, grow in different temperature zones.

The growth mechanisms of many nanowires from thermal evaporation (without adding metal catalysts) are poorly understood. There are some special materials containing no metal elements that can also develop into nanowires from their oxide decomposition (setup similar with figure 1.2). Wang et al. [1.21] reported that SiO_2 largely enhanced Si nanowire growth. A model called oxide-assisted growth (OAG) was therefore proposed with evidence from experiments The OAG method provides a viable alternative for metal-free bulk production of Si NWs [1.22]. This method, however, has limitations for the shape control and uniformity of the resulting nanostructures. Thin and crystalline Si NWs are often coupled with partially or fully oxidized structures, resulting in crystalline Si spheres connected into chains by SiO_2 bridges of variable length. The advantages of the OAG technique are (1) its versatility, (2) the use of a relatively cheap experimental setup, (3) the fact that NW bundles of different materials can be easily synthesized without the need of potentially dangerous precursor gases, such as SiH_4, (4) the NWs are highly pure since no metal catalyst is involved and (5) doping of NWs can be easily achieved because the experimental setup for OAG of Si NWs is very similar to that of the laser ablation technique. Doping can be easily realized with the assistance of laser ablation of solid dopant materials during nanowire growth. Si nanowires fabricated by this method showed uniform diameters (about 20 nm) and their lengths were over several hundred micrometers. On the other hand, the high temperatures

involved in the process do limit the substrate selection. NWs prepared by this technique are suitable for post growth processing, typically via dispersion in solution. Shape separation of as-grown NW bundles requires further processing. Ideally, one should engineer and optimize the synthesis to achieve 100% yield of the desired nanostructure morphology.

1.2.3 Template-assisted synthesis and alignment

The template-assisted synthesis of nanowires is a conceptually simple and intuitive way to fabricate nanostructures [1.23]. These templates contain very small cylindrical pores or voids within the host material, and the empty spaces are filled with the chosen material, which adopts the pore morphology, to form nanowires. In template-assisted synthesis of nanostructures, the chemical stability and mechanical properties of the template, as well as the diameter, uniformity and density of the pores are important characteristics to consider. Templates frequently used for nanowire synthesis include anodic alumina (Al_2O_3), nano-channel glass, ion track-etched polymers and mica films. A similar structure could be obtained by the template-mediated electrochemical synthesis of nanowire. The control over the location of the nucleation of nanowires in the electrochemical deposition is determined by the pore positions, which can be precisely controlled by imprint lithography [1.24], and by growing the template on a patterned conductive substrate that serves as a back electrode, different materials can be deposited in the pores at different regions of the template.

Ordering nanowires into useful structures is another challenge in order to harvest the full potential of nanowires for applications. Control of the position of a nanowire in the growth process is important for preparing devices or test structures containing nanowires, especially when involving a large array of nanowires. Post-synthesis methods to align and position nanowires include micro-fluidic channels [1.25], Langmuir–Blodgett assemblies [1.26], and electric-field assisted assembly [1.27]. The first method involves the orientation of the nanowires by the liquid flow direction and by the interaction of the nanowires with the sidewalls of the channel. The second method involves the alignment of nanowires at a liquid-gas or liquid-liquid interface by the application of compressive forces on the interface. The third technique is based on dielectrophoretic forces that pull polarisable nanowires toward regions of high field strength. The nanowires align between two isolated electrodes, which are capacitatively coupled to a pair of buried electrodes biased with an AC voltage. Once a nanowire shorts the electrodes, the electric field is eliminated, preventing more nanowires from depositing.

1.2.4 Alternative nanowire fabrication techniques

One critical step for the integration of nanowire devices in standard CMOS technology is the well position control and alignment. The NWs need to be organized into the desired device setting and that remains a challenge. Thus, the majority of NW studies have focused on single or few-device demonstrations, albeit often with spectacular resulting science. In this section, we will present alternative techniques for nanowire fabrication using this time top-down processes.

The superlattice nanowire pattern transfer method, or SNAP [1.28], provides an alternative to the aforementioned material growth methods, with its own unique advantages. Namely, SNAP can be harnessed to produce large arrays of virtually any type of NW; the only limitation is that the material from which the NWs are made must begin as a thin film. The SNAP technique resides between NW materials growth methods (the template for SNAP NWs is grown) and traditional top-down patterning methods. Figure 1.3 presents a flow diagram of the SNAP process. The process details can be found in [1.28].

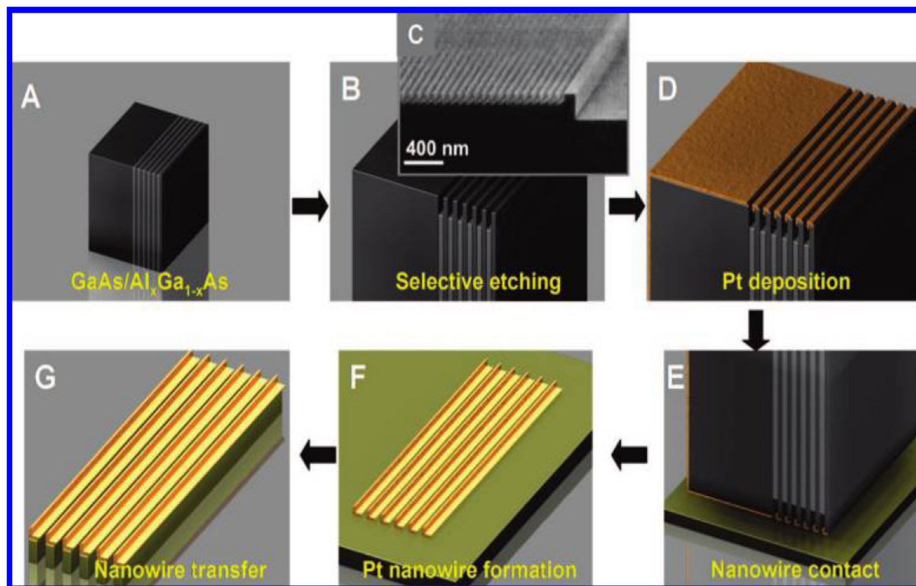

Figure 1.3 The SNAP process: (A) A piece of a GaAs/Al$_x$Ga$_{1-x}$As superlattice serves as the master, (B) the superlattice is differentially etched, leaving a comb-like structure, (C) a SEM micrograph of an etched master is shown, (D) metal (typically Pt) is evaporated onto the master, (E) the master is dropped onto a substrate pre-coated with a thin epoxy layer, (F) the interface between the evaporated metal and the superlattice is etched, leaving nanowires on the surface, (G) dry etching translates the metal nanowire array into the supporting substrate. [1.28]

SNAP NWs have other advantages compared to standard methods. First, they inherit their doping levels, stoichiometry, crystallographic orientation, and thickness from the thin film substrate

from which they are made. This means, for example, that p-type and n-type Si NWs can be readily prepared side by side and that pn diodes and other devices are readily obtained. Some NW materials are uniquely available using SNAP, including insulators and certain metals. Second, the width and pitch of an array of SNAP NWs are translated from the precisely controlled film thicknesses and spacing of the superlattice template (figure 1.3a). Arrays containing 10^3 or more non-touching, well-conducting NWs with NW widths as thin as 7±2 nm and at a NW array pitch of 13±2 nm have been prepared. No other method can approach these dimensions with such precision. Third, SNAP NWs may be a millimetre long or longer. Materials grown NWs typically have lengths of 10 μm or less. Long NWs can exhibit unique physics, and they enable the construction of relatively large-scale NW circuits. The SNAP process has evolved into a tremendously versatile method that is unmatched in terms of its capability for producing high-quality nanowire arrays. The development of the SNAP process over the past few years was largely driven by the goal of developing an electronics-grade manufacturing approach that operated at macromolecular dimensions. Several benchmarks toward achieving this goal, including the fabrication of ultrahigh density memory, novel de-multiplexing structures, and complementary symmetry nanowire logic circuits, have been achieved.

Another approach is the nanowire lithography (NWL) [1.29]. This technique uses chemically synthesized NWs (CS-NWs) or nanotubes as nanomasks to etch conformal one-dimensional (1D) structures into an underlying thin film. Initially, this method was applied to metal films or SiO_2. Colli et al. in [1.30] showed that SiO_2 NWs are a simple and compatible system to implement NWL on Silicon on Insulator (SOI) films and silicon wafers in general. The process steps are shown in figure 1.4. This unique combination of bottom-up and top-down fabrication allows us to achieve nanoscale features on SOI wafers with minimum processing effort. They demonstrated a variety of device concepts and architectures, from highly conductive NW networks to aligned arrays of vertically stacked NWs, showing that the potential of this approach goes far beyond planar ultra miniaturization, extending to very-large-area pattering and 3D electronics [1.30].

The use of CS-NWs as nanomasks for SOI lithography has in principle several advantages over their direct implementation as active device elements. For example, even by using a poorly conducting network of CS-NWs as mask, the resulting conformal network etched into the underlying wafer would be monolithic, with single-crystalline bulk junctions, allowing maximum performance. In addition, a precise control over the doping concentration and crystallographic direction of CS-NWs is still lacking, while for SOI-NWs these parameters would be accurately

determined by the initial properties of the SOI substrate and the relative orientation of the NWL mask.

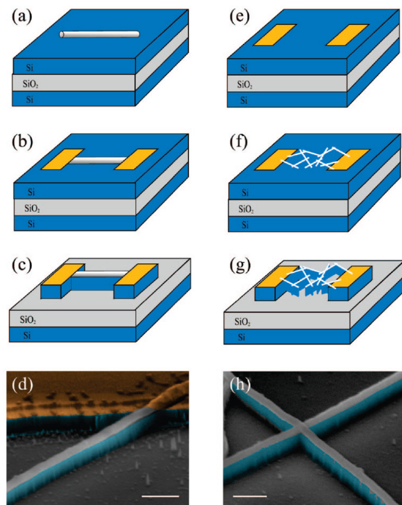

Figure 1.4 Complementary fabrication routes for direct-bridge (left) and network-like (right) NW devices using NWL on SOI layers. (a) Dispersion of fully oxidized Si NWs, (b) lithographic patterning of metal contacts, (c) etching of SOI by DRIE to define NW channels, (d) SEM micrograph of the final architecture, Different colours indicate different materials: (gray) SiO_2 ,(blue) Si,(yellow) metal. Scale bar is 200 nm. (e) Patterning of metal pads on SOI, (f) deposition of SiO_2 NW network from solution by spin casting or ink-jet printing, (g) etching of SOI by DRIE. A monolithic Si network with single-crystalline bulk junctions is carved into the SOI layer. (h) SEM micrograph of a monolithic Si junction with overlapping NW masks. Scale bar is 200 nm. [1.30]

Another fabrication techniques which is not relied on bottom up growth method such as VLS mechanism, is the nanoimprint lithography (NIL) [1.31]. NIL was employed to fabricate crossbar structures with half-pitch down to 17 nm, isolated nanowires with 6 nm line width, and other functional applications for nanoelectronics and nanophotonics. While the resolution of nanoimprint has exceeded that of photolithography, it is still in the nascent phases of development. Fundamentally, nanoimprint is a mechanical contact rather than optical process, and therefore has a different set of challenges: how to preserve alignment and the subsequent overlay during mold approach, how to apply contact force uniformly, and how to prevent air from being trapped between the mask and the substrate (figure 1.5). Conventional approaches to meet those challenges have been to improve the mechanical stability of the system and to use ultra flat templates and double-sided polished wafers; these inevitably add cost that can potentially take away the value advantage of NIL. The mold or template is a 5 in. photo mask. The key enablers of the concept were spacers with precise heights deposited around the imprint areas. These spacers, which are located outside the perimeter of the imprint field (i.e., the streets), spatially offset the wafer from the mask while maintaining the two surfaces within a short distance and close parallelism during the fine alignment phase. These are critical both for keeping the mask and wafer alignment marks simultaneously in focus and for maintaining the alignment during approach and contact. Indeed the precise control of

the spacer heights is critical, but this is not a challenge as today's deposition and etching processes easily give features with better than one nanometer thickness uniformity.

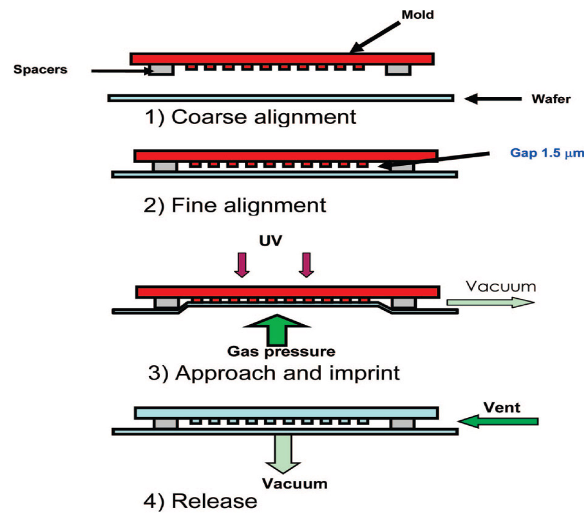

Figure 1.5 Schematic diagram of the nanoimprint module work flow. [1.31]

The nanoimprint process is divided into the following steps: (1) coarse alignment, (2) fine alignment, (3) approach and imprint, and (4) release (figure 1.5). Coarse alignment is performed without the mask and substrate in contact with an accuracy of 1 μm, after which the mask (more specifically the spacers on the mask) are brought into contact with the substrate. During fine alignment, the spacers slide on the streets of the substrate to keep the mask and substrate exactly parallel with a gap the same as the spacer height. It is important to point out that the sliding occurs only during the fine alignment and its magnitude is <1 μm; the spacers are designed to be located in the street area on the substrate, so that no patterns will be destroyed during spacer sliding. In approach and imprint, the air between the wafer and the mask is pumped out and gas pressure can be applied to the backside of the wafer (or the mask). The wafer and the mask are pressed onto each other because one or both bow under the applied pressure, transferring the patterns into the resist. The nanoimprint resist is then cured by exposure to Ultra-Violet (UV) light. To facilitate the release of the mask from the wafer, air is vented into the gap between the wafer and the mask and a vacuum is applied to the backside of the wafer, after which the imprint process is completed.

This approach has the following advantages: (1) there is no local mechanical movement other than wafer bowing during the approach and imprint, thus preserving the alignment during the process, (2) the mask and the substrate are in contact through the spacers during the fine

alignment step, so that the mechanical path between the nanoimprint mask and substrate is minimized for better mechanical stability, (3) the wafer-bowing method ensures that the imprint pressure is uniform and without lateral components in the imprint field, (4) during the imprint process, the centre of the imprint area reaches contact first and then spreads out to the edges, preventing air from being trapped between the mask and substrate and (5) the mold and wafer separation is facilitated simply by releasing the gas pressure.

1.2.5 Heterostructures of nanowires

The preparation of nanowires with a graded composition or with a superlattice structure along their main axis was demonstrated by controlling the gas-phase chemistry as a function of time during the growth of the nanowires by the VLS method. Control of the composition along the axial dimension was also demonstrated by a template-assisted method, for example by the consecutive electrochemical deposition of different metals in the pores of an alumina template. Alternatively, the composition can be varied along the radial dimension of the nanowire, for example, by first growing a nanowire by the VLS method and then switching the synthesis conditions to grow a different material on the surface of the nanowire by CVD. This technique was demonstrated for the synthesis of Si/Ge and Ge/Si coaxial (or core-shell) nanowires, and it was shown that by a thermal annealing process, the outer shell could be formed epitaxially on the inner core.

Radial core/shell heterostructures can be achieved if dissociation of the reactants is promoted at the grown nanowire surface, analogous to the layered growth of planar heterostructures. Compared with NWs in the simple homogeneous form, core/shell heterostructure NWs offer better electrical and optical properties as they can now be tailored through band structure engineering [1.42]. Unlike radial heterostructures in which the shell growth does not involve reaction with the nanocluster catalyst, axial nanowire heterostructures can be obtained by alternative introduction of vapor phase reactants that react with the same nanocluster catalyst. A critical requirement of the axial nanowire heterostructure growth is then that a single nanocluster catalyst can be found which is suitable for growth of the different components under similar conditions [1.42].

1.2.6 Properties of semiconductor nanowires

Quantum confinement properties

By now, the phenomenon of charge carrier confinement in quantum dots, wires, and wells is familiar to researchers working with nanostructures. Quantum confinement is approximately described by simple particle-in-a-box type models, and its most distinctive signature is the $1/d^n$ (where d is the diameter and $1 \leq n \leq 2$) size dependence of the band gap in semiconductors. A recent detailed study of the effect of dimensionality on confinement in InP dots and wires [1.32] concluded that the size dependence of the band gap in wires is weaker than in dots by the amount expected from simple theory. However, the absolute band gap shifts in InP dots ($\Delta E_g \sim 1/d^{1.35}$) and wires ($\Delta E_g \sim 1/d^{1.45}$) did not follow the particle-in-a box prediction (i.e., $1/d^2$), demonstrating that accurate treatments of confinement require higher-order calculations to account for band structure.

Electrical transport regimes

The study of electrical transport properties of nanowires is important for nanowire characterization, electronic device applications, and the investigation of unusual transport phenomena arising from one-dimensional quantum effects. Important factors that determine the transport properties of nanowires are first the geometrical dimension of the nanowire, in other words the wire diameter and length, which is important for both classical and quantum size effects. The electronic transport behaviour of nanowires may be categorized based on the relative magnitude of four length scales: the phase coherence length, the carrier mean free path ℓ, the de Broglie wavelength of electrons λ_e, and the wire diameter d. Besides this, the material composition, the surface and nanowire/dielectric interface conditions, the crystal quality, and the crystallographic orientation along the wire axis (for materials with anisotropic material parameters, such as the effective mass tensor, the Fermi surface, or the carrier mobility) play also a crusial role for the electrical transport.

Electronic transport phenomena in low-dimensional systems can be roughly divided into two categories according to their length (l): ballistic transport and dissipative transport. Ballistic transport phenomena occur when the electrons can travel across the nanowire without any scattering. In this case, the conduction is mainly determined by the contacts between the nanowire and the external circuit, and the conductance is quantized into an integral number of universal conductance units $G_o = 2e^2/h$ [1.33]. Ballistic transport phenomena are usually observed in very short quantum wires, such as those produced by using mechanically controlled break junctions (MCBJ) [1.34] where the electron mean free path is much longer than the wire length and the conduction is a pure quantum phenomenon. Another requirement to observe ballistic transport is that the thermal energy obey the relation $k_B T < e_j - e_{j-1}$, where $e_j - e_{j-1}$ is the energy separation between subband levels j and (j – 1). On the other hand, for nanowires with lengths much larger than the carrier mean free path, the electrons (or holes) undergo numerous scattering events when they travel along the wire. In this case, the transport is in the dissipative regime, and the conduction is dominated by carrier scattering within the wires, due to phonons (lattice vibrations), boundary scattering, lattice and other structural defects, and impurity atoms. Recent work showed that the transition from ballistic to dissipative behaviour would be limited to wire lengths of only 2–3 nm for Si case and around 180 nm for InAs nanowires [1.35].

For wire diameters much larger than the carrier mean free path ($d >> \ell$), the nanowires exhibit transport properties similar to bulk materials, which are independent of the wire diameter, since the scattering due to the wire boundary is negligible compared to other scattering mechanisms. For wire diameters comparable or smaller than the carrier mean free path ($d \sim \ell$ or $d < \ell$), but still much larger than the de Broglie wavelength of the electrons ($d > \lambda_e$), the transport in nanowires is in the classical finite size regime, where the band structure of the nanowire is still similar to that of bulk, while the scattering events at the wire boundary alter their transport behaviour. For wire diameters comparable to the electronic wavelength $d \sim \lambda_e$, the material band structure and the electronic density of states is altered dramatically and quantum subbands are formed due to the quantum confinement effect at the wire boundary.

Therefore, the transport properties for nanowires in the classical finite size and quantum size regimes are highly diameter-dependent because of the enhanced surface to volume ratio of nanowires, their transport behaviour may be modified by changing their surface conditions. For example, researchers have found that by coating n-InP nanowires with a layer of redox molecules, such as cobalt phthalocyanine, the conductance of the InP nanowires may change by orders of

magnitude by altering the charge state of the redox molecules to provide bistable nanoscale switches.

The larger diameter semiconducting nanowires are expected to be described by classical physics, since their quantization energies are usually smaller than the thermal energy $k_B T$. By comparing the quantization energy with the thermal energy, the critical wire diameter below which quantum confinement effects become significant is estimated to be 1nm for Si nanowires at room temperature, which is much smaller than the size of most of the semiconducting nanowires that have been investigated so far. By using material systems with much smaller effective carrier masses m^*_e (such as bismuth), the critical diameter for which such quantum effects can be observed is increased, thereby facilitating the study of quantum confinement effects. It is for this reason that the bismuth nanowire system has been studied so extensively. Furthermore, since the crystal structure and lattice constants of bismuth nanowires are the same as for 3D crystalline bismuth, it is possible to carry out detailed model calculations to guide and to interpret transport and optical experiments on bismuth nanowires. For these reasons, bismuth can be considered as a model system for studying 1D effects in nanowires.

1.3 Nanowire- based transistors

1.3.1 General characteristics

In the previous section, we described that the fabrication technology of NW channels can be broadly categorized into two groups, namely, 1) the bottom–up approach and 2) the top–down approach. In the case of bottom–up approach, the wire channels are synthesized, for example, using VLS chemistry, typically with the help of a metal catalyst. In the top–down approach, the NWs are prepared in place utilizing lithography and etch processes, followed by trimming or stress-limited oxidation techniques. Integration of top–down-fabricated NWs in circuit functionality is straightforward, while the bottom–up approach faces a daunting challenge of assembling the wires into circuit functions.

FET devices based on NW grown with bottom-up fabrication techniques

Si NWs have been most extensively studied partly due to the dominance of Si devices in the semiconductor industry and partly due to the well-developed recipes to grow Si NWs with controlled size and doping level. In typical device geometry, the NWs are first transferred into liquid suspension after growth via gentle sonication, and then dispersed on a degenerately doped Si substrate with a SiO_2 thermal overgrowth layer, as shown in figure 1.6. FET devices can then be studied after source–drain electrode formation, which is normally carried out, by e-beam or photolithography (with the degenerately doped Si substrate serving as the back gate). In most cases, unlike conventional MOSFETs in which degenerately doped Si forms the source (S) /drain (D) contacts, metal contacts are commonly used in a nanowire device. In this regard, a nanowire FET device is essentially a Schottky barrier device [1.36]. Typically, positive Schottky barriers (the metal work function is higher than the electron affinity for n doped material) are observed at the metal/semiconductor interface due to the combined effect of metal work function and Fermi level pinning by surface states. As a result, the device performance is to a large degree affected by the contact properties.

For example, Cui et al observed [1.37] that after thermal annealing which was believed to improve the source/drain contacts, the average transconductance of the Si NW devices increased from 45 to 800 nS and the deduced average mobility, μ, increased from 30 to 560 cm^2 $(V\ s)^{-1}$. In Cui's study, boron-doped (p-type) Si NWs with diameters in the range of 10–20 nm were used. The nanowire FETs were fabricated using Ti S/D contacts, and transport characteristics were studied as a function of annealing. Ti was used since it is known that Ti can form a stable conducting silicide with a low Schottky barrier height on p-type silicon [1.38]. Figure 1.7a shows the current (I_D) versus source– drain voltage (V_{SD}) behaviour of a typical Ti-contacted Si NW device before and after thermal annealing. In general, the $I–V_{SD}$ curves become more linear and symmetric, and the transport behaviour becomes more stable after annealing, with the measured conductance increasing by 3-fold. To characterize the reproducibility of these observations, similar measurements were made on over 50 devices. These results are summarized in a histogram showing the frequency that different values of two-terminal resistance were observed (figure 1.7b). Before annealing, the resistance shows a large distribution ranging from ~MΩ to larger than GΩ with an average of 160MΩ. In contrast, the resistance after annealing has a narrower distribution of 0.1–10MΩ with an average of 0.62MΩ; that is, a 260-fold improvement in the two-terminal conductance. The increased two-terminal conductance and stability can be attributed in part to better metal Si NW

contacts, although passivation of defects at Si–SiO_x interface, which can occur during annealing, may also contribute to the observed enhancements.

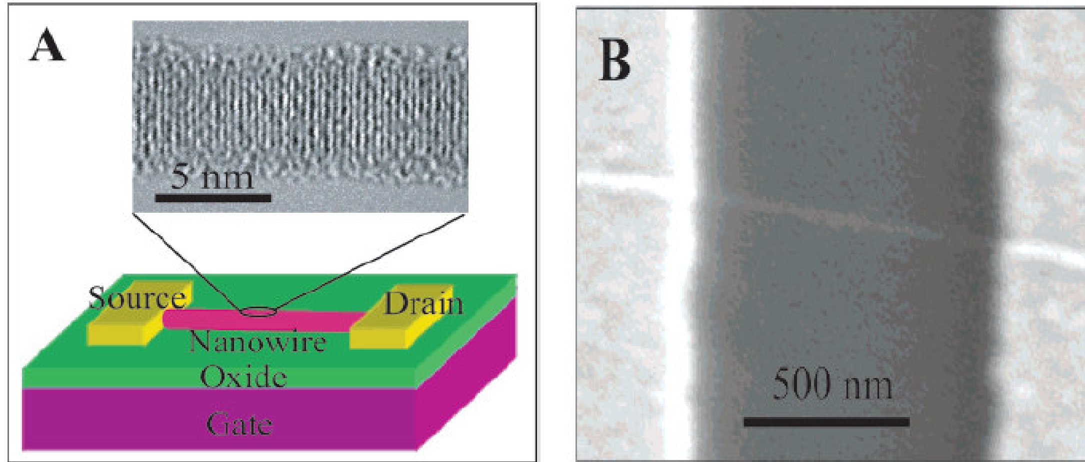

Figure 1.6 (a) Schematic of a Si NW FET showing metal source and drain electrodes with the NW and contacts on the surface of SiO_2/Si substrate. (inset) High-resolution TEM of a 5 nm diameter SiNW; the scale bar is 5 nm. (b) SEM of a SiNW FET device; the scale bar is 500 nm.[1.37]

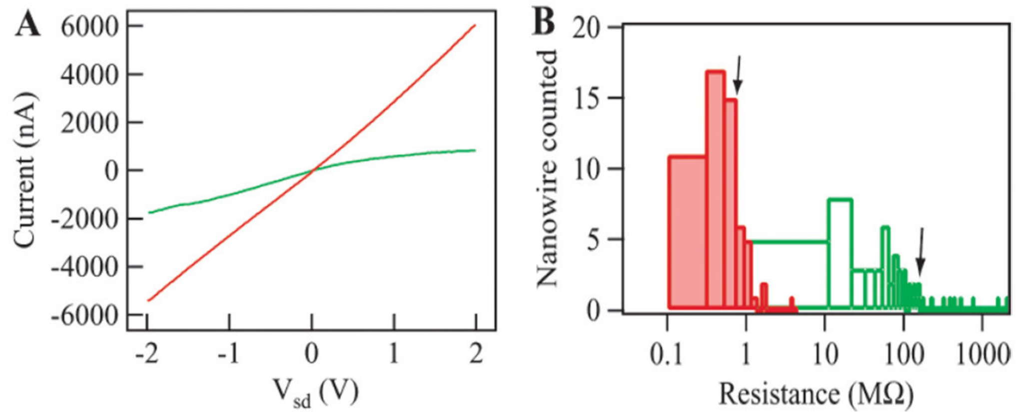

Figure 1.7 (a) I_D versus V_D measured on the same Si NW before (green) and after (red) thermal annealing, (b) histogram of Ti-contacted Si NW resistance determined from measurements before (open green bars) and after (filled red bars) contact annealing.[1.37]

Based on I_D-V_G (transfer) characteristics the electron mobility is estimated from the transconductance according to the formula

$$g_m = \frac{dI_D}{dV_G} = \mu\left(\frac{C}{L^2}\right)V_{DS} , \quad (1.1)$$

, where μ is the carrier mobility, C is the gate capacitance and L is the channel length of the device [1.39]. Although the real device capacitance is in the order of atto-Farad and it is difficult to be experimentally measured, it can be estimated by an approximated cylinder to plate capacitance model, which gives

$$C=2\pi\varepsilon\varepsilon_o L/\ln(2t_{ox}/r), \quad (1.2)$$

, where ε is the dielectric constant, t_{ox} is the thickness of the silicon oxide layer, r and L are the NW radius and length, respectively. In the case of highly doped nanowires, the back gated FET structure can be described as a capacitor having a cylinder, the nanowire, as one plate and as the other plate the highly-doped substrate. This capacitor model is widely used in NWFETs, despite the fact that underestimates the real value of the capacitance. In the case of highly doped nanowires, the carrier concentration can be estimated by using the formula

$$I=nq\mu EA, \quad (1.3)$$

, where I is the drain current, n the carrier concentration, q the electron charge, μ the mobility, E the electric field along the nanowire and A the area of nanowire cross section [1.46]. At this point, we would like to explain why the combination eq. 1.1 and eq. 1.3 can be used for the parameter extraction, although the first one is related with nanowire surface and the second with the bulk of nanowire. Most of the NWFET devices operate in the accumulation mode, which means that we do not have generation of inversion layer but in the contrary, the majority carriers carry the current through the formation of an accumulation layer. For example, in the case where the nanowire is n-type doped, positive gate voltages are used (instead of negative gate voltages) to modulate the current by creating an accumulation layer (instead of inversion layer). Apart from the surface contribution of the accumulation layer (varying part of the current by the gate control), we have a second contribution to the current due to the bulk of nanowire (volume contribution which is independent of the gate control). In eq. (1.3), we use the mobility value extracted from eq. (1.1) to estimate the carrier concentration along the nanowire. More appropriate would be to use the bulk mobility value instead of that in the accumulation layer (the bulk carrier mobility is higher than the corresponding value in the accumulation layer) in eq. (1.3) but from the electrical characterization only the surface (either inversion or accumulation) mobility can be calculated. This method leads to an overestimation of carrier concentration. In the case of highly doped NWs the error is less (the surface mobility is on the same order of magnitude with the bulk mobility). This is the standard way for the parameter extraction in NWFETs, despite the limitations noted above.

On the other hand, the measured transconductance g_{ex} with finite S/D contact resistances is reduced from its intrinsic value g_{in} to [1.40]

$$g_{ex} = g_{in} /(1 + g_{in}R_S + (R_S + R_D)/R_{in}), \quad (1.4)$$

where R_S and R_D are, respectively, the source and drain contact resistance, and R_{in} is the intrinsic NW resistance. From equation (1.4), it is clear that contact resistances can greatly influence the performance of nanowire transistors, and the extracted mobility using equation (1.1) may not reflect the true intrinsic mobility of the device. For example, in the extreme case when $R_S >> 1/g_{in}$, $g_{ex} \sim 1/R_S$ and becomes independent of g_{in}. Such a scenario can occur either when the contacts are poor or when high performance transistors are desired such that even a small R_S is unfavourable due to the large g_{in}. The important role of R_S in nanowire devices was reported by Zheng et al. [1.41]. Interestingly, Zheng et al. observed that the heavily doped devices (where the relative ratio between Si and P atoms is Si/P = 500) exhibit an apparent larger transconductance compared with the lightly doped devices (Si/P = 4000), at the same device geometry and bias voltage conditions. This observation, however, contradicts the predictions of equation (1.1), as the heavily doped NWs would suffer from increased impurity scattering and possess a lower mobility. Four-probe measurements lifted this discrepancy by revealing the increased effect of R_S in the case of low-doped nanowires. After the correction of the contact resistance effects using equation (1.4), Zheng et al. found that the estimated intrinsic transconductance could be up to four times larger than the value deduced from the raw data.

Si and Ge NWs have been the focus of recent studies of 1D FETs. However, metal contacts to single-component NW generally produce Schottky barriers that limit device performance, and scattering from charged dopants can reduce the intrinsic mobility of these NW devices. In contrast, Lu et al. [1.42] recently demonstrated transparent contacts and low-bias ballistic transport in undoped Ge/ Si core/shell nanowire heterostructures, with an estimated scattering mean free path of ~500 nm.

Cui et al. presented a comparison between the key characteristics of Si NW FETs with state-of-the-art planar MOSFETs fabricated using SOI [1.37] (table 1.2). First, the hole mobility, which is independent of channel length, is an order magnitude larger than that in planar Si devices with comparable doping concentrations. Since the mobility determines how fast charge carriers move in the conducting channel, it is one key parameter affecting the raw device speed. Ignoring other factors, the mobility implies that terahertz operation could be achieved in a ~2000 nm Si NW FET. For direct comparison of other key parameters, the Si NW FET results have been scaled using the SOI FET gate length of 50 nm and gate oxide thickness of 1.5 nm. Significantly, the scaled on-state

current (I_{on}) for the Si NW FET is larger than state-of-the-art Si FETs, and the average subthreshold slope approaches the theoretical limit, while the average transconductance is 10 times larger. These improvements could lead to substantial benefits for high-speed and high-gain devices. The Si NW FET devices also have larger leakage currents, but this issue could be addressed by implementing pn-diodes at the source and drain contacts as in conventional MOSFETs. This comparison suggests that efforts to make smaller Si NW FETs and explicitly test scaling predictions could have an important impact in the future.

Table 1.2: Comparison of the key device parameters between Si NW and SOI FET. [1.37]

	nanowire raw data	nanowire converted data	Planar Si device
gate length (nm)	800-2000	50	50
gate oxide thickness (nm)	600	1.5	1.5
mobility (cm^2/Vs)	230-1350	230-1350	150
I_{on} (μA/μm)	50-200	2000-5600	650
I_{off} (nA/μm)	2-50	4-45	9
subthreshold slope (mV/decade)	174-609	60	70
Transconductance (μS/μm)	17-100	2700-7500	650

FET devices based on NWs fabricated with top down techniques

Most of the reported data on the I–V characteristics of top-down fabricated GAA NW FETs show excellent gate control, near-ideal subthreshold behaviour, high I_{ON}/I_{OFF} ratio, and high drive current [1.43]. For instance, Singh et al. obtained I_{ON} values of 2.4 and 1.3 mS μm^{-1}, DIBL values of 8 and 13 mV/V, and SS of 60 and 65 mV/ dec for NMOS and PMOS, respectively [1.44]. The I–V characteristics of these GAA Si-NW devices with 3-nm diameter are shown in figure 1.8, where the current is normalized to diameter. Although it is a matter of debate, it is worth mentioning here that the typical trend in the contemporary NW literature is the normalization to diameter, which may be appropriate only with fully volume-inverted channels existing in the case of ultra narrow

undoped wire channels. With thicker wire where conduction remains at surface, it should be more appropriate to use perimeter for normalization. In Singh study, normalization to diameter for wire diameters up to 10 nm is used. Above 10 nm, normalization to perimeter is performed.

Table 1.3 gives the comparative list of device electrical and structural parameters reported in the literature, along with the best-reported FinFET performance. The top–down approach is highly integrable in circuit functionality and is compatible with the existing CMOS technology. NWs and nanostructures seem to have possible novel solutions in the "more-than-Moore" regime of applications such as in the area of fabrication of chemical/biochemical sensors. The presented top–down techniques can potentially address the needs of the "end-of-the-technology roadmap" and beyond CMOS era, possibly with the help of a hybrid approach.

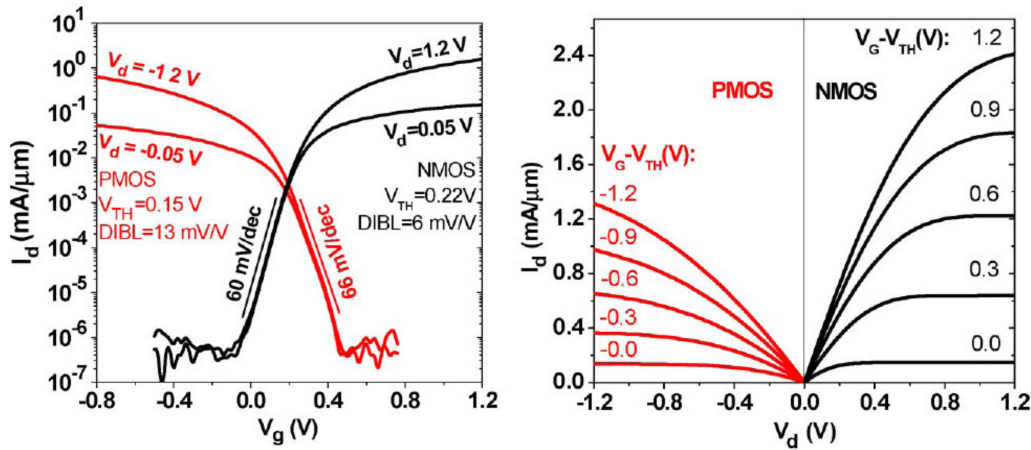

Figure 1.8 (a) Transfer characteristics of GAA n- and p-FETs showing near-ideal SS indicating the excellent electrostatic control, (b) drain current characteristics showing that high drive currents are possible in GAA FETs. [1.44]

Table 1.3 NW and FinFET transistor performance data

Device Type	Grown Nanowire		Top-Down Nanowire		Fin-FETs	
	N* [37]	P [38]	N [36]	P [27]	N [39]	P [39]
NW dia./Fin Width	20	15	10	8	25	25
Channel length (nm)	2000	40	8	15	40	40
Normalization method	diameter	diameter	diameter	diameter	$W_{FIN}+2*H_{FIN}$	$W_{FIN}+2*H_{FIN}$
I_{ON} (uA/um)	80	2100	3670	1940	1395	1140
I_{ON}/I_{OFF}	~10^4	~10^3	>10^6	>10^5	>10^4	>10^4
DIBL(mV/V)	-	-	28	43	89	101
SS(mV/dec)	300	140	73	71	76	82
V_{DD} (V)	5	-0.5	1	-1	1.1	-1.1

*Ion data is at V_G=5V and V_D=1V. W_{FIN} and H_{FIN} are fin width and height respectively.

Conclusion between bottom-up and top-down FET devices

Table 1.3 summarizes the performance comparison in terms of figure of merits between FET devices based on bottom-up and top-down nanowires. If we compare the absolute numbers we could say that bottom up nanowires have much higher on current and mobility values. This is due to the GAA device geometry and the radial heterostructures that are feasible in the case of bottom-up growth techniques. On the other hand, the scaling down process is much more easily in the case of top-down techniques, which are based on e-beam lithography process. This allows reaching extremely low SS values and high I_{on}/I_{off} ratio.

1.3.2 Device operation mode

Introduction

Due to the 1-D nature of the NWs, the simplest way to measure the electrical current passing through them is the implementation of a back gated FET (figure 1.6). After the NWs dispersion over the SiO_2/Si substrate, it follows a deposition of metal contacts, as source and drain regions, and through e-beam lithography and lift-off process, the device fabrication is finalized. This is the simplest process, which ends up to a SB-NWFET (Schottky metal-semiconductor contact). An annealing step usually follows aiming to the suppression of the SB. The non-uniformity of the final SB at S/D is the explanation, as we will present later (chapter 3), of the existence of various 'strange' I-V characteristics (symmetric linear, symmetric non-linear, asymmetric non-linear etc.) in the literature of NWFETs. Various reasons could be proposed in order to explain these different behaviours (even for devices belonging to the same sample) like variations of nanowire doping, local surface contamination etc.

The other more advanced way to fabricate a NWFET is by using implanted S/D regions (with inversed polarity from that of the channel doping) instead of using metal contacts directly to the nanowire. This method leads to more stable electrical results and similar to planar MOSFETs characteristics, and that is why these devices are named as Conventional (C)-NWFETs. This kind of

devices is unipolar, in contrast with SB-FETs, which are ambipolar (in the case where the SB has almost the same height for holes and electrons, otherwise if the SB of one type of carriers is much higher than the other then the device is unipolar).

SB-NWFET and C-NWFET

The research groups working on NWFETs with metal S/D regions are trying to suppress the SB by performing annealing steps. This is obvious from the I_D-V_D characteristics which are linear (especially at low V_D) in the most cases of SB-NWFETs (after the proper annealing). The linear behaviour shows that the SB is almost zero (or very thin so the tunnelling is very high, T(E)=1). Besides the annealing step, there are some other parameters that affect the relevant position of the Fermi level in the nanowire with the Fermi level of metal (SB height) or the 'thickness' of the SB. One parameter is the doping level of the nanowire. In the case of high carrier concentration, a very strong band bending and a short depletion region produce a very "thin" SB [1.45].

For better understanding of the influence of contacts on the operation mode of NWFETs, Hayden et al [1.49] used undoped silicon nanowires, grown by the VLS mechanism, to fabricate FETs in a lateral architecture. These NWFETs operated in accumulation or inversion mode, depending on whether Schottky (Ti Schottky contact) (type one: SB-NWFET) or implanted S/D contacts (type two: C-NWFET) (i.e. n-i-n structure) are used, respectively. In their first type of device, with metal as S/D areas, a normally on FET characteristic is measured without any current saturation at low V_D and operating in accumulation mode. In the case of their second type of device, the one with implanted S/D (C-NWFET), a normally off characteristic with clear current saturation is observed. The electrical transport properties indicated a fully depleted n-channel metal MOSFET in enhancement mode operating in inversion. As it is clear from the I-Vs (figure 1.9a) of the SB-NWFET, the I-Vs are not linear for small V_D. This shows that after the annealing step (e. g. due to the local geometry and chemical synthesis of the metal/nanowire contact) the contacts are not completely ohmic. In addition, the I-V is not symmetric, fact that shows that the SB of source was different from that in drain. The NWFET exhibits p-type behaviour (the current increases by increasing negatively the V_G), which means hole conduction. For this device, only accumulation of carriers (holes) was achieved and full depletion of the NW occurred for $V_{GS} > +6$ V (the carrier concentration is not as high as in [1.46, 1.47]). For higher positive V_G no conduction was observed. The fact that we have unipolar conduction shows that the SB for electrons is extremely high (there is an inversion layer in the nanowire for high positive V_G but due to the high SB, electrons cannot

overcome the barrier). The second type of device is characterized as C-NWFET [1.49]. The difference was an implantation step for S/D formation instead of using metal. The drain current values are linear for small V_{DS} values and a well-defined saturation region is observed for V_{DS}>2 V with saturation currents up to the microampere range (like as a C-MOSFET) (figure 1.9b). The NW n-i-n-MOSFET operates as a conventional enhancement-mode n-channel MOSFET in inversion mode, which is in strong contrast to the results from the Schottky contact NWFET.

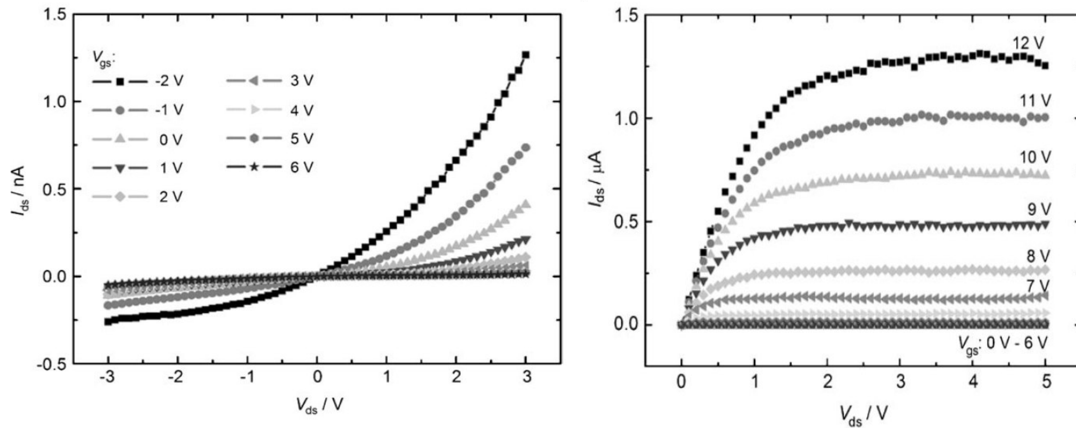

Figure 1.9 Output characteristics of a) SB-NWFETs and b) C-NWFETs. [1.50]

In [1.50], it is presented a simultaneous fabrication of a nanowire FET and a micro-wire (μW) FET. In this work, the effect of the different aspect ratio between NWs and μW is observed. The μW FETs were classified as ambipolar whereas in NW FETs only hole are significant. Given that the NW and μW FETs are fabricated side by side on the same substrate and have undergone the same processing sequences, the doping levels, crystal orientations, and electrical contacts should be identical. The only difference should be the increased surface-area-to-volume ratio for the NWs.

Cohen et al. [1.51] presented another work on this topic. They reported on the fabrication and electrical characteristics of *p*-FETs and *n*-FETs with a silicon nanowire as channel and doped silicon S/D regions. The difference with [1.50] is that the process that they used thickens the nanowire bodies in the regions where a source and a drain are formed similarly to the raised S/D approach followed in SOI technology. Unipolar characteristics were achieved in both n-FET and p-FET devices. The p-FET device exhibited unipolar transport, while reference FETs exhibited ambipolar characteristics. The ambipolar I_D-V_G exhibits higher hole current than electron current. This is probably due to the Ni forming a higher Schottky barrier for electrons (0.68 eV) than for holes. The effect of contact type is evident.

1.4 3C-SiC nanowires: Growth, properties and applications

1.4.1 Introduction

Recently, the growth and characterization of 1D nanostructures (nanowires, nanorods, nanotubes) of wideband- gap semiconductors have been extensively studied due to their potential for applications in nanoelectronics, sensors, batteries, and field emission displays (FEDs) [1.11-1.13]. Among the wideband-gap materials, SiC presents high thermal conductivity, high breakdown electric field, high electron drift velocity, high Young's modulus and hardness, high melting temperature, excellent oxidation and corrosion durability, high strength at elevated temperatures, good thermal shock resistance and excellent chemical and physical stability. The native oxide is silicon dioxide, which makes SiC more compatible with Si technology. SiC NWs combine the above properties of 1D material with that of SiC and electronic devices based on SiC NW are expected to present concrete advantages in terms of dissipated power, stability and high voltage operation in comparison to their Si (Ge) counterparts. In this section, we will review the various growth methods that were used to fabricate 3C-SiC NWs and summarize their application in FETs and other devices.

1.4.2 Growth of 3C-SiC nanowires

Conversion of Carbon NTs to 3C-SiC nanowires

In the beginning of the previous decade, 3C-SiC nanowires were produced by several routes: carbothermal reduction of silica, decomposition of organic silicon compounds, and reaction between silicon halides and CCl_4. Generally, these nanowires have diameters of about half a micrometer (not suitable for micro/nanoelectronic applications). For the production of smaller diameter NWs, CNTs were used as templates, spatially confining the reaction into the nanotubes, to make SiC NWs. Zhou and Seraphin [1.54] developed a process for producing SiC NWs through a reaction between CNTs and SiO (powder form), but the size of the SiC NWs were typically much

larger than the CNTs. However, H. Dai et al. successfully synthesized SiC NWs whose diameters were similar to or much smaller than the diameters of the CNTs through a reaction between the CNTs and SiO or SiI_2 [1.55].

A later study was accomplished from Han et al. [1.56]. A two-step reaction scheme has been employed for the synthesis of SiC NWs at 1400 °C. SiO vapour was generated via the silicon reduction of silica, and then this SiO vapor reacted with CNTs to form SiC NWs. The NWs were single crystalline SiC with the diameters ranging from 3 to 40 nm. Since the starting CNTs used by Dai et al. and Han et al. are randomly distributed, the formed SiC NWs also have a disordered structure, which restricts investigation of both properties and applications of the NWs. Thus, it is desirable to be able to prepare oriented SiC NWs. Pan et al. [1.57] were the first who demonstrated the synthesis of oriented SiC NWs by reacting aligned CNTs with SiO (at 1400 ^{o}C for 2 h) having diameters ranging from 40-100 nm. TEM images revealed a high density of stacking faults. A systematically time dependent TEM analysis revealed the key growth steps of the CNTs conversion to SiC [1.58].

3C-SiC NW growth based on VLS mechanism

The first experiments for SiC NWs growth (with small diameter) based on VLS mechanism were implemented through Hot Filament Chemical Vapor Deposition (HFCVD). Chen et al. [1.52] accomplished the first experiment at this field by fabricating well-aligned graphitic nanofibers on a large scale on Si (100) wafers by plasma-assisted HFCVD using a mixed gas of nitrogen and methane. The discharge plasma and its uniformity were the key for the growth of aligned fibres. The growth direction of the fibres was perpendicular to the substrate surface and the plasma-induced Ni particles serve as a catalyst. The diameter of the fibres was in the range 50-500 nm, mostly between 100-200 nm, controlled by the size of the nickel particles (characteristic of VLS mechanism).

In a later study of X. T. Zhou et al [1.53], they reported an approach for the synthesis of SiC NWs from solid sources of Si and C by the HFCVD method. This process is catalyzed by metallic particles which come from impurities in the solid source (solid plate) which is a plate made by pressing a mixture of graphite and silicon powders at 150 °C. The NWs consisted of a crystalline 3C-SiC core with an amorphous silicon oxide shell layer and grew along the (100) direction. The nanorods were 10–30 nm in diameter and less than 1 mm in length. Contrary to the inert atmosphere

used for the growth of CNTs or Si NWs by arc discharge, laser ablation, or high temperature evaporation, atomic hydrogen was produced by and in the vicinity of hot filaments in CVD chamber. The atomic hydrogen etched the solid plate and produced gaseous hydrocarbon radicals (CH_x), hydrosilicon radicals (SiH_x), or organosilicon molecules. When these vapor molecules reached the vapor–liquid surface, they were dissociated into Si and C atoms. These atoms were dissolved into the liquid catalyst, which upon supersaturation, induced solid SiC precipitation onto the substrate. As precipitation continued, the NW grew, lifting the catalyst particle from the substrate and forming a NW.

Initial effort of our Korean collaborators. Seong et al. [1.46, 1.47] fabricated SiC NWs towards the aim of SiCNWFET development, by using a Chemical Vapor Deposition (CVD) process, and had diameters of ~100 nm and lengths of several mm. The growth of 3C-SiC NWs was carried out in a horizontal hot-wall CVD furnace. Thermally oxidized Si wafers with a sputtering deposite two nm layer of Ni were used as initial substrates. During the growth process, the substrates were placed in the central region of an inner quartz tube reactor surrounded by an outer alumina tube. Methyltrichlorosilane (MTS, CH_3SiCl_3) was chosen as a source precursor due to the 1:1 ratio of Si and C and the low decomposition temperature. H_2 was used as both the carrier gas, which transfers the source precursor through a bubbler to the quartz reactor and as a diluent gas, which regulates the concentration of the mixture containing MTS vapor and carrier gas. The diluent and carrier gas, containing MTS vapor, was completely mixed before its introduction to the reactor. Typically, the system was heated up to 950 °C under a flow of H_2 at a rate of 1000 cm^3 min^{-1} and maintained at this elevated temperature for 5 min. During this time, the MTS was added to the flow of H_2 at a rate of 5 cm^3 min^{-1}, and then the system was cooled down to room temperature.

X-ray diffraction (figure 1.10) and TEM analysis showed highly oriented NWs with a preferable growth direction of (111) (zinc blend structure 3C–SiC). The NWs were nearly perfect single crystalline (apart from the main direction (111) there are two more peaks (200) and (220) that destroy the single crystalline nature of the NWs) with few intrinsic defects such as stacking faults that are also observed in bulk or thin film SiC. Photoluminescence characterization showed blue emission at room temperature (Figure 1.10c). As compared to bulk and/or thin film SiC, the blue-shifted emission (by few nm) could be attributed to either quantum confinement effects or simple defects that have not been addressed yet [1.46]. At this point, we have to mention that we fabricated devices based on this kind of 3C-SiC nanowires in collaboration with Prof. S. K. Lee group from Korea. These nanowires are representative of the state of the art SiC NWs grown. Electrical characterization of SiCNWFETs will be presented in chapter 3.

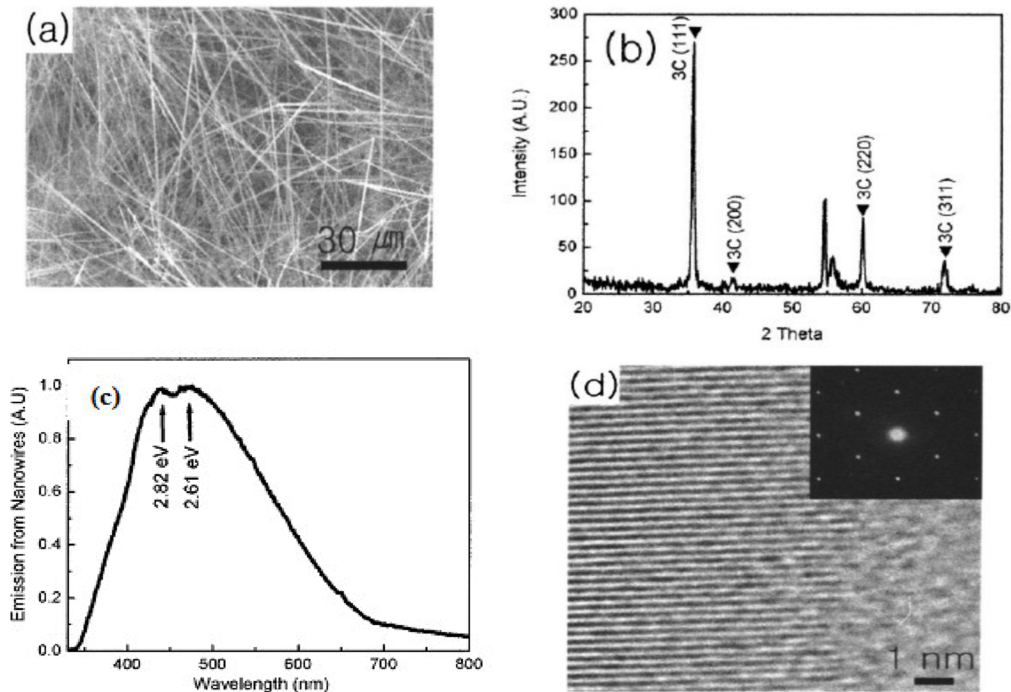

Figure 1.10 (a) Typical SEM image of 3C-SiC NWs grown on substrates, (b) XRD pattern of the sample, (c) Photoluminescence spectrum measured at room temperature, (d) high-resolution TEM image of the individual 3C-SiC NW. Inset is SAED pattern recorded along the [110] zone axis [1.46].

Growth through direct heating without catalyst

X.W. Du et al [1.59] presented a simple and convenient approach to grow SiC NWs directly on Si substrate by heating single-crystal Si wafer and graphite without metal catalysts. The diameter of SiC NWs was in the range of 10–30 nm, and the length was up to a few millimeters. Two kinds of SiC NWs, namely pure SiC NWs and SiC/SiO_2 coaxial composite NWs, formed at higher temperature and lower temperature, respectively. A multiple-reaction model was proposed to explain the formation of SiC NWs.

Effort of our collaborators from the University of Lyon. Recently, a breakthrough in the mass production of 3C-SiC-based nanostructures was achieved with the discovery of a commercially competitive method based on a VS growth mechanism, which allowed for the fabrication of large amounts of 3C-SiC NWs with tuneable geometric features and surfaces, without usage of catalyst, that could potentially be chemically modified in situ [1.60]. The set-up consisted

of an alumina boat containing Polypropelane (PP), followed by a second alumina boat containing an equimolar mixture of Si(s) and SiO_2 (s), which was partially covered by a graphite condensation plate. The entire setup was placed into the hot-zone of the alumina tube of a convective furnace equipped with two water-cooled flasks at each ends. All of the experiments were conducted under argon at a very low flow rate (10 mL min^{-1}), heated to 1400 °C, and maintained at this temperature 7 for 10 h. Following this method and by adjusting the concentration of the precursors, radial heterostructures such as SiC/SiO_2, SiC/BN, SiC/C could be prepared.

These NWs have been extensively studied over the last few years by SEM, TEM, and Raman spectroscopy and have been used as cantilevers in mechanical resonance experiments. In particular, TEM studies showed that the NWs were single-crystalline 3C-SiC with various concentrations of stacking faults and covered by a native oxide layer of several nanometers (figure 1.11). The stacking faults, which can be seen as inclusions of other polytypes into 3C-SiC, can lead to variable band gaps along the NW. If we compare the quality of these NWs with that grown by Seong et al. based on XRD spectra and TEM characterization, we observe same material quality in terms of stacking faults density, crystal orientation etc. (figure 1.11). We also fabricated devices based on this kind of NWs. In chapter 3, we will refer in more detail on the characterization of these devices.

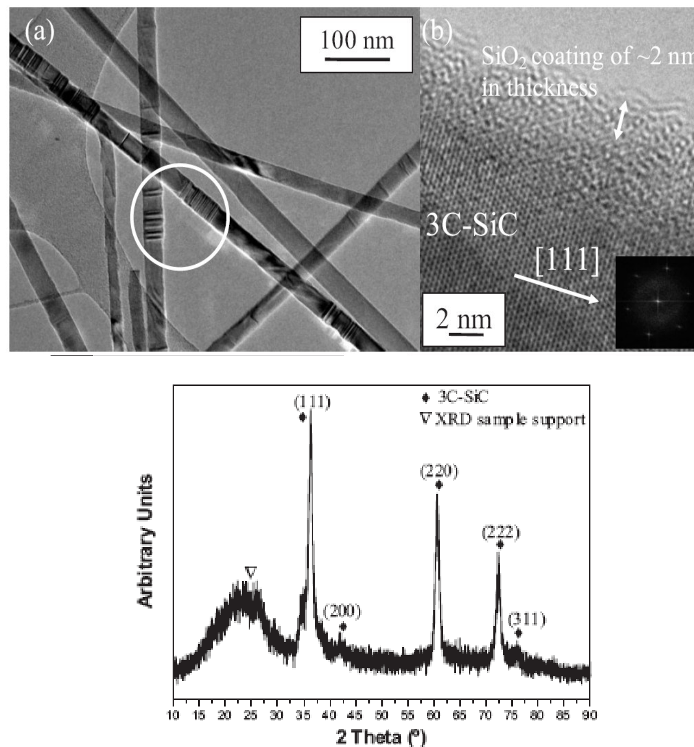

Figure 1.11 a) Conventional TEM image. Stacking faults are marked by a white circle, b) HRTEM image of a typical NW 40 nm in diameter [1.60], c) XRD spectrum.

1.4.3 3C-SiC NWFET

There are many device applications in which nanowires could be used instead of standard bulk materials, presenting improved performance. The first main device application is related with the CMOS technology. Due to their 1D nature, new device concepts could be implemented such as radial/axial heterostructures leading to devices with enhanced performance. The low density of states of nanowires, allows us to reach the quantum capacitance limit where the maximum of the potential energy along the electrical transport direction is controlled by the gate voltage and not by the carrier charge of the drain voltage. Furthermore, the confinement of the scattering phase space in one dimension, the subband modulation and the volume inversion are expected to improve the carrier mobility. A GAA device architecture is easily implemented in nanowire devices specialized for electrical applications, leading to improved electrostatic control of the carriers. Finally, the high package density and the 3D integration are expected to significally lower the device cost.

On the other, bulk SiC is a promising material for transistors (and sensors) operating at high temperatures (and/or high operating voltages) or hostile environments due to its wide band gap and excellent chemical and physical stability. Nowadays, the first priority of the microelectronic industry is to face the problem of the high temperature raised in the ultra scaled down integrated circuits. The increasing package density of integrated circuits has as a result the even higher temperatures at which devices should still be operational (ITRS 2003). As a first solution to this temperature issue, the microelectronic industry initiated the multicore processor (e. q. dual core) production. Another approach could be the usage of wide band gap semiconductors at least for some high temperature applications. For example, MOSFETs based on Si have an upper temperature limit where the device is operational ~200 ^{o}C. On the other hand, wide semiconductors and especially SiC could easily extend this limit to over 250 ^{o}C. If we also take in account the three times higher thermal conductivity of SiC, we can realize that issues related with the thermal energy removal and the high temperature operation, which are among the two more severe problems which CMOS technology is facing nowadays, could be resolved in a better way in SiC case.

In the previous section, we presented many different growth techniques, which have been used for SiC NW growth. Despite the fact, that many SiC NWs were grown (following different method), only two studies (in the beginning of this thesis) on 3C-SiC nanowire FETs were published (due to difficulties in the device fabrication), both presenting similar low device performance in terms of transconductance and mobility [1.46, 1.48]. The main factor affecting the device performance is the high unintentional doping, which might come from the high density of

stacking faults, donors traps or uncontrolled contaminations during the growth of NW (e.g. nitrogen). Typical electrical characteristics of state of the art SiC NW based FETs before 2006 are shown in figure 12. From the I-V curves is obvious the weak gating effect originating from the high carrier concentration.

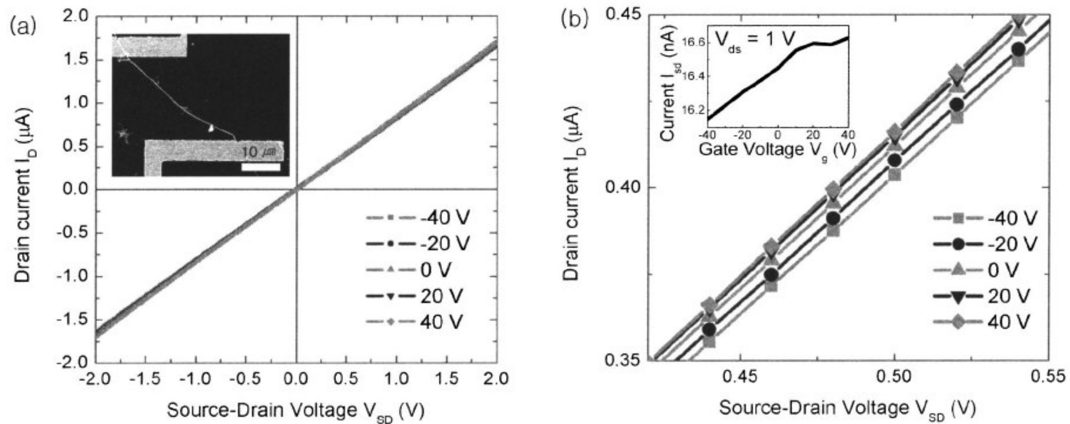

Figure 1.12 : (a) I–V characteristics of SiC nanowire device contacted with Ti/Au electrodes after annealing at 700 °C for different back gating from −40 V to 40 V. Inset is SEM image of SiC two-terminal nanowire device. (b) Enlarged plot of (a). Inset is current versus gate–voltage data of same device at V_D=1 V [1.46].

In contrast to these experimental electrical results, theoretical studies indicated that SiC NW offers good opportunities for developing various devices [1.61]. For example, high-temperature operation sensors, detectors and actuators based on 3C-SiC NWs could be designed by utilizing the characteristics of 3C-SiC NWs (e.g., low resistivity, thermal stability etc) [1.46]. Improvements on high temperature properties of SiC NW devices have been theoretically predicted by means of simulations based on classical molecular dynamics [1.62], but they should be confirmed via a full quantum treatment of both electron and phonon transport within for example NEGF formalism.

1.4.4 Other applications of 3C-SiC NWs

i) <u>Field emission (FE) cathodes</u>

In general, for FE applications a high aspect ratio is highly desirable. In the formula for the emission current calculation, a geometrical enhanced parameter, β, plays an important role. This geometrical parameter depends on the ratio between the length and the diameter of the material. In

the case of nanowires, this aspect ratio is considerable increased compared to bulk materials. Apart from the geometry of the material, another important parameter is the low electron affinity that permits the emission of electrons for lower applied electric fields and leads to higher emission current density. The low electron affinity provides an extra advantage for SiC compared to Si for FE applications. If we also take in account, the superior chemical and physical stability of SiC that result to a longer lifetime of the device, we could conclude that SiC is a good material for FE applications.

Early publications have evidenced good FE properties of SiC nanowires/nanorods [1.63]. In a more recent study, Spanakis et al. [1.69] presented results of the attempt to produce arrays of sharp SiC electron emitters by ultraviolet pulsed-laser processing of single-crystal SiC surfaces. This simple one-step technique, has demonstrated efficient SiC cold cathodes both in terms of current density and of emission threshold. The corresponding cathodes have a lower emission threshold and produce higher current densities than their Si-based counterparts. Moreover, Kim *et al*. [1.64] reported the fabrication of diode-type FED devices with 3C-SiC NWs-based cathodes, which demonstrated excellent FE properties at low applied voltages/electric fields and stable long-term performance. The obtained results point out that 3C-SiC NWs show great promise for applications in FED.

ii) <u>Thermoelectrical applications</u>

There is a growing interest in thermoelectric power generation, which allows direct conversion of thermal energy into electrical energy. Thermoelectric energy conversion has many technical advantages over other methods. However, the materials developed so far are easily oxidized, decomposed or melt above 1000 °C and thus limit the efficiency of the devices. Increasing the temperature difference can improve the efficiency. Therefore, the development of high temperature thermoelectric materials is of special interest. Recent development and investigations showed that SiC is promising candidates for high temperature applications because of their high thermoelectric power, high thermal stability, high resistance to oxidation and corrosion, and their no toxicity [1.65-1.67]. Recently, Wang *et al.* [1.68] presented a detailed analysis on the thermoelectric properties of bulk 3C-SiC. At the nanoscale, it is expected a 100-times reduction of the thermal conductivity κ due to the increased role of phonons scattering which will lead to an even more increased of ZT, making 3C-SiC NWs an excellent candidate for thermoelectric applications.

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Chapter two: Modeling of electrical transport in 3C-SiC and Si NWFETs

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2.1 Introduction

As the dimensions are scaled down, the increasing importance of physical phenomena like quantum tunneling, reflections through metallic/semiconducting barriers and through channel potential barriers and as well as strong quantum confinement have drawn the interest of a full quantum description of carrier transport. Hence, device numerical simulations based on the self-consistent solution of the Schrödinger and Poisson equations are envisaged in order to correctly model these physical effects and give a valuable analysis and prediction of the device performance (section 2.2).

At this point we should mention that the present material growth technology is not mature enough to produce 3C-SiC without defects, micro-pipes and stacking faults. However, in this chapter we investigate the electrical transport properties of 3C-SiC nanowires, assuming perfect interface and completely absence of intrinsic defects. This theoretical work aims to predict the upper performance limit of 3C-SiC NWFETs, directly compared with corresponding Si devices. This comparison will reveal us if it does have sense to fabricate experimental SiC NWFETs. We use three different simulation techniques in order to describe the electrical transport properties of 3C-SiC and Si NWFETs operating at different electrical transport regimes. Depending on the channel length (L_G) a transistor operates in ballistic, quasi-ballistic and diffusive electrical transport regime. When $L_G<l$, where l is the mean free path in the semiconductor (the distance between two collisions-scattering events), then we do not expect any scattering along the channel (only scattering at the source/channel and drain/channel interfaces), in other words we have ballistic conduction. In this regime, by excluding the effect of scattering, we could note down the upper limit of device performance. Mobility theory estimates a mean free path value for Si and 3C-SiC around 10 nm. The experiments predict even shorter lengths, around 2-3 nm due to the presence of acoustic phonon scattering. In ballistic transport regime, we use a Poisson/Schrödinger self-consistent solution within the NEGF formalism (section 2.3). Our NWFETs are triple-gated and have channel length varying from 5 to 15 nm and a cross section side three and four nanometers.

On the other hand, ultimately scaled experimental NWFETs, mainly based on Si nanowires, operate in quasi ballistic regime. When the channel length is comparable with the mean free path the transport is not pure ballistic but due to the increased effect of both surface roughness and phonon scattering we have a deviation from the ideal transport conditions of ballistic carriers. For this transport regime, we use a similar simulation scheme as for the case of ballistic transport, and moreover we include a quantum treatment of scattering effects (both surface roughness and phonon

scattering) (section 2.4.3). For this kind of simulations, we implement GAA device geometry and we chose the length of the nanowire to be equal to 20 nm and the cross section side at 5 nm.

Our experimental 3C-SiC NWs (as they will be presented in chapter three) have length of few micrometers and diameter from 40 to 90 nm. These dimensions are far away from the ballistic and quasi-ballistic transport regime conditions (L_G>>l) allowing us to use a drift-diffusion model to describe this diffusive transport regime. We solve the continuity equation self-consistently with the Poisson equation and we calculate the current through the drift-diffusion model (which is an approximation of Boltzmann transport equation) (section 2.4.2). The simulated devices have a length from 200 to 750 nm and cross section side of 10 nm.

At this point, we should mention that our SiC calculations are based on an initial code dedicated to Si NWFETs. This code was appropriately modified in order to describe the behavior of SiC. Apart from the changes in the material parameter we included an extra scattering mechanism, the polar optical scattering, which is present only for SiC case (since Si is a non polar material). In the condition of low field regime, we observed that the effect of polar scattering is minor and therefore we did not present these calculated data.

2.2 Presentation of the simulation scheme

2.2.1 Self-consistent solution

Simulation of electrical devices normally involves a self-consistent simulation scheme between the electrostatic potential φ (obtained from Poisson equation) and the charge distribution (obtained from Schrödinger equation) inside the devices [2.1]. When a device is coupled to the contacts (electrodes), some charge is transferred into or out of the device (e.g., from the source/drain contacts), or some electric field lines penetrate into or inject out of the device (e.g., from the gate contact); both effects will result to a self-consistent potential energy $U_{SC}(r)$ (figure 2.1). This potential energy is called 'self-consistent' because changes in $U_{SC}(r)$ alter the charge density ρ(r) inside the device, which in turn modifies the $U_{SC}(r)$ until both the charge density and the potential energy attain consistent values.

For correctly modeling this process, we need to solve the two major equations in our simulations. The first one is the Poisson equation

$$\nabla\cdot(\varepsilon(r)\,\nabla U_{SC}(r))=-q\cdot\nabla\,(\varepsilon(r)\,\nabla\varphi_{SC}(r))=\rho(r)=q(N_D-n),\ (2.1)$$

which determines the self-consistent potential energy $U_{SC}(r)$ (φ is the electrostatic potential) for a given charge density $\rho(r)$ (figure 2.1). Here the dielectric coefficient $\varepsilon(r)$ is, in general, position-dependent due to the material transition from one simulated region to another (e.g., from the SiC body to SiO_2 layers). The second one is the transport equation that is solved to obtain the electron (carrier) density $\rho(r)$ inside the device for a given $U_{SC}(r)$

$$H\Psi(r)=\left(-\frac{\hbar^2}{2m^*}\nabla^2+U_{SC}\right)\Psi(r)=E\Psi(r),\ (2.2)$$

where H is the Hamiltonian (in parabolic effective mass approximation), $\Psi(r)$ is the electron wave function and m^* is the effective mass of the material. The electron density depends on the solution of the Schrödinger equation through the square modulus of the electron wave function. Thus, a coupling through the carrier density between eq. (2.1) and (2.2) is determined and an iterative self-consistent scheme has to be applied for the determination of the solution. Due to this coupling the total charge is non-linearly dependent on the potential itself and an explicit formulation of ρ as a function of φ is not possible. The system of $N_xN_yN_z$ equations (N_a is the number of nodes along the a axis where a=x, y and z) representing the discretization of the Poisson equation can be generally expressed in the form

$$F\,[\varphi,\ \rho\,(\varphi)]=0,\ (2.3)$$

where $\varphi=[\varphi_1,\ldots,\varphi_{NxNyNz}]$ and $\rho=[\rho_1,\ldots,\rho_{NxNyNz}]$ are the vectors representing the discretized potential and charge, respectively. In order to have better convergence properties for the self-consistent problem, a Newton-Raphson scheme is adopted, solving eq. (2.3) in terms of the correction vector $\delta\varphi$ of a trial solution φ^0

$$F\,[\varphi^0+\delta\varphi]=F\,[\varphi^0]+J\,\delta\varphi=0,\ (2.4)$$

where J represents the Jacobian matrix of the partial derivatives of F with respect to the components of φ. The definition of the Jacobian matrix is not a trivial part of the problem. A local dependence of the charge on the potential is assumed

$$\rho_i(\phi_i)=\rho_i(\phi_i^0)+\left.\frac{\partial\rho}{\partial\phi}\right|_i\delta\phi_i\text{, for i=1,...,}N_xN_yN_z,\quad(2.5)$$

Several solutions have been proposed to calculate the set of partial derivatives, $\frac{\partial \rho}{\partial \phi}$, ensuring different convergence properties. The adopted choice has been that of expressing the relation between electron density and potential exploiting the semi-classical relation:

$$n_i(\phi_i) = N_c F_{1/2}\left(q \frac{\phi_i - \phi_{n_i}}{k_B T} \right), \text{ (2.6) for i=1,...,} N_x N_y N_z$$

being, N_c the effective density of states, F_n the n-order Fermi-Dirac integral, and $\Phi_n = [\Phi_{n1},\ldots, \Phi_{n_{NxNyNz}}]$ an auxiliary variable, physically related at quasi-equilibrium conditions, to the electron quasi-Fermi level. Starting from an initial guess for the solution of the Poisson equation, the two equations (eq. 2.1 and 2.2) are iteratively solved till a convergence criterion is verified. The calculation of all physical quantities of interest will be performed on the last obtained solution.

In the semi-classical context, the Boltzmann Transport Equation (BTE) describes carrier transport

$$\frac{\partial f}{\partial t} + \vec{v} \cdot \nabla_r f - \frac{q\vec{E}}{\hbar} \nabla_k f = \hat{C} f \text{ , (2.7)}$$

where $\vec{E}$ is the electric field, $\vec{v}$ is the carrier velocity and $\hat{C}f$ describes the effects of scattering. In equilibrium, f (r, k, t) is simply the Fermi function, but in general, we need to solve eq. (2.7) to calculate f. Once f (r, k, t) is known, quantities of interest are readily found. The drift-diffusion model is an approximation of the BTE, in other words starting from the BTE and by computing the zeroth and the first moment we end up to the continuity and the drift-diffusion equations, respectively [2.2]. In BTE, it is assumed that the motion of a single particle (e.g., electron) obeys Newton's second law while the collective behaviour of the particle system (e.g., a collection of electrons) is described by statistical mechanics. This assumption works quite well when the device size is relatively large (i.e., much larger than the de Broglie wavelength of electrons). In the nanometer regime, however, the wave-like behaviour of electrons becomes substantially significant, so the semi classical transport equation may not be valid anymore. As a result, a full quantum mechanical transport model, such as the NEGF approach, is necessary to solve the Schrödinger equation.

2.2.2 Non Equilibrium Green's Function (NEGF) formalism: Ballistic and quasi-ballistic transport regime

The non-equilibrium Green's function formalism, which solves the Schrödinger equation under non-equilibrium conditions and can treats coupling to contacts and dissipative scattering process, provides a sound basis for quantum device simulations (figure 2.1) [2.3]. Although in the case of non-interacting transport (e. g. ballistic transport) the NEGF formalism is equivalent to the Landauer- Buttiker description of mesoscopic physics, the real power of NEGF is to provide a general approach for describing dissipative transport, combining quantum dynamics (G^R) and a statistical description of the interactions ($G^<$). In the following, a steady state analysis is considered. In this framework, the Fourier transform of all the operators of interest allows for the description in terms of space and energy coordinates instead of space and time [2.1]. A matrix notation with respect to the discrete spatial coordinates will be adopted.

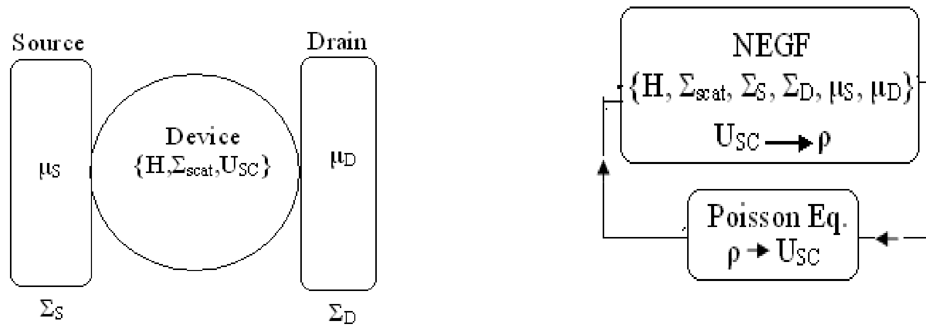

Figure 2.1 a) Schematic structure of a device coupled to the S/D contacts ($\mu_{S/D}$ is the chemical potential of the S/D contacts, U_{sc} is the electrostatic potential energy), b) self-consistent calculation scheme (ρ is the charge density).

In the calculations, the first step is to identify a suitable basis set (eigenfunctions' space) and then the Hamiltonian matrix (H) for an initial guess of the potential (usually $U_{SC}(r)=0$). The NW transistors are treated in a simplified tight-binding theory (we set one orbital per atom and only first-nearest-neighbours interactions are considered). The interaction energy, β, between two consecutive atoms is adjusted to obtain the carrier transport behaviour of a confined SiC (or Si) wire: the shape of the bottom of the conduction band provides the SiC (or Si) transverse effective mass ($m_t = 0.19m_o$ or $0.92\ m_o$ [2.4] for Si and $m_t= 0.25m_o$ or $0.68\ m_o$ for SiC [2.5] depending on the valley) by using the expression [2.1]:

$$\beta=\frac{\hbar^2}{2m_t a^2}, \quad (2.8)$$

where a=0.2 nm is the distance between two atoms. This simple (1s) tight-binding approach is quite equivalent to the effective mass approximation, but includes explicitly the atomic structure of the active region. It is clearly found that the effective mass approach, calibrated with bulk parameters, gives an incorrect transport description as the wire dimensions are scaled down to few nanometers [2.6, 2.7]. This implies a redefinition of the transverse and longitudinal mass values in order to extend the application of this method. In our simulation, we adjusted the nanowire cross section side to be over three nanometers, where the validity of the parabolic effective mass approach is still maintained. Other effects on the band structure cannot be captured by the effective-mass approximation. The second step is to compute the self-energy matrices, Σ_S, Σ_D and Σ_{scat} (figure 2.1), which describe how the channel couples to the source/drain contacts and to the scattering process (if Σ_{scat} is not zero). The source and drain contacts are characterized by a chemical potential μ which controls the carrier injection from the contacts into the channel.

After identifying the Hamiltonian matrix and the self-energy terms, the third step is to compute the retarded Green's function G^R (E) as derived from Dyson's equation [2.2]:

$$[EI - H_d - \Sigma^R] \cdot G^R = AG^R = I, \quad (2.9)$$

where E is the energy of carriers, H_d is the device Hamiltonian and Σ^R the retarded self energy term which includes the effect of both contacts ($\Sigma^R_{S/D}$) and scattering (Σ^R_{scat}) processes. Concerning the calculation of the contact self energy functions, in general, an analytical solution is not determined. A general expression can be derived from the truncation of the discrete Dyson's equations for a layered structure and reads out [2.1]:

$$\Sigma^R_{S/D} = H_{d,S/D} \; g^R_{S/D} \; H^{\dagger}_{d,S/D}, \quad (2.10)$$

where $H_{d,S}$ is the Hamiltonian describing the coupling between the semi-infinite source contact to the first (last for the drain contact) slice of the device, and $g^R_{S/D}$ is the retarded surface Green's function, describing the correlation between two points inside the contact when isolated from the device ($H_{d,S/D}$= 0). The surface Green's functions are expressed by a recursive relation and independently of the basis set used, they can be found numerically through an iterative algorithm [2.8]. In the mode space representation of the effective mass problem, analytical formulations are possible.

Partition of the device layers into two regions Z and Z' is shown in figure 2.2. Dyson's equation is a very useful method that relates the retarted Green's function of the full system Z+Z' in

terms of the subsystems Z, Z' and the coupling between Z and Z'. Dyson's equation provides us with a systematic framework to calculate the diagonal blocks of G^R (and $G^<$ which follows below) without full inversion of the A matrix of eq. (2.9) [2.2].

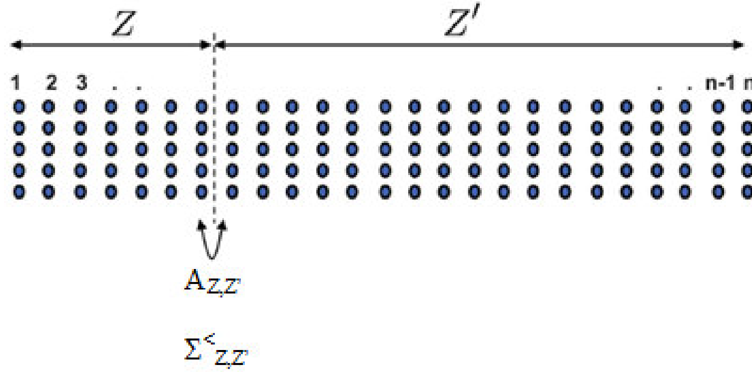

Figure 2.2 Scheme of device for application of Dyson's equation by splitting the device in two parts [2.2].

Following this method, eq. (2.9) can be written in the form:

$$\begin{pmatrix} A_{Z,Z} & A_{Z,Z'} \\ A_{Z',Z} & A_{Z',Z'} \end{pmatrix}\begin{pmatrix} G_{Z,Z} & G_{Z,Z'} \\ G_{Z',Z} & G_{Z',Z'} \end{pmatrix} = \begin{pmatrix} I & 0 \\ 0 & I \end{pmatrix} \quad (2.11)$$

The solution of eq. (2.9) is

$$G=G^0+G^0UG= G^0+GUG^0 \quad (2.12),$$

where

$$G = \begin{pmatrix} G_{Z,Z} & G_{Z,Z'} \\ G_{Z',Z} & G_{Z',Z'} \end{pmatrix},\ G^0 = \begin{pmatrix} G^0{}_{Z,Z} & 0 \\ 0 & G^0{}_{Z',Z'} \end{pmatrix} = \begin{pmatrix} A^{-1}{}_{Z,Z} & 0 \\ 0 & A^{-1}{}_{Z',Z'} \end{pmatrix},\quad U = \begin{pmatrix} 0 & -A_{Z,Z'} \\ -A_{Z',Z} & 0 \end{pmatrix} \quad (2.13)$$

Equation (2.12) is the Dyson's equation for the retarted Green's function. For clarity, we substituted in the Dyson's equation the symbol G^R (E) of the retard Green's function with simply G. Here, G represents the final perturbed Green's function and G^0 the unperturbed one. The G^R (E), which describes the carrier dynamics inside the device, is enough in order to describe the transport properties in ballistic regime. In the case of quasi-ballistic transport, things are more complicated. Apart from the retarded Green's function G^R, the lesser-than Green's function $G^<$ which correlates the electron wave functions should also be calculated [2.2, 2.3]. In steady-state conditions, the two kinetic equations describing the transport properties of the system are eq. (2.9) and:

$$G^< = G^R \Sigma^< G^A \quad (2.14),$$

where $\Sigma^<$ describes the in-scattering rate including the effect of scattering from both contacts and phonons as further explained below. In the case of quasi-ballistic transport eq. (2.9) and (2.14) are non-linearly coupled ($\Sigma^<$ is a function of $G^<$ and it is introduced in eq. (2.9) through Σ^R as we will present below) and self-consistently solved (extra self-consistent loop when phonons are included in the simulation in order to correctly estimate the charge density, $G^<$). Self-consistency is required for current conservation [the non-elastic optical phonon scattering modifies the charge distribution ($G^<$)]. Following a similar method like in the case of G^R, a Dyson's equation for the $G^<$ can be also calculated:

$$G^< = G^0 U G^< + G^0 \Sigma^< G^A = G^{<,0} + GUG^{<,0} + G^< U^\dagger G^{A,0} \quad (2.15),$$

where G^A is the advanced Green's Function and is the Hermitian conjugate of G^R , $G^{<,0} = G^0 \Sigma^< G^{A,0}$ and G^0 and U are the same as previously defined.

The spectral density of charge and current are determined as the expectation value of the respective field operator and they can be expressed, for a given energy E as:

$$n(r;E) = -\frac{i}{2\pi} G^<(r,r;E), \quad (2.16)$$

$$J(r;E) = \pm \frac{q\hbar^2}{2m^*} \lim_{r' \to r} (\nabla' - \nabla) G^<(r,r';E), \quad (2.17)$$

The presented description can be also repeated for hole transport. A similar expression as in the case of electrons is derived:

$$p(r;E) = \frac{i}{2\pi} G^>(r,r;E), \quad (2.18)$$

The lesser than and greater than Green's functions verifies the relation

$$i\,(G^> - G^<) = i\,(G^R - G^A) = \Lambda\,, \quad (2.19)$$

Λ being the density of spectral function, describing the total available electronics states, filled and not, at a given energy. The imposition of an equilibrium condition for the carrier distribution in the contacts is fulfilled through the definition of the lesser than and greater than self energy functions. They are expressed by the following relations [2.1]:

$$-i\Sigma_a^<(E) = \Gamma_a(E) f(E - \mu_a), \qquad -i\Sigma_a^>(E) = \Gamma_a(E)(1 - f(E - \mu_a)), \quad (2.20)$$

for a=S/D for source and drain contacts, and where $f(x)=1/(1+\exp(x/k_bT))$ is the Fermi-Dirac distribution, k_b is the Boltzmann constant, T the temperature and

$$\Gamma_a(E) = i[\Sigma_a^R(E) - \Sigma_a^A(E)] = i[\Sigma_a^>(E) - \Sigma_a^<(E)] \quad , (2.21)$$

The physical meaning of the Γ functions defined by eq. (2.21) allows for a better understanding of the self-energy description of scattering mechanisms. The quantity $1/\tau=-i\Gamma/\hbar$ represents a scattering probability describing the decay rate of a carrier from an external system to the device and vice-versa. In the case of an ideal ballistic conductor, the in- and out- scattering from the contacts remain the only interaction mechanism affecting the propagation of the carrier along the device. This physical description holds for both source and drain contacts and for the self energy functions representing the electron phonon interaction. In the case of ballistic conductor the division between statistical and dynamical description of the system is more evident. The charge density is given by

$$2\pi \cdot n(r;E) = \Lambda_S(r;E)f_S + \Lambda_D(r;E)f_D \quad , (2.22)$$

where $\Lambda_{S/D}=G^R\Gamma_{S/D}G^A$.The knowledge of the retarded Green's function is required in the calculation of Λ independently of the knowledge of its occupancy.

2.2.3 Mode-space approach

While still keeping all the relevant physics of the real space approach, the mode-space (MS) approach is introduced in order to reduce the computational costs for the solution of the transport problem. It consists in finding the real-space solution through its expansion on the basis set constituted by the wave function solution of the 2-D Schrödinger problem defined at each slice of the device along the transport direction. The real space Green's function can be expressed as

$$G^<(i,i',j,j',k,k';E) = \sum_{n,m} G^<_{nm}(i,i';E)\phi_n^i(y_j,z_k)\phi_m^{i'*}(y_{j'},z_{k'}) , \quad (2.23)$$

where $G^<_{nm}(i,i';E)$ is the mode space counter part of the real space Green's function, n and m sweep on all the transverse modes, and $\phi_n^i(y_j,z_k)$ is the n-th eigenfunction of the i-th slice of the device. The advantages of the MS approach come from the use of a truncated expansion, retaining a subset of $N_m \ll N_yN_z$ modes, thus limiting the dimensions of the transport problem to be solved. The

truncated basis set and the related matrix V_m is then used for the definition of the new mode space Hamiltonian

$$H_{ms} = V_m^{\dagger} H_d V_m \,, \quad (2.24)$$

that it will conserve the block three-diagonal structure but with each block matrix having leading dimension $N_m x N_m$. It can be easily found that each of the block matrices lying on the principal diagonal is diagonal, representing the on-site Hamiltonian for each of the N_m considered modes. The off diagonal matrices are full matrices in general, representing the coupling among the different transverse modes for every transition between two adjacent slices (correlation matrix). Using the previous assumptions, the discrete form of the device mode space Hamiltonian operator associated to mode space Green's function of the n-th mode on the i-th site is found to be:

$$-t_x \sum_m [c_i^{n,m} \delta_{i+1,j} + c_{i-1}^{n,m} \delta_{i-1,j}] + [2t_x + \varepsilon_i^n] \delta_{i,j} \,, \quad (2.25)$$

where $\delta_{i,j}$ is the Kronecker delta and ε_i^n is the n-th subband at i-th slice and

$$c_i^{n,m} = \int dydz \phi_i^n (y,z) \phi_{i+1}^{m\,*} (y,z) \,, \quad (2.26)$$

is the correlation between the n-th and the m-th mode for the i-th and (i+1)-th slices.

If the solution of the problem is carried out retaining all the information connected to the correlation matrix, the method is referred to as Coupled Mode Space (CMS) approach, due to the fact that the solution is correctly describing the coupling effect between the considered transverse modes arising from the potential variations. An additional approximation is possible, discarding the correlation terms and forcing the correlation matrix to a diagonal matrix describing the propagation slice by slice of a single mode with no interactions with the others. This approach is referred to as Uncoupled Mode Space (UMS), and has the computational advantage of diagonalizing the set of equations to be solved in N_m uncoupled problems. Concerning the contact self-energy an analytical formulation can be found in the MS representation for the chosen contact model [2.8, 2.9]. Due to the infinite repetition of the same confining potential a unique basis set is present in the contact and the correlation terms (eq. (2.26)) are null, making no difference between CMS and UMS description.

The transformation of the kinetic equations (2.9) and (2.14) is straightforward, keeping the same structure but with an obvious redefinitions of symbols moving from the real space representation to its mode space counterpart. In mode space representation, the electron density at

the discretized space site (i,j,k) and the current density flowing between (i+1,j,k) and (i,j,k) are calculated as [2.10]

$$n(x_i, y_j, z_k) = -\sigma_s \frac{i}{\Delta_X \Delta_y \Delta_z} \sum_{n,m,v} \int \frac{dE}{2\pi} G_v^{<,nm}(i,i;E) \cdot \phi_{v,n}^{i}(y_j, z_k) \phi_{v,m}^{i\,*}(y_j, z_k), \ (2.27)$$

$$J_x(x_i, y_j, z_k) = -\sigma_s \frac{q}{\hbar \Delta_y \Delta_z} \sum_{n,m,v} \int \frac{dE}{2\pi} 2\Re[H_d(i,i+1,j,j,k,k) \cdot G_v^{<,nm}(i+1,i;E) \cdot \phi_{n,v}^{i+1}(y_j, z_k) \phi_{m,v}^{i\,*}(y_j, z_k)]$$

$$, \ (2.28)$$

where σ_s accounts for the spin degeneracy, $\Delta_{x,y,z}$ is the discretization step in each direction, $H_d(i,i+1,j,j,k,k)$ is the discrete device Hamiltonian, q is the electron charge and $\Re$ indicates the real part of the resulting complex product. $G_v^{<m,m}$ is the m-th diagonal entry of the mode-space lesser-than Green's function and $\phi_{i,v'}^{n}(y,z)$ are the eigenfunctions at the transverse plane.The integration over the transverse plane of eq. (2.28) gives the current flowing along the transport direction at each slice of the device. The reduction to the UMS case is straightforward discarding all the off-diagonal terms of the mode-space Green's function. In the ballistic case, an analogous to Landauer-Büttiker formula is obtained [2.3]:

$$I = \frac{4e}{h} \int T(E)[f_s(E) - f_D(E)]dE, \ (2.29)$$

where $T(E)=\mathrm{Trace}(\Gamma_S G^R \Gamma_D G^A)$ is the S/D transmission coefficient. In the limit of a linear transport regime (low V_D) the linear approximation of $I=GV_{DS}$ holds, defining the conductance

$$G = \sigma_s \frac{q^2}{h} \int dE T(E)[-\frac{\partial f}{\partial E}(E - \mu_s)], \ (2.30)$$

An uncoupled mode-space approach has been adopted within the NEGF formalism to calculate the electron charge density in ballistic transport regime and when scattering mechanisms are included in the simulation, a coupled mode space approach is incorporated in order to capture the effect of interacting modes.

The computationally expensive part of the NEGF simulation is to calculate the retarded and lesser than Green's functions which requires the inversion of a matrix for each energy grid point and store them in memory for a range of energies. The straightforward way is to explicitly invert the matrix, whose size is the size of the basis set. In the ballistic limit, the problem is simplified because only a few columns of the Greens' function are needed. Still, reducing the size

of the Hamiltonian matrix (using mode space discretization) and developing computationally efficient approaches are of great importance for an atomistic simulation (for recursive algorithm's details see [2.2]). Conclusively, within the NEGF formalism, the self-consistent procedure for a quantum mechanical simulation of NWFETs consists of the following steps:

1 Given a particular NW FET structure, we first discretize all the operators.
2 To start the self-consistent loop, we need to give a guess value of $U_{SC}(r)$.
3 For a given $U_{SC}(r)$, we can write down the device Hamiltonian, H_d, and then calculate the contact self-energy matrices, Σ_S and Σ_D (and the self-energy matrix, Σ_{Scat} , if scattering is present that represents incoherent carrier transport in NW FETs).
4 With all the information obtained in the steps above, the retarded Green's function is evaluated and then the density matrix is computed.
5 Knowing the electron density inside the NW FET, a 3D Poisson equation is solved for the self-consistent potential, $U_{SC}(r)$.
6 Steps 3) – 5) are iterated until both the computed self-consistent potential and the electron density converge.
7 With the converged self-consistent potential and density matrix, the terminal currents of NW FETs are calculated.

In quasi-ballistic transport regime apart from the Poisson-Schrödinger loop, an extra inner self-consistent loop for charge density computation is required. The flow chart adapted from [2.2] can be seen in figure 2.3.

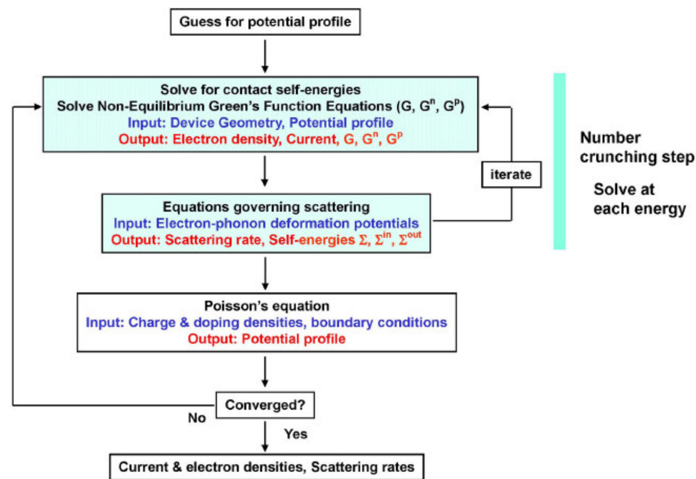

Figure 2.3 Flow chart of a typical device simulation operating in quasi-ballistic transport regime. [2.2]

2.2.4 Scattering processes

Introduction

Phonons are expected to have increased effect on transport properties of devices with one or two confined dimensions such as nanowire and nanotube transistors (the spatial confinement increases the phonon overlapping leading to increased scattering). Another property of 1D-materials is the high surface to volume atoms ratio which leads to an increased effect of the surface quality. In this framework, we focus on two main scattering mechanisms limiting the mobility of carriers in short nanowire devices: 1) Phonon (PH) scattering due to the various modes of lattice vibrations including acoustic (in the elastic approximation) and optical phonons, 2) Surface roughness (SR) scattering due to the spatial fluctuations at the interface between the channel and the oxide layer. A full quantum treatment of phonon and surface roughness scattering allows us to address a realistic performance prediction of ultimately scaled NWFETs. Scattering from acoustic phonons in the elastic approximation and dispersionless optical phonon scattering accounting for both f- and g-type processes for Si and only g-type for 3C-SiC (table 2.1) are considered. The Si and 3C-SiC phonon angular frequencies are slightly modified with respect to the nominal bulk values in order to have an optimization of the computational costs as reported in [2.11]. Polar optical phonons are not considered for 3C-SiC devices due to their minor effect at low drain voltages as shown in [2.12]. We describe the phonon scattering within a perturbative approach based on the definition of suited self-energy functions [2.13], whereas the effect of surface roughness is exactly treated with a geometrical description of spatial fluctuations [2.14, 2.15].

Table 2.1 Material parameters [2.16-2.18].

Transport properties	Si	3C-SiC
Crystal orientation	(100)	(100)
Bandgap energy (eV)	1.12	2.36
mass density (g/cm^3)	2.329	3.166
Lattice constant (Å)	5.43	4.3596
dielectric constant (ε_o)	11.7	9.72
Longitudinal acoustic velocity (x10^{5}cm/s)	9.04	9.5
Longitudinal optical phonon energy (eV)	0.063	0.098
Longitudinal effective mass (m_o)	0.916	0.68
Transverse effective mass (m_o)	0.19	0.25
Electron acoustic deformation potential (eV)	14.6	24.6
Intervalley g-type (x10^{8}eV/cm)	11	13
Intervalley f-type (x10^{8}eV/cm)	2	-
Valley degeneracy	2	1

Self energy matrix for phonon scattering

The electron-phonon interaction is described via the self-consistent Born approximation, and is included in the NEGF formalism by means of local self-energies. Here we assume bulk band structures for all phonons and neglect effects due to the confinement on the transverse plane [2.19]. The interaction between the electron and phonon system is represented by a proper self-energy (Σ) function, confined between a starting and a final state. The phonon system is considered unperturbed by the interactions with the electron gas. Within the self-consistent Born approximation, the lesser self-energy function for the electron phonon interaction can be written as $\Sigma^<(x_1, x_2) = G^<(x_1, x_2)\cdot D^<(x_1, x_2)$, where x_1 and x_2 represent the space-time points (r_1, t_1) and (r_2, t_2), and $D^<(x_1, x_2) = \langle\varphi(x_2)\varphi(x_1)\rangle$ is the lesser than free-phonon Green's functions. The analytical formulation of the lesser-than and greater-than Green's functions are calculated from the free phonons Hamiltonian in the interaction picture, which in the harmonic approximation for the lattice vibrations reads out:

$$\phi(r,t) = \frac{1}{\sqrt{V}}\sum_q M_q (a_q e^{-i\omega t} + a_{-q}^{\dagger} e^{i\omega t}) e^{iq\cdot r} \quad (2.31),$$

where V is the volume of the sample, q is the wave vector of the phonons, ω_q is the corresponding angular frequency, M_q is the electron-phonon matrix element and $a_q^{\dagger}$ and a_q are the phonon creation and annihilation operators. Inserting eq. (2.31) in the aforementioned expression for $\Sigma^<(x_1, x_2)$ and Fourier- transforming the time-dependent operators, the self-energy functions at a given energy E are given by

$$\Sigma^<_{ph}(r_1, r_2; E) = \int \frac{dq}{(2\pi)^3} e^{iq(r_1 - r_2)} \left|M_q\right|^2 (N_q + \frac{1}{2} \pm \frac{1}{2}) \cdot G^{<m,m}_{v'}(r_1, r_2; E \pm \hbar\omega_q) \quad (2.32),$$

where $N_q = \frac{1}{e^{(\hbar\omega_q / k_B T)} - 1}$ is the average phonon density at the energy $\hbar\omega_q$. In eq. (2.32) it is assumed that the phonon system remains in equilibrium even though the electron system is driven to the nonequilibrium condition. In matrix notation now, for the case of acoustic phonons, the lesser-than self energy for n-th mode at the i-th discrete space site along the transport direction reads:

$$\Sigma^{<n,n}_{v}(i,i;E) = \left|M_q\right|^2 \cdot \sum_m G^{<m,m}_{v}(i,i;E) \cdot I^{n,v}_{m,v}(i,i), \quad (2.33)$$

where v is the valley index. For the j-th optical mode the lesser-than self-energy reads out:

$$\Sigma^{<n,n}_{j,v}(i,i;E) = \left|M_q\right|^2 \cdot (N_j + \frac{1}{2} \pm \frac{1}{2}) \cdot \sum_{m,v'} g_j^{v,v'} \cdot G^{<m,m}_{v'}(i,i;E \pm \hbar\omega_j) \cdot I^{n,v}_{m,v}(i,i), \quad (2.34)$$

where $g_j^{v,v'}$ represents the final subband degeneracy according to the selection rules:

$$g_j^{v,v'} = \begin{cases} \delta_{vv'} & \text{for g-type} \\ 2(1-\delta_{vv'}) & \text{for f-type} \end{cases}, (2.35)$$

and $I_{m,v}^{n,v'}(i,i)$ represents the usual form factor:

$$I_{m,v}^{n,v'}(i,i) = \int dydz \cdot \left|\phi_{i,v'}^{n}(y,z)\right|^2 \cdot \left|\phi_{i,v}^{m}(y,z)\right|^2, (2.36)$$

The two different electron-phonon matrix elements are $\left|M_q\right|^2 = \frac{D_{AC}{}^2 \cdot k_B \cdot T}{\rho \cdot u_s^2}$ and $\left|M_q\right|^2 = \frac{\hbar \cdot D_{op}{}^2}{2 \cdot \rho \cdot \omega_o}$ for the acoustic and optical phonons case, respectively. D_{AC} and D_{op} represent the acoustic and optical deformation potentials, ρ the mass density, u_s the acoustic velocity and ω_j the optical phonon angular frequency. The phonon retarded self-energies are considered as purely imaginary for both optical and acoustic scatterings. The inclusion of the electron- optical phonon interaction as mentioned above, implies a coupling between the solution at energies at a distance $\Delta E=\hbar\omega_o$, where ω_o is the frequency associated to the specific optical mode. In order to include every optical-phonon coupling, a sufficiently refined energy grid is required, along with the simultaneous storage of the coupled Green's function during the iterative solution of the kinetic equations in the self-consistent Born approximation. For the chosen parameters, a fixed minimum energy step of ΔE_{min} =15.82 eV is identified, being the phonon energies of the considered modes all multiple integers of ΔE_{min}. By this way, it is possible to describe the coupled solution for energies ranging from a minimum value ΔE_{min} to a maximum value $\Delta E_{max}= \Delta E_{min}+N \times \Delta E_{min}$, with N integer, accounting for the complete set of relevant phonon modes. It is important to recall that a bulk model has been assumed for the phonon system. Effects of quantization on the phonon dispersion relation due to the confinement on the transverse plane are neglected. Suitably modified deformation potentials were used to mimic the phonons confinement.

The solution of the kinetic equations requires also the knowledge of the retarted self-energy, which can be calculated from the general relation [2.21]

$$\Sigma^R(E) = P\int \frac{d\varepsilon}{2\pi} \frac{\Gamma(\varepsilon)}{E-\varepsilon} - i\frac{\Gamma(E)}{2}, (2.37)$$

where P is the Cauchy principal integral value on the complex plane, and Γ, as defined in eq. (2.21) for every point inside the device. The real part of Σ^R, represented by the first term of the right side of eq. (2.37), is a non-hermitian energy contribution giving a shift of the particle energy levels [2.1]. The second term is associated to the scattering rate due to the electron-phonon interaction. The calculation of the principal value is computationally expensive and its contribution is in general

omitted. Only the information connected to the imaginary part of the retarted self-energy will be retained within the approximation

$$\Sigma^R(E) \approx -i\frac{\Gamma(E)}{2}, \quad (2.38)$$

It is obvious that through eq. (2.38) a dependence of Σ^R on $G^<$ is introduced. This implies, that in the presence of the electron-phonon interaction equations (2.9) and (2.14) are coupled through a non linear relation. As previously stated, this is not the case if ballistic transport is considered and the two equations separately describe the dynamics and the statistical properties of the system. When the phonon scattering is included, a self-consistent iterative solution of the two equations with the phonon self-energy functions required, in addition to the self-consistent loop with the Poisson equation (figure 2.3). It is important to note that in the self-consistent Born approximation the conservation of the current flux is guaranteed along the entire device, verifying the fulfillment of the continuity equation.

Generation of surface roughness

Surface roughness (SR) is often referred to be the most important cause of mobility degradation in conventional MOSFETs at high transverse fields. In Si NWs several competing mechanisms determine the impact of SR. As reported in [2.14], a reduction of the density of states, in association with the effect of the volume inversion, will lead to a beneficial reduction of SR impact on mobility. On the other side, as the dimensions of the wires is reduced, in connection to enhanced potential fluctuations, the SR scattering becomes stronger at low transverse fields, causing a drastic mobility decrease.

As we already mentioned in the introduction part, in order to account for the potential fluctuation effects we adopted the coupled-mode space (CMS) approach including up to 50 transverse modes. As far as the surface roughness is concerned, an abrupt randomly varying interface between Si and SiO_2 is considered. SR is not treated by using a perturbative approach but a quasi-continuous function $\Delta(r)$ representing the 2-D Si–SiO_2 interface displacement is assumed to be characterized by an exponential auto-covariance function [2.21]:

$$C(r) = \Delta^2_m e^{-\sqrt{2}r/L_m}, \quad (2.39)$$

where Δ_m is the root mean square (rms) of the fluctuations, and L_m is the correlation length. Each particular realization of SR was generated by starting from the power density spectrum obtained by

Fourier transforming the correlation function and adding a random odd phase to the square root of the power spectrum in order to create a statistics of local fluctuations in the momentum space. The obtained rough surfaces are properly discretized using a constant discretization step of 0.2 nm for each spatial direction. In the following a single device realization is considered for both Si and 3C-SiC nanowires, focusing on a comparison between the transport properties of the two materials and not on a statistical analysis of electrical performance.

2.2.5 Drift diffusion model: Diffusive transport regime

The current SiC technology is far away from the implementation of a ballistic nanowire FET with a channel length of few nm. Therefore, in order to compare theoretical with experimental results as reported by other groups (see chapter one), we simulated large devices with channel lengths up to 750 nm, using a drift diffusion model. In this case, the code is much more efficient from a computational point of view since we do not have to inverse huge Hamiltonian matrices (like in Poisson-NEGF scheme for computing the retarded Green function), we just solve the Poisson equation (equation 2.1) self consistently with the continuity equation and then by using the drift diffusion equations we compute the current [2.22] through larger structures (up to hundreds of nanometers) with much smaller computation time.

The continuity equation for electrons is defined by the equation:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \vec{J}_n + G_n - R_n \quad (2.40)$$

where n is the electron concentration, J_n is the electron current densitiy, G_n is the generation rate for electrons, R_n is the recombination rate for electrons, and q is the magnitude of the electron charge.

Equations (2.1) and (2.40) provide the general framework for device simulation in diffusive regime. However, further secondary equations are needed to specify particular physical models for J_n, G_n, R_n. The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation (the zeroth moment of BTE gives the continuity equation). These assumptions can result in a number of different transport models such as the drift-diffusion model, the energy balance model or the hydrodynamic model. The choice of the charge transport model will then have a major influence on the choice of generation and recombination models. The simplest model of charge transport that is

useful is the "drift-diffusion" model (eq. 2.41). This model has the attractive feature that it does not introduce any independent variables in addition to the potential (φ_n) and charge density.

$$\vec{J}_n = nq\mu_n E_x - q\mu_n n\nabla\phi n \quad (2.41)$$

2.2.6 Device geometry and parameters

Ballistic and diffusive transport

Devices operating in ballistic and diffusive transport regime were simulated with exactly the same geometry except the nanowire length. This parameter defines the transport regime, ballistic and diffusive one. When L_G<l the device operates in ballistic regime and when L_G>>l then in diffusive regime. In figure 2.4, a schematic representation of the devices is shown. For the ballistic case, we considered undoped nanowires/channels with the following characteristics: (a) tri-gated, (b) square cross sections (3 nm x 3 nm and 4 nm x 4nm), (c) 1 nm gate oxide width, (d) 9 nm channel length (we also varied the channel length from 5 to 15 nm to compute the subthreshold slope versus channel length) and (e) 4 nm source and drain electrode length. The usage of squared cross section instead of circular is more convenient by permitting us to simulate more easily different device geometries like double/triple-gated or GAA. In contrast, the polar coordinates are only dedicated to GAA devices. The crystal orientation is chosen to be along to (100) direction in all the simulations. This choice simplifies the calculation effort, for example in the case of (111) direction, the tensor of the effective masses is no more diagonal and this means for example that the hopping matrices between adjacent slices cannot be approximated with scalars but they have to be accounted as matrices. Although the experimental NWs based on VLS are mainly grown along (111), there are many reported studies on Si NWs grown along (100) using top-down techniques. All calculations are performed at room temperature (300 K). To describe diffusive transport we varied the nanowire length from 200 to 750 nm and keeping the cross section size at 10 nm. In table 2.2 are shown the physical parameters values of Si and SiC that we used in our code (table 2.2 contains parameters both for ballistic and diffusive transport regime. For example, the mobility values are used only in drift diffusion model and not in NEGF to describe ballistic transport). Only

the case of n-type devices is considered due to the known limitations of the effective mass model in describing transport in Silicon and SiC valence band.

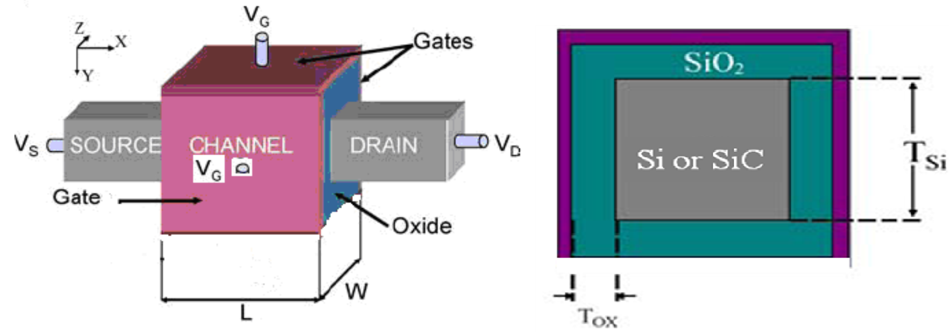

Fig 2.4: a) Schematic structure of the simulated nanowire transistor. (b) Cross-section view.

Table 2.2: Physical Parameters values of Si and 3C-SiC.

Parameters	Si	3C-SiC
Crystal orientation	(100)	(100)
Electron m_t^*/m_l^* (m_o)	0.19/0.92 [2.5]	0.25/0.68 [2.6]
Dielectric constant (ε_o)	11.7	9.72
Valley degeneracy	2	1
Electron affinity (eV)	4.05	3.83
Electron mobility (cm^2/Vs)	1200	1000
Conduction Band energy difference with SiO_2 (eV)	3.0	3.6
$E_g(T)$ (eV)	$E_g=1.1785-9.025\cdot10^{-5}\cdot T-3.05\cdot10^{-7}\cdot T^2$	$E_g=2.390-6.0\cdot10^{-3}\cdot T^2/(T+1200)$[13]

Quasi-ballistic transport

For quasi-ballistic transport, we used a completely different calculation code (see previous section). As far as the device geometry concerns, we have a similar structure as in the case of ballistic and diffusive transport regime. The only difference is related with the number of gates. This time, we consider Gate All Around (GAA) rectangular Si and 3C-SiC NW FETs with ideal ohmic contacts (similar structure as in figure 2.4 with an extra gate at the back side). We chose GAA geometry, due to the improved electrostatic control compared to the triple-gate geometry. The source and drain regions have a fixed length of 6 nm and donors doping concentration $N_d= 10^{20}cm^{-3}$. The channel is left intrinsic with a length of 20 nm and a cross section of 5x5 nm^2. A SiO_2 layer of 1 nm thickness is used as dielectric material. Bulk effective masses are considered for Si (m_t = $0.19m_o$, $m_l = 0.916m_o$) and 3C-SiC ($m_t = 0.25m_o$, $m_l = 0.68m_o$), while the electron effective mass in the oxide is fixed at 0.5 m_o, with m_o the free electron mass. Different gate work functions are

considered in order to have similar off-currents for the two materials. All calculations are performed at room temperature (300 K) and all simulation parameters are based on experimental material values, as listed in table 2.1 (page 70). The two most important differences arising from the material comparison are the transverse effective mass, which determines the transport properties in the ballistic regime, and the acoustic deformation potential, which largely affects the device performance in the quasi-ballistic transport regime. We notice that bulk parameters are used except for an increased acoustic deformation potential. A value of 14.6 eV is used for silicon instead of the bulk value, which is known to reproduce more accurately mobility curves in strongly confined Si devices [2.19, 2.23, and 2.24]. Accordingly, to this choice, a proportional increase of the acoustic deformation potential was assumed also for 3C-SiC with respect to the bulk value of 16 eV [2.16-2.18]. It is worth noticing that a direct comparison with experimental data from ultimately scaled NWFETs is quite difficult due to some uncertainty on experimental parameters such as exact device geometry dimensions, NW defects and doping distribution in the channel and it is out of the scope of our work.

2.3 Simulation results: Ballistic transport

2.3.1 Introduction

As we have already mentioned in the introduction of this chapter, we tried to completely study the electrical transport properties of 3C-SiC nanowire FET operating in ballistic, quasi-ballistic and diffusive transport regime. In this section, we used the powerful simulation scheme of the self-consistent Poisson-Schrödinger within NEGF formalism that we previously described, in order to investigate the electronic transport behaviour of triple gated 3C-SiC nanowire FETs in the ballistic transport regime. In parallel, we simulated Si nanowire devices with exactly the same geometry and under the same bias condition in order to compare these two semiconductors with respect to their electrical transport properties. The nanowire length was varied from 5 to 15 nm and the cross section side was 3 and 4 nm. Before presenting the transfer characteristics of the transistors, we focus on the subbands profile along the nanowire length and the transmission profile versus the carrier energy. This information helps us to understand the physics behind NWFET operation. At the end of this chapter, we perform a direct comparison between 3C-SiC and Si devices in terms of I_{ON}/I_{OFF} ratio and subthreshold slope values both extracted from the transfer characteristics (I_D-V_G).

2.3.2 Subbands profile

In this section we focus on the subbands profile and the transmission coefficient through the contacts. In figure 2.5 is shown the subband profile along the nanowire length both for Si and 3C-SiC at V_G=0 V (left) and at V_G=0.7V (right) and at V_D=0.4 V for the case of 4 nm cross section size of nanowire. The channel length was kept equal to 9 nm. We should mention that in our code for V_D=0.4 V the Fermi level of the source is fixed around 0.2 eV (and -0.2 eV for drain contact). At low V_G the potential barrier in the channel is quite high and prevents the carriers from passing through the nanowire. At these specific conditions, near the source contact the transmission coefficient is around zero and the reflection coefficient around one. The same situation stands for the area next to drain contact (at right of the channel barrier). We end up to equilibrium of carriers between the source and the drain contacts with negligible conduction through the nanowire. In addition, the total resistance of the device is a serial resistance, the sum of the two contact resistances and the channel resistance. At high gate voltages (~V_G=0.7 V), we have a lowering of the potential barrier, in other words a decrease of the channel resistance. The total resistance of the device is controlled from the contact resistance, which in the quantum ballistic limit is equal to $R_q=(\frac{2e^2}{h})^{-1}$ for each conductance mode (subband). When high voltage is applied, we have a transmission coefficient at the source region equal to one and a reflection coefficient equal to zero. In the contrary, at drain region the transmission coefficient is again equal to zero and the reflection coefficient equal to one and we end up to non equilibrium of carriers at V_G=0.7 V. In order to be compensated this effect, the subband energy decreases at the interface to the source contact (in order to increase the electron concentration) and the subband energy increases at the interface to the drain (in order to decrease the electron concentration). We note that the Fermi levels of source and drain are pinned: they represent the thermodynamic equilibrium of the huge electron reservoirs of the source and drain. In the active region, the potential is allowed to move by gate action since the electrons are far from the equilibrium. For that reason, for Si devices we have in total three subbands below the Fermi level at high V_G and only two at V_G=0 V (Figure 2.5). We have to mention that in any bias conditions our code computes the subbands until the first subband above the E_F.

The longitudinal effective mass of 3C-SiC is smaller than silicon ($0.68m_o$ for 3C-SiC and $0.92m_o$ for Si) and the transverse effective masses are almost equal ($0.25m_o$ for 3C-SiC and $0.19m_o$ for Si). Smaller longitude effective mass for 3C-SiC means that the energy separation of

subbands is higher ($\Delta E = \frac{\hbar^2 k^2}{2m^*}$) than Si. This has as a result that even at V_G=0.7 V the third subband is much higher than the second one, which it is still higher than Fermi level, and only the first two subbands are included in current computation. Another difference between the two materials is that the subbands are higher in 3C-SiC than in silicon and the energy separation between the first and the second subband is also larger. We can clearly see the differences between the two devices at two different V_G voltages (0 and 0.7 eV) in figure 2.5.

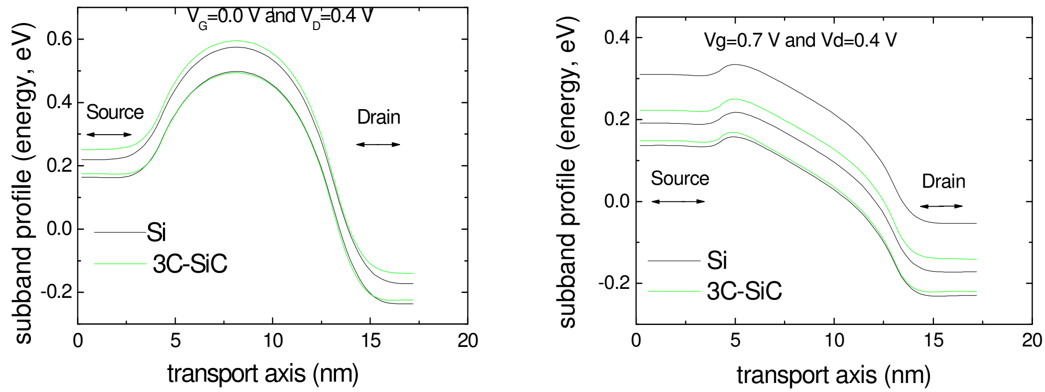

Figure 2.5: Comparison between Si and 3C-SiC subbands (cross section side of 4 nm).

In figure 2.6 is shown the comparison of Si and 3C-SiC when the cross section side of nanowire is decreased down to 3 nm. The results are similar with the case of 4 nm, apart from the fact that the quantum confinement is now more intensive. This has as a result that the energy levels (subbands) and the energy separation (between the various subbands) are higher than the case of 3 nm (for this reason even for silicon at V_G=0.7 V we have only two subbands).

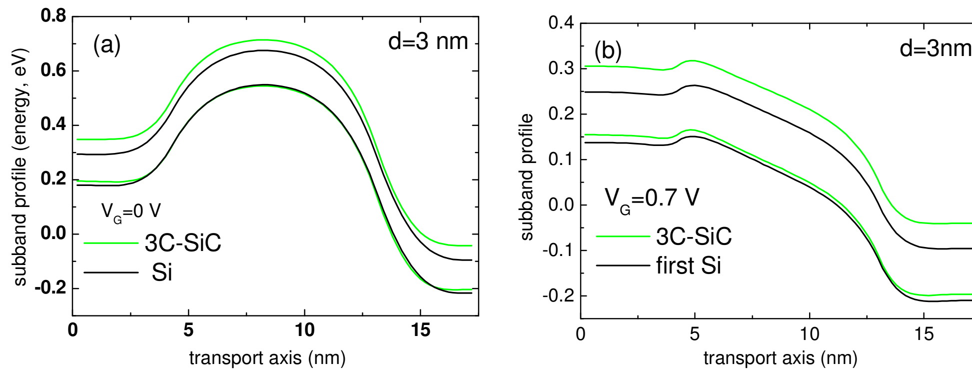

Figure 2.6: Comparison between Si-SiC subbands (3 nm).

2.3.3 Transmission coefficient

In figures 2.7 and 2.8 we present the transmission coefficient versus the carrier energy for Si and 3C-SiC devices, respectively. In figure 2.7 is shown the transmission for Si NWFET with for 4 nm cross section size of rectangular nanowire at low (a) and high (b) gate voltage.

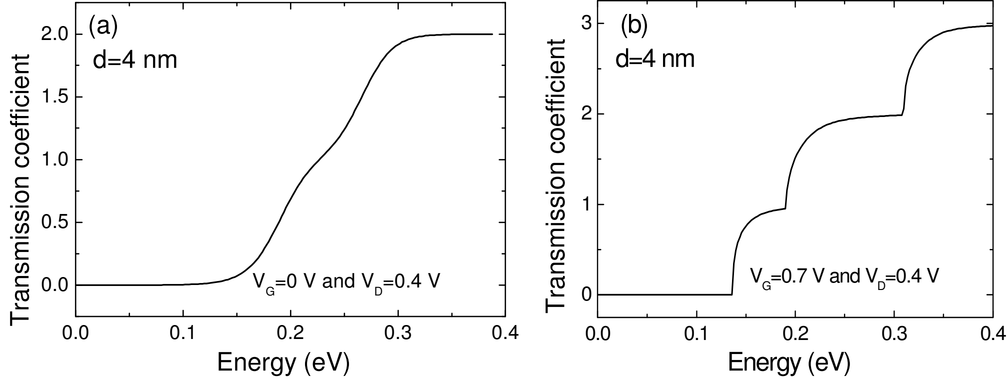

Figure 2.7: Transmission coefficient versus carrier energy (Si-d=4 nm).

The transmission profile is step-like due to the quantum nature of the transport. When the energy increases and reaches the first subband (or conduction mode), we have an increase of the transmission coefficient by a unit. When two subbands contribute to the conductivity, the transmission goes up to two. If three subbands are below the Fermi level, the case of Si nanowire FET with four nm diameter at high gate voltage, the transmission goes up to three (figure 2.7b). The total conductance is given by $G=\frac{M\cdot 4e^2}{h}$ (4 is for the spin and valley degeneracy), where M is the number of subbands which contribute to the conduction. At V_G=0.7 V the increase of the transmission is more abrupt than the case of V_G=0 V. This happens because at low gate voltages, we have a higher potential barrier in the channel and therefore it is more difficult for carriers to pass through the contacts. The energy difference and the position of the steps are the same as the position and the energy difference between two successive subbands (from direct comparison between figures 2.5 and 2.7). The transmission profile is analogous for the case nanowire with three nm cross section size. The same behaviour is noted down for 3C-SiC NWFETs with four nm cross section side of nanowire as shown in figure 2.8.

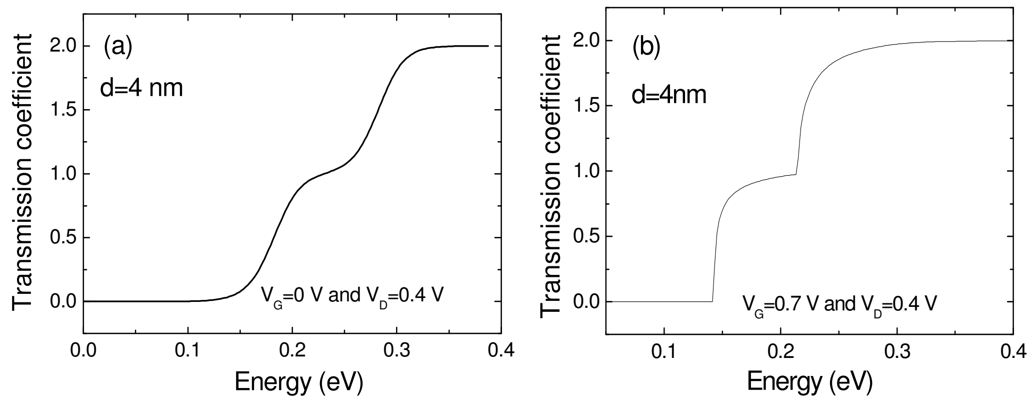

Figure 2.8: Transmission coefficient versus carrier energy (3C-SiC-d=4 nm).

2.3.4 Transfer characteristics

After examining the basic operation principles of NWFETs, we pass now to the electrical characteristics which will help us to extract some figures of merit for the device performance such us I_{ON}/I_{OFF} ratio and subthreshold slope. We chose two different nanowire (square) cross section sides for our FETs, 3 and 4 nm, in order to reveal the effect of quantum confinement on the transport properties while decreasing the dimensions. It is known [2.25] that there is a computational error when bulk effective masses (like our case) instead of the nanowire effective masses are incorporated (due to the quantum confinement we have a different effective mass in nanowires compared to the bulk material). This error is important only when the nanowire diameter is smaller than 3 nm. In figure 2.9 are shown the initial transfer characteristics for both silicon and 3C-SiC NW FETs with 3 and 4 nm nanowire cross section sizes.

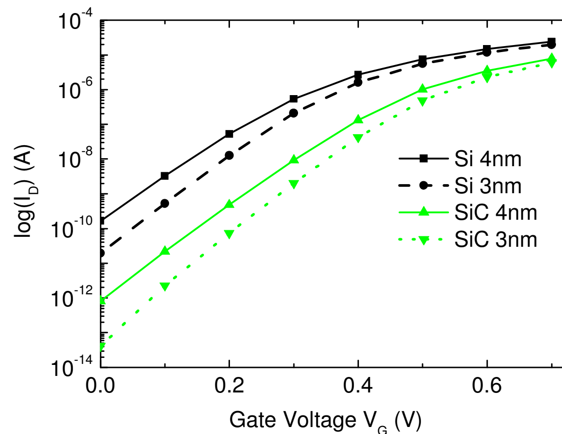

Figure 2.9: Initial Id-Vs for Si and SiC NW FETs (both for 3 and 4 nm).

As it is expected, the transfer characteristics for silicon and 3C-SiC do not coincide and an appropriate direct comparison is not possible. The first useful observation from this diagram is that the quantum confinement, which is stronger when we are passing to a cross section size of 4 to 3 nm, has as result a right shift of the curves. The quantum confinement leads to an enlargement of the energy gap and higher energy distance between the energy levels (ΔE), and more external power is needed in order to have current flow (when we compare FETs with cross section size of 4 and 3 nm at same V_G, FETs with 3 nm cross section size have smaller current). The second observation is that 3C-SiC devices are right shifted in comparison with the silicon devices, which is straightforward if we consider the smaller longitude effective mass (in the cross-section plane) of 3C-SiC.

In figure 2.10 are shown the components of the total current in one of our devices. The total current is the sum of the thermionic and the tunneling current. The thermionic current is higher than tunneling at higher voltages (when we have low potential barrier for the carriers, the tunneling is negligible) and the tunneling current is higher at low voltages (when we have high barrier along the channel, the tunneling current is higher than thermionic current).

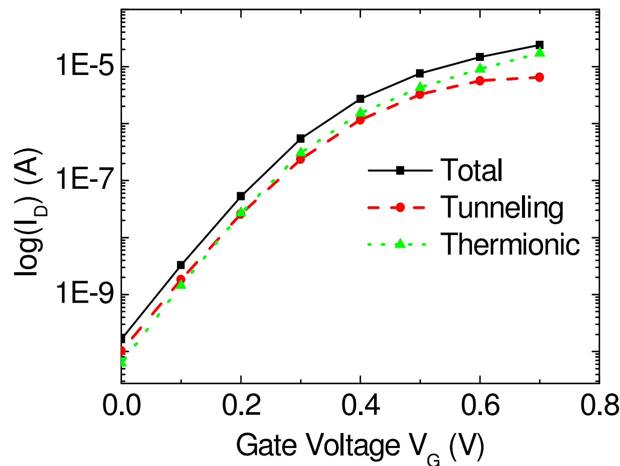

Figure 2.10: Total, tunneling and thermionic current.

A direct comparison could be possible if 3C-SiC and Si devices have comparable off currents (current at V_G=0 V and V_D=0.4 V). In order to achieve this, we adjusted the gate work-function of the 3C-SiC devices in order to have similar drain currents with silicon devices at V_G=0 V and V_D=0.4 V. The gate work-function for silicon devices was constant at w=4.6 eV, and for 3C-SiC devices at 4 and 3 nm we adjusted the work function at w=4.439 eV and w=4.441 eV, respectively. With these work-function values, we were able to adjust the same I_{OFF} between Si and

3C-SiC devices and derive a comparison. In the next few figures, we will present the comparison between Si and 3C-SiC transfer characteristics and the extraction of two important device figures of merit, the subthreshold slope (SS) and the I_{ON}/I_{OFF} ratio, which are figures of-merit of the device electrical performance.

In figure 2.11 are shown the I_D-V_G characteristics of Si and 3C-SiC NW FETs for both 4 and 3 nm cross-section size and constant at 9 nm channel length [2.26, 2.27]. In table 2.3 are shown the values of subthreshold slope and the I_{ON}/I_{OFF} ratio for both Si and 3C-SiC NW FETs. We extracted the subthreshold slope by taking two points at the subthreshold region of transfer characteristics and by computing the $SS=\Delta V/\log(I_2/I_1)$ which gives us the subthreshold slope in terms of mV/decade. In the case of 4 nm cross section size of NW, the 3C-SiC FET has a slightly lower subthreshold slope and as a consequence the Si device has the highest on-current, in particular I_{ON}/I_{OFF} (3C-SiC) ~83% I_{ON}/I_{OFF} (Si) (79% in case of 3 nm). The fact that Si has higher I_{ON} than 3C-SiC is due to the transverse effective mass, m_t (m_t for Si equals 0.19 m_o and for 3C-SiC is 0.25 m_o). The lighter is the transverse electron effective mass the higher the I_{ON} will be.

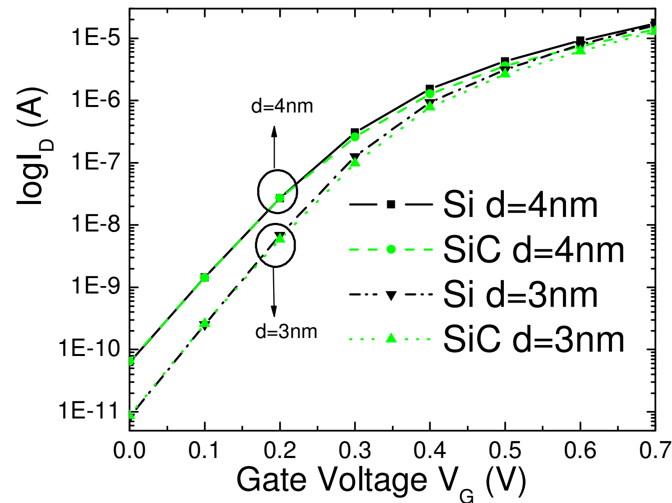

Figure 2.11: I_D-V_G characteristics of Si and 3C-SiC NW FETs for 4 and 3 nm cross-section side and 9 nm fixed channel length.

Table 2.3: Simulation results of 4 nm and 3nm NW cross section side FETs.

Device characteristics	3C-SiC NW FET		Si NW FET	
NW cross section side (nm)	4	3	4	3
Subthreshold slope (mV/dec)	76.5	69.4	77.1	69.8
I_{ON}/I_{OFF} (10^5)	1.21	7.9	1.44	10

We obtain similar results for NWs with 3 nm cross section size by comparing Si and 3C-SiC device performances. In addition, due to the quantum confinement (which is stronger than in 4 nm cross section size) we have a decrease in the subthreshold slope value and an increase in the I_{ON}/I_{OFF} both for Si and 3C-SiC devices which express FETs with improved performance when the NW cross section size decreases. Apart from the above results, we kept constant the NW cross-section size of NW FETs (both for Si and 3C-SiC at 4 nm) and we varied the channel length from 5 nm to 15 nm in order to compute the subthreshold slope in each case. As the channel length decreases, the subthreshold current (and equivalently the subthreshold slope) increases (figure 2.12a and b) [2.27]. For small channel length (5nm) the subthreshold slope of Si is higher (due to lower m_t) than the one of 3C-SiC device (figure 2.12b). Both effects are due to electron tunneling through the potential barrier of the channel, which is affected by the barrier width (i.e. channel length), and the effective transverse mass (m_t) of the barrier material. The increasing of the channel length progressively reduces the tunnelling and it then induces lower off-currents for the devices. For the devices with 15 nm channel length, the curves (both for Si and 3C-SiC) have a nearly ideal subthreshold slope of 64 mV/decade. In all cases, 3C-SiC NW devices have slightly lower I_{ON}/I_{OFF} in comparison with Si devices.

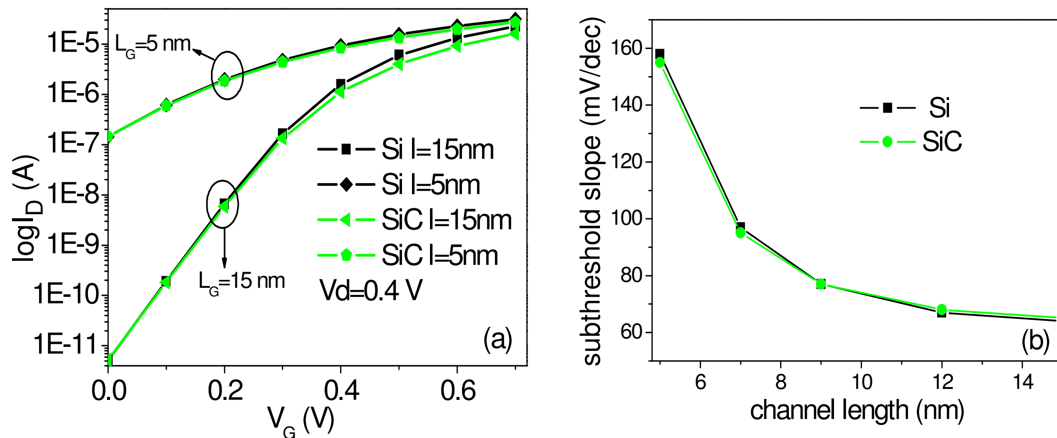

Figure 2.12: (a) I_D-V_G's for various channel lengths both for 3C-SiC and Si (4 nm NW cross section side), b) Subthreshold slope versus channel length.

2.4 Simulation results: Dissipative transport

2.4.1 Introduction

The electrical transport analysis in ballistic regime revealed the upper performance limit of 3C-SiC NWFETs. In the first part of this section, we simulate large devices with channel lengths up to 750 nm, using a drift diffusion model in order to compare our theoretical data with corresponding experimental results as reported by other groups (see chapter one). In this case, the code is faster from a computational point of view since we do not have to inverse huge Hamiltonian matrices (like in Poisson-NEGF scheme for computing the retarded Green's function), we just solve the Poisson equation (eq. 2.1) self consistently with the continuity equation (eq. 2.36) and by using the drift diffusion equation we compute the drain current [2.22] through larger structures (nanowires up to few hundreds of nanometres in length) with small computation time. When $L_G >> l$, for example when $L_G > 100$ nm, we can assume that the transport is purely diffusive and the drift diffusion model is capable to describe the electrical transport.

In the second part of this section, in an attempt to model ultimately scaled down NWFETs operating in quasi ballistic transport regime, where $L_G \sim l$, we include a quantum description of scattering effect in the NEGF formalism. The two scattering mechanisms included in our simulations are the phonon and surface roughness scattering. The basic figure of merit extracted from the electrical characteristics (following similar method with experimental characterization techniques) is the low field electron mobility. The effect of each scattering mechanism on mobility values is identified. Finally, using mobility values extracted both in ballistic and dissipative transport regime, we calculate the backscattering coefficient of our devices (again by following similar method with experimental characterization techniques).

2.4.2 Drift-diffusion results

For these calculations, we used the same device geometry with the case of ballistic transport regime apart from the channel length and cross section size. The difference in terms of

computation technique is that we used a Poisson-Continuity simulation approach instead of Poisson-Schrödinger within NEGF formalism. This allowed us to simulate the behaviour of larger devices with small computation time. For the drift- diffusion simulation, we chose to keep constant the NW cross section at 10 nm and we varied the NW length (channel length) from 200 up to 750 nm (figure 2.13). This last NW FET geometry of 750 nm and 10 nm NW length and cross section size respectively, is similar to the experimental one of Zhou et al [1.156]. In figure 2.13 is shown the comparison between 3C-SiC and Si NW device simulation and in table 2.4 the results are summarized and compared with the experimental device of Zhou et al.

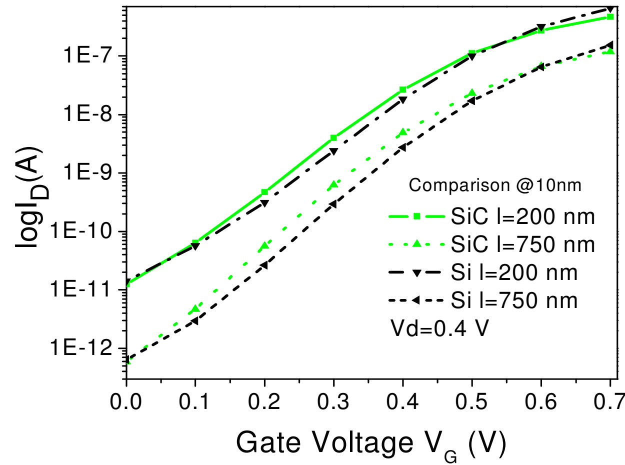

Figure 2.13: Transfer characteristics of Si and 3C-SiC NW FETs for various gate (from 200 up to 750 nm) lengths and 10 nm constant NW rectangular section side.

Table 2.4: Simulation results of 10 nm NW cross section side FETs. Comparison with experiment [1.156].

Device characteristics	3C-SiC NW FET			Si NW FET			Exper. SiC NW FET [6]
NW length (nm)	200	500	750	200	500	750	1500
Subthreshold slope (mV/dec)	113	98	93	135	113	105	-
I_{ON}/I_{OFF} ($\cdot 10^4$)	3.73	13.6	21	4.67	15.3	24	0.1

The results of drift diffusion model show a similar trend with that in the ballistic regime when comparing devices from the two semiconducting materials, except that the drift diffusion model predicts a smaller subthreshold slope for SiC (figure 2.14a). Si NW FETs still have a slightly higher on current (I_{ON}/I_{OFF} (SiC) ~87% I_{ON}/I_{OFF} (Si) in case of 750 nm nanowire length) (figure 2.14b). As we already mentioned, few experimental results on SiC nanowire FETs have been reported. The I_{ON}/I_{OFF} (SiC) of Zhou et al. [1.156] device is 10^3, much lower than the expected from

our simulation results. Indeed, by increasing the channel length from 200 to 750 nm the I_{ON}/I_{OFF} increases, from 3.73 to $20{\cdot}10^4$ instead of the measured 10^3, according to our results. Therefore, for a channel length of 1500 nm as in the case of Zhou et al, it is expected a value much higher than $20{\cdot}10^4$. An explanation for this discrepancy might be the existence of interface traps in the SiC/SiO_2 interface as the same authors for explaining their poor results have also reported it.

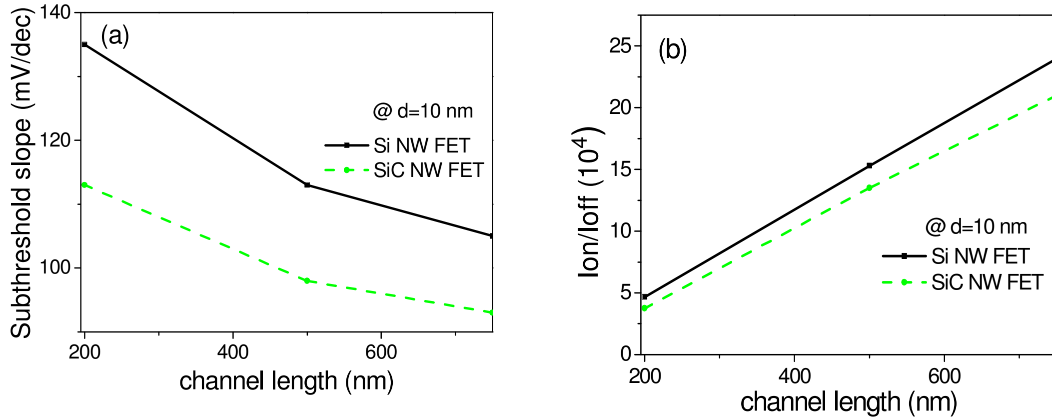

Figure 2.14: a) Subthreshold slope versus channel length at 10 nm NW cross section side, b) I_{ON}/I_{OFF} versus channel.

In conclusion, the drift diffusion model predicts a better performance for SiC devices. More specifically, SiC NW FETs have lower subthreshold slope than Si devices as the FET channel length increases (from 200 to 750 nm), and similarly with the case of ballistic regime, 3C-SiC devices have slightly smaller on- current.

2.4.3 Quasi-ballistic transport regime results

<u>Introduction</u>

In this section, we present simulation results based on a full quantum treatment of phonon and surface roughness scattering and this allows us to address a realistic performance prediction of ultimately scaled NWFETs. We previously described and presented details about the code, at this point we will present the simulation results. We initially calculate the low field

mobility both in ballistic and quasi-ballistic transport regime. By using a Mathiessen like formula, we investigate the effect of each scattering mechanism on mobility value. At the end, based on mobility values in ballistic and dissipative transport regime, we extract the backscattering coefficient of GAA Si and 3C-SiC NWFETs.

Subband fluctuations generated from surface roughness

When surface roughness is included in our simulation, the direct results of this effect is shown in the subbands profile along the nanowire length. In figure 2.15 is shown the corresponding subbands profile both for Si and 3C-SiC for two different rms values, 0.2 and 0.4 nm. We have more or less the same subbands profile for the two semiconductor nanowires.

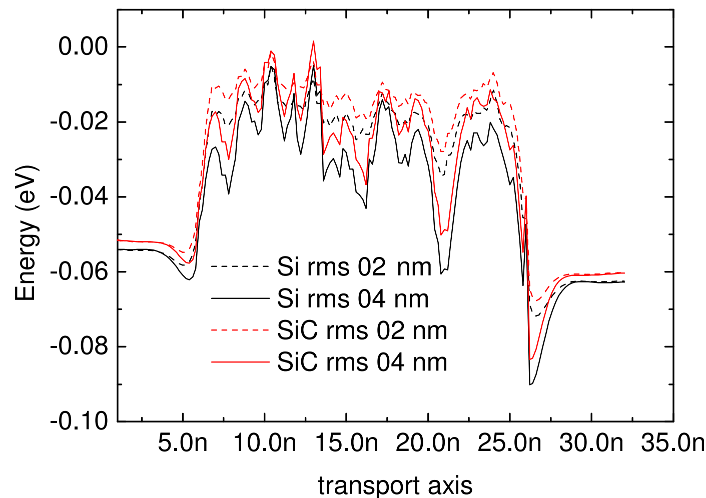

Figure 2.15 Subbands profile when SR is included.

Transfer characteristics and mobility extraction

In figure 2.16 we present the transfer characteristics at low V_{DS}=10 mV of Si and 3C-SiC devices in case of ballistic transport and when phonon and SR scattering are included [2.29]. SR parameters are Δ_m = 0.2 nm and L_m = 1 nm (eq. 2.35), which are comparable to the experimental

values of 3C-SiC thin films roughness [2.30]. In the ballistic case, consistently with previously presented results, Silicon NW FETs have higher on-current, due to the lower transverse effective mass (0.19 m_o for Si with respect to 0.25 m_o for 3C-SiC). When SR is present, transfer characteristics exhibit a relevant threshold voltage shift (~0.02 V) due to the potential fluctuations which lower the DOS in the channel [2.24] and change the maximum value for the potential energy barrier along the transport direction.

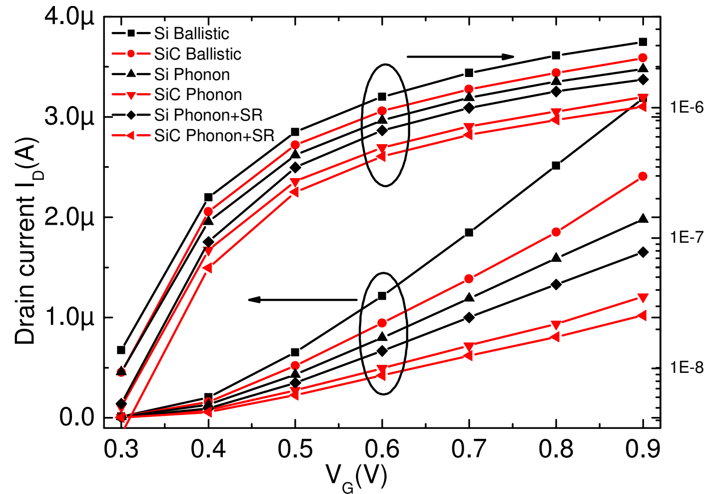

Figure 2.16 Transfer characteristics of GAA NW FETs at V_D=10 mV with and without scattering effects (logarithmic scale at left and linear at right).

A further analysis on the electrical performances of these devices could be obtained by analyzing the figure of-merit given by the low-field mobility. In a similar way as it is obtained from experimental characterization we compute the effective mobility of Si and 3C-SiC NWs as

$$\mu_{eff} = \frac{GL_{ch}}{qN_{1D}} , (2.42)$$

where G is the linear conductance, L_{ch} is the channel length, and N_{1D} the one-dimensional charge density along the channel. In order to avoid spurious effects due to charge penetration into the channel from doped regions we have estimated the charge density in a reduced region of the channel as proposed in [2.15]. Following the above method, we calculated the electron mobility for both Si and 3C-SiC devices as a function of the inversion charge density, as reported in figure 2.17a, where the ballistic case is shown, and in figure 2.17b, where the electron mobility in the presence of both SR and PH scattering is presented. Generally, the electron mobility decreases due to the effect of Fermi degeneracy in the ballistic case and due to the increasing effect of both PH and SR scattering at large gate overdrive in the presence of scattering in the channel. The ballistic

component of 3C-SiC devices is smaller than the one of Si devices, as shown in figure 2.17a, due to the different transport masses of the unprimed valleys (transverse effective mass), which would lead to a faster decrease of the effective mobility for smaller channel lengths for the 3C-SiC case. The evaluation of the effective mobility for such short channel devices directly accounts for the apparent or ballistic mobility component arising from scattering occurring at the contacts and directly depending on the channel length (curves labeled as BAL+PH+SR in figure 2.17b). Additionally, a purely scattering limited mobility can be recovered by subtracting the ballistic component as proposed by Shur [2.31] (curves labeled as PH+SR). The difference between $\mu_{BAL+SR+PH}$ and μ_{SR+PH} demonstrates the importance of ballistic carriers in such short devices. Moreover, the difference of the scattering limited mobility μ_{SR+PH} between the two materials shows a larger impact of PH and SR scattering in the 3C-SiC nanowires, mainly due to the larger value of the deformation potential for acoustic phonons (see table 2.1).

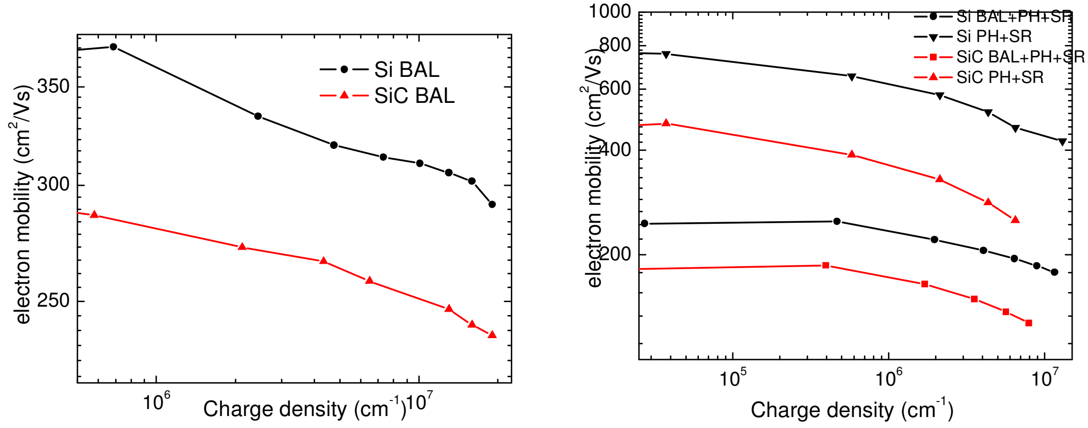

Figure 2.17 Electron mobility versus charge density in ballistic (a) and (b) quasi-ballistic transport regime (logarithmic scale both in x and y axis).

To further investigate the different role played by phonon and surface-roughness scattering in figures 2.18a and b we present the phonon (PH)-limited and SR-limited mobility versus charge density. These values are computed assuming that all scattering mechanisms are independent by means of the "Mathiessen" formula:

$$\mu_{PH} = \left[\frac{1}{\mu_{BAL+PH}} - \frac{1}{\mu_{BAL}} \right]^{-1}, \quad (2.43)$$

$$\mu_{SR} = \left[\frac{1}{\mu_{BAL+PH+SR}} - \frac{1}{\mu_{BAL+PH}} \right]^{-1}, \quad (2.44)$$

In figure 2.18a it is clearly shown the stronger impact of phonon scattering on transport properties for 3C-SiC with respect to Si devices. We notice a ratio between the PH-limited mobility of Si and 3C-SiC devices of approximately 2 at each gate voltage. Such a difference is directly related to the almost double value of acoustic phonon self-energy of 3C-SiC at the same charge density.

A different behaviour is found for SR-limited mobility as shown in figure 2.18b where curves for two different rms values, 0.2 and 0.4 nm, are presented. SR-limited mobility of Silicon NWs shows a steeper decrease as the charge density increases, revealing a slightly better electrostatic control compared to 3C-SiC ones which originates from the different material permittivity. The different dependence on N_{1D} of the SR-limited mobility for the two materials is hence due to the interplay of the two main mechanisms originating from surface roughness: the subband potential fluctuations along the transport direction and the mode-mixing arising from finite coupling between adjacent transverse eigenfunctions [2.14]. The first one determines the mobility value at low charge densities, whereas the second one becomes important at large charge densities when carriers are pushed towards the surface by the gate action. At low charge density, where subband fluctuations are effective, the SR-limited mobility of 3C-SiC devices is lower than Si ones due to the larger density of states (larger transverse effective mass), whereas at high charge density, where mode-mixing mechanism is effective, 3C-SiC presents smaller degradation due to the worst electrostatic control. This implies that the difference in SR-limited mobility of 3C-SiC and Si at low charge densities is partly reduced at larger gate voltages due to the smaller impact of mode-mixing in 3C-SiC. Moreover, when rms is very high, the case of rms=0.4 nm, potential fluctuations are the main degradation mechanism and SR-limited mobility is almost constant starting to further degrade only at very large charge densities.

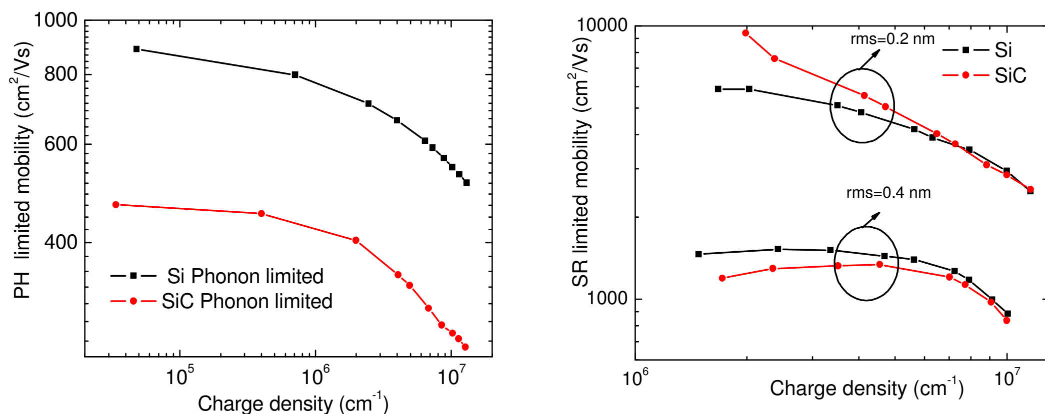

Figure 2.18 (a) PH-limited mobility versus charge density and (b) SR-limited mobility versus charge density (both x and y axis in logarithmic scale).

Backscattering coefficient

Recently, Pappas et al. [2.32] proposed a new method for the extraction of the backscattering coefficient (r) in nanoMOS devices based on mobility measurement. We should mention at this point that the r coefficient is obtained from macroscopic quantities (mobility) that are available from experiments and not, for example, from the transmission coefficient (which is hard to be experimentally extracted). Following [2.32], the backscattering coefficient is computed through the relation

$$r=1-(\mu_{BAL+PH+SR}/\mu_{BAL}), \quad (2.45)$$

where μ_{BAL} and $\mu_{BAL+PH+SR}$ are the ballistic and the effective mobility, respectively.

Following the above method, we first calculated the ballistic or apparent mobility (μ_{BAL}) when only the scattering effect due to the contacts was taken in account (top two curves in figure 2.19) both for 3C-SiC and Si devices. This is not a standard mobility since it scales linearly with the device length, but it is a useful quantity to evaluate ballistic carriers and then extract backscattering coefficients. The same procedure was followed when both phonon and surface roughness scattering mechanisms were included and an effective mobility $\mu_{BAL+PH+SR}$ was extracted (bottom two curves in figure 2.19). The ballistic component of 3C-SiC devices is smaller than the one of Si devices, as shown in figure 2.19, due to the different transport masses of the unprimed valleys (transverse effective mass), which would lead to a faster decrease of the effective mobility for smaller channel lengths for the 3C-SiC case. A direct comparison between $\mu_{BAL+SR+PH}$ and μ_{BAL} shows us how critical is the carrier scattering in such short devices.

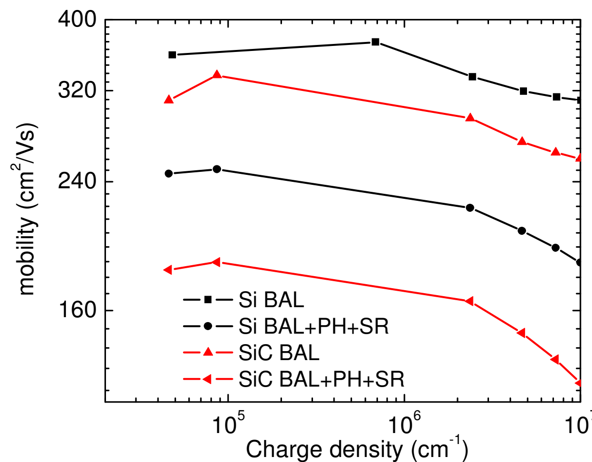

Figure 2.19 Ballistic and effective mobility versus charge density at V_{DS}=10 mV (curves of ballistic mobility are defined as BAL, and curves of effective mobility are defined as BAL+PH+SR).

In figure 2.20, the backscattering coefficient is calculated according to eq. (2.45) and plotted versus the charge density along the channel [2.33]. We find that backscattering coefficient increases with the inversion charge due to the effect of carrier degeneracy and the effect of both PH and SR scattering, which become important at large gate overdrive. From the values in figure 2.20, we extracted for the case of rms=0.2 nm r_{Si} =0.31 and r_{SiC}=0.43 at low charge density and r_{Si} =0.40 and r_{SiC}=0.52 at high charge density, which quantifies the larger amount of scattered electrons for 3C-SiC devices (25% higher than the Si case). This is a direct result of the larger acoustic deformation potential of the 3C-SiC NWs, resulting in an enhanced phonon scattering with respect to the Si case.

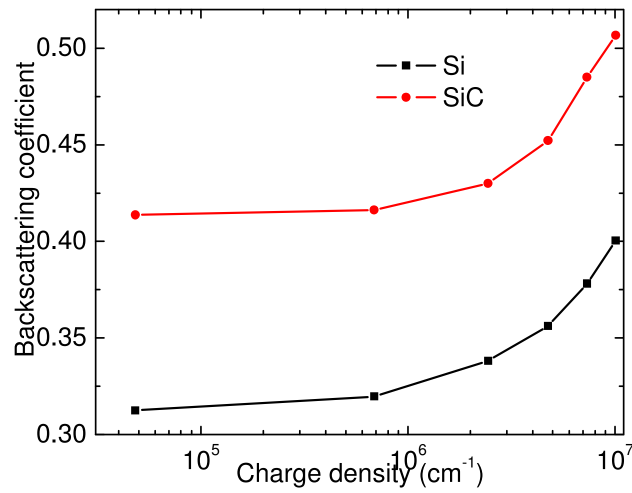

Figure 2.20 Backscattering coefficient versus charge density at V_{DS}=10 mV

2.5 Conclusions

The aim of this theoretical work was before proceeding to the fabrication of SiCNWFETs to estimate the upper performance limit of SiC devices. This is more evident through a direct comparison with corresponding Si NWFETs. This comparison revealed that SiC devices are quite competitive to Si ones. Our results revealed that Si and 3C-SiC NW FETs have comparable electrical behaviour in ballistic regime. They have the same subthreshold slope (69.4 mV/dec for SiC and 69.8 mV/dec for Si devices for 3 nm NW cross section size) and almost comparable on current [I_{ON}/I_{OFF} (SiC) ~83 % I_{ON}/I_{OFF} (Si) for 4 nm NW cross-section size]. In order to extract a critical figure of merit of the device performance, the low field carrier mobility, we also simulated devices operating in non-coherent transport regime using a similar self-consistent Poisson-NEGF

calculation scheme. The apparent mobility of 3C-SiC devices operating in ballistic regime is about 90 % of Si ones which is a direct result of the transverse effective mass difference of the two semiconductors. The picture is quite similar when inelastic phonon scattering processes are included in the simulation since their relative comparison reveals an extra degradation for 3C-SiC mobility as a consequence of a larger acoustic deformation potential. A smaller difference for SR-limited mobility was found for equivalent parameters of spatial fluctuations. Moreover, for 3C-SiC slower mobility degradation was observed for increasing gate voltage, revealing that the performance gap between Si and 3C-SiC devices is reduced in the operation regime. Analysis of backscattering coefficient versus carrier density is derived based on mobility extraction. The decrease of the effective mobility as a function of electron density originates from the carrier degeneracy and both phonon and surface-roughness scattering, resulting in an increase of the backscattering coefficient at large gate overdrive. A larger amount of backscattered electrons was found for 3C-SiC devices compared to Si ones, mainly due to the different acoustic deformation potential of the two materials.

By taking in account the simulation results we could conclude that SiC NWs, despite the slightly worst electrical performance compared to Si ones, could be used in targeted applications such as high temperature FETs and sensors. In chapter three, we present our effort for the experimental SiC NWFET realization.

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Chapter three: SiC nanowire growth through conversion

3.1 Introduction…………………………………………………………………....p. 98

3.2 Growth of 3C-SiC nanowires……………………………………………….....p. 98

3.2.1 CNT and Si NW conversion to 3C-SiC NW……………………………p. 98

3.2.2 Si NW conversion to 3C-SiC……………...……………………………p. 102

3.1 Introduction

In this chapter, we show results from our experimental efforts dedicated to prepare SiC NWs using conversion techniques. The first approach that we followed was to convert commercial CNTs by exposing them to Si vapour to SiC. In the second method, we prepared mono-crystalline, defect-free, vertical Si nanowires and we tried to convert them to 3C-SiC by exposing them in carbon vapor (methane). Novel experiments were organized and accomplished and the results of these first experiments are presented. Devices based on these nanowires are not prepared yet due to their worst quality compared to the available SiC NWs which we received from our collaborators (Prof. S. K. Lee and Prof. D. Cornu). An optimization of the growth technique is needed before fabricating devices based on these NWs.

3.2 Growth of 3C-SiC nanowires

We already presented in chapter one the various nanowire growth techniques, including among others the relevant literature on Si and 3C-SiC nanowires. In this section, we focus on conversion experiments which we performed during this thesis. We firstly attempted to convert CNTs to SiC NWs. These conversion experiments were accomplished in a conventional furnace. Unfortunately, no evidence for SiC nanowire formation was observed. Possible origins for these results are proposed. The second growth technique was to prepare Si NWs and convert them to SiC NWs in a CVD system. This method allowed us to prepare SiC nanowires (confirmed by EDX and Raman spectroscopy). We will present the different experimental setups/conditions and selected characterization results from each growth method.

3.2.1 CNT and Si NW conversion to 3C-SiC NW

CNTs conversion to SiC NWs in conventional furnace

Following the first route, we used commercial Multi Wall (MW) CNTs (Aldrich, O. D. x length: 6-20 nm x 1-5 microns). These CNTs were diluted in methanol solution and were kept without any movement for one week. We used two different types of samples, samples with sparse and dense CNT films. When we are referring to sparse film, we mean that we picked up one or two droplets from the top of CNT solution and we drop them over the silicon substrate (figure 3.1a). There is still a small possibility to find some small bundles of CNTs over the sample. On the other hand, with the expression 'dense' we mean that we selected droplets from the bottom of the solution where the heavy bundles of CNT were "dropped" after one week of quiescence (figure 3.1b). By naked eye, the difference between these two types of samples is evident (the dense film is black due to the CNT coverage). Many experiments, with CNTs on top of silicon wafers were initially performed. At the centre of the tube, we placed the Si source (SiO) at 1250 ^{o}C for 40 minutes and the samples were placed right of SiO in a region between 1100 and 900 ^{o}C (figure 3.2). We had a continuous gas flow (H_2/ Argon with 5% (figure 3.3) and 20% in hydrogen (figure 3.4)) of 50 sccm.

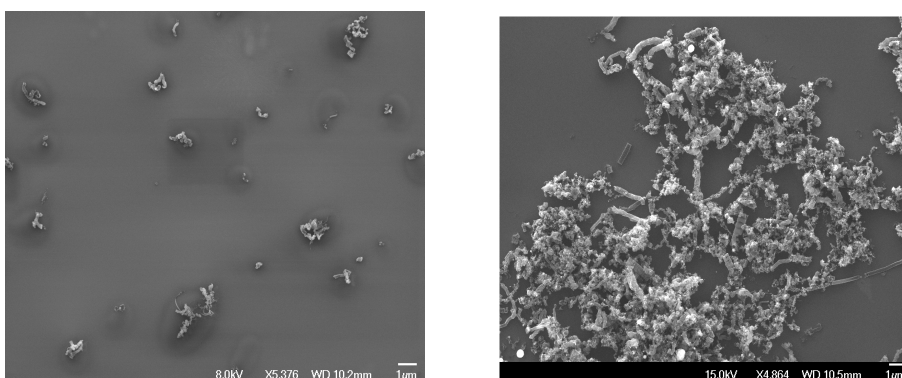
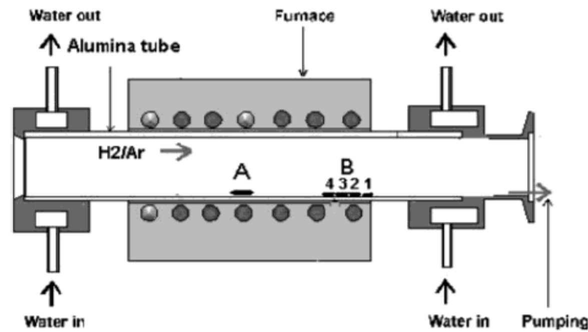


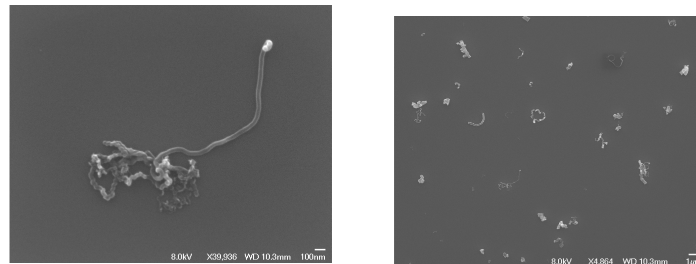
Figure 3.1: Representative SEM images from: (left) sparse and (right) dense CNTs film.

A conclusion of these first experiments, converting CNTs to SiC NWs, was firstly that we should use Ar/ 5% H_2 not Ar/ 20% H_2. When we have more H_2 present, we end up with high Si substrate etching especially at high temperature. We can see the samples before putting them in the furnace (figure 3.3a), and we can distinguish the effect of high percentage of hydrogen (high surface roughness when we use 20% H_2) (figure 3.3b-e). In all SEM images, we observe a black shadow around nanotubes, in contrast both with the prior-to-heating-substrate surface and the samples of experiment with 5% of hydrogen (figure 3.4). Moreover, at high temperature cracks and surface damage on the substrate are observed. Another critical parameter was the type of CNT film, in other words if the sample had sparse or dense film of CNTs. If the film was dense, we had presence of metal catalysts (Fe, Ni) (figure 3.4). The reason was that we picked up the CNTs from the bottom of the solution, where the heavy metal catalysts are deposited.

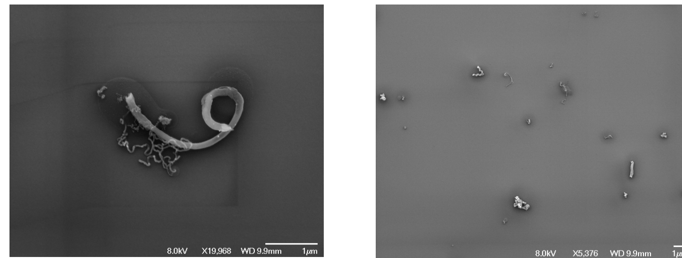
Unfortunately, XRD characterization did not reveal any SiC formation. From the SEM images below, it seems that the presence of metal catalysts affects the conversion. EDS analysis showed the presence of metal catalysts (Ni,Fe) all over the sample with dense CNT film (figure 3.5). We observed broken CNTs only in the samples where we had dense film (see figure 3.4a). In the samples with sparse film, which means without catalysts, we did not observe any broken or damaged CNT (3.4b). It is quite probably that the metal catalysts speed up the reaction between Si and CNTs and this led to overreaction (broken CNTs) with result no formation of SiC.



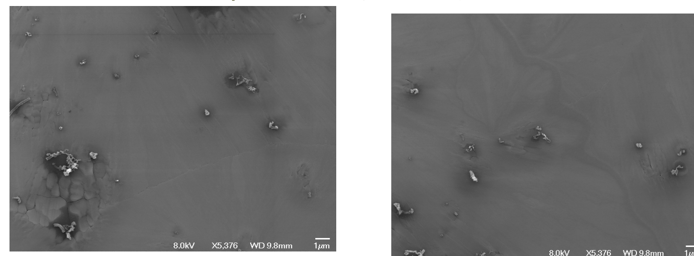
Fgure 3.2: Experimental setup.



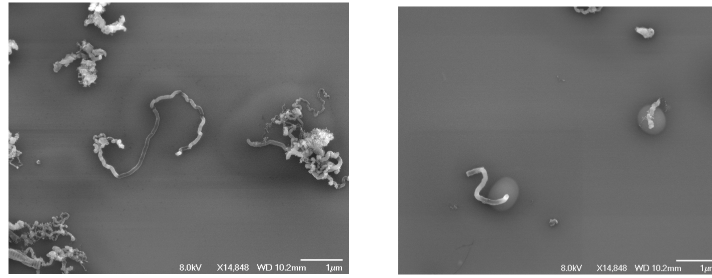
a) Initial samples



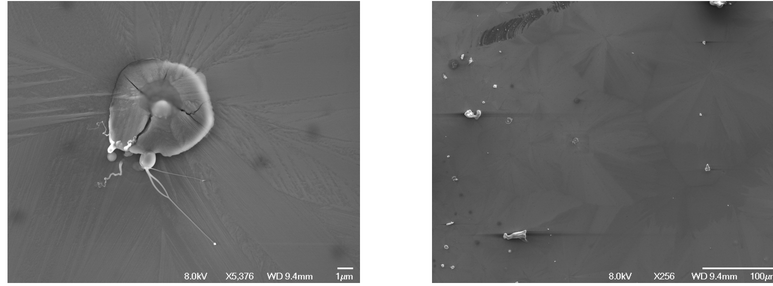
b) After conversion (880-800 ^oC)



c) After conversion (957-909 ^oC)

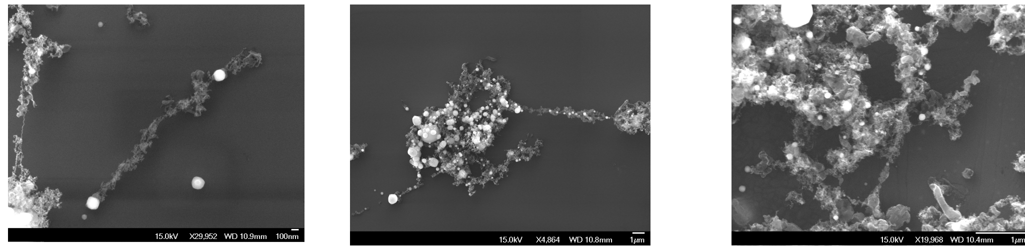


d) After conversion-Sample B (1100-971 C)

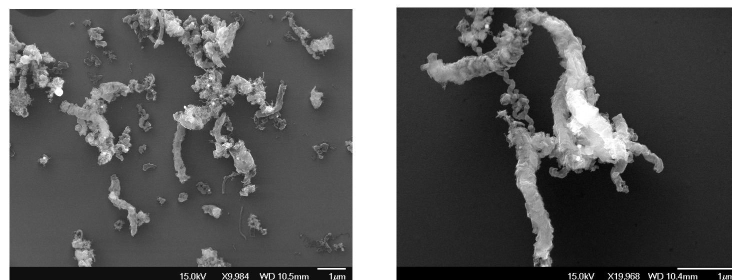


e) After conversion-Sample A (1250 C)

Figure 3.3: Initial (a) and after heating samples (b-e), experiment using 20% H_2.



a) After conversion-dense sample, lower temperature from left to right



b) After conversion-sparse sample, lower temperature from left to right

Figure 3.4: SEM images of samples after experiment with 5% H_2; a) dense CNT film, b) sparse CNT film.

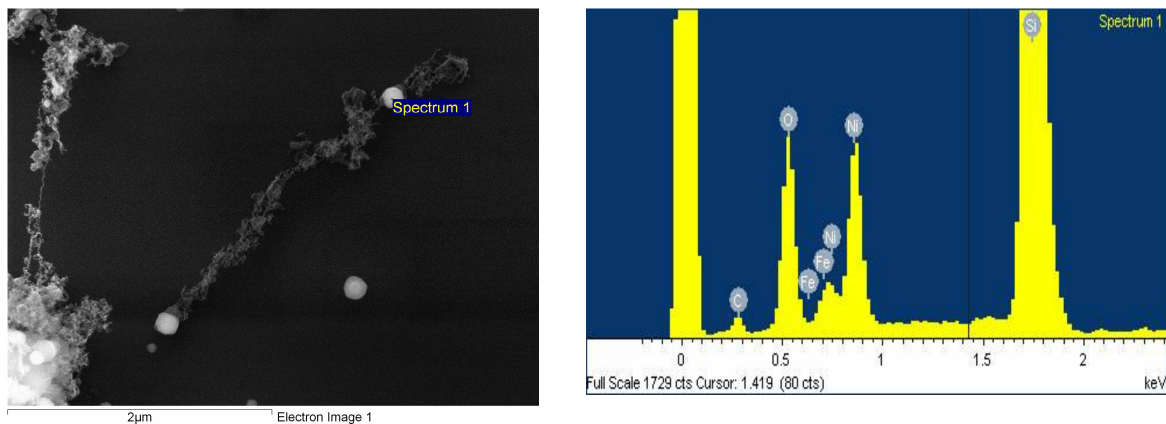


Figure 3.5: a) SEM images of samples after experiment -damaged CNT; b) EDS analysis confirm the catalyst presence (Fe, Ni).

3.2.2 Si nanowires growth and conversion to SiC in CVD

We initial grew (in a CVD chamber) vertically orientated, monocrystalline and undoped Si nanowires, following the VLS mechanism using as Si precursor silane (SiH_4) and gold as catalyst. Structural quality of Si NWs is excellent: single crystal with <111> growth direction (very few stacking faults). The size (diameter and length) is well controlled: from 5 to 100 nm in diameter for instance. We followed a well-established process for Si nanowire growth and details on which can be found in [3.1, 3.2]. An initial SEM image of Si nanowires is shown in figure 3.6. No presence of Au nanoparticles was found after appropriate chemical treatment in order to remove the catalyst seeds. The target was to convert these Si nanowires to 3C-SiC by exposing the material to carbon source, namely methane. A conventional CVD system was used. The temperature was raised up to 1200 ^{o}C and was maintained there for 15-120 minutes. The best results were received when the temperature was 1100 ^{o}C and the dwell time was 60 minutes. A diagram of the process steps is depicted in figure 3.7. Under these experimental conditions, Raman and energy-dispersive spectroscopy (EDS) characterization revealed both carbon and Si presence in the nanowire region (figure 3.8 and 3.9).

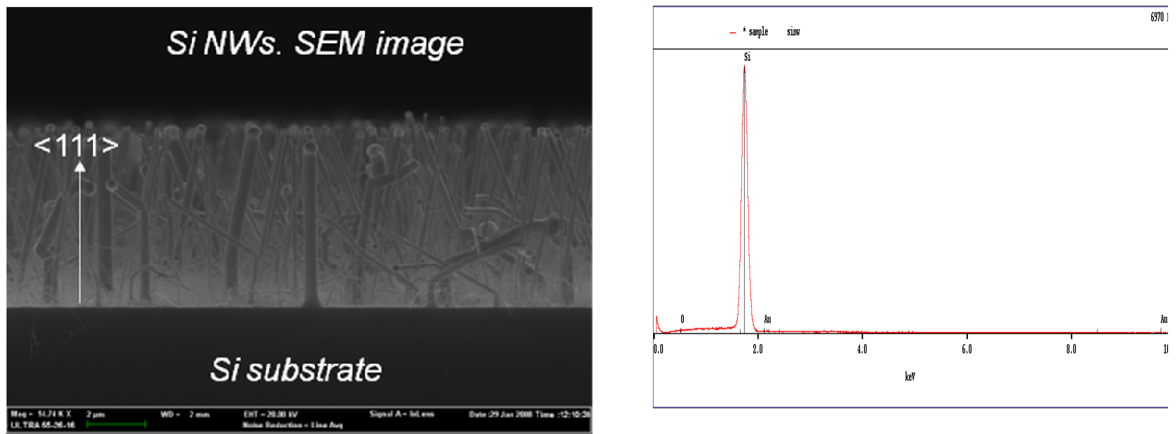


Figure 3.6 (left) SEM image of Si nanowires grown in CVD based on VLS method, (right) EDS spectrum confirms the absence of gold after chemical treatment (placing the sample in HF and HCL for few minutes).

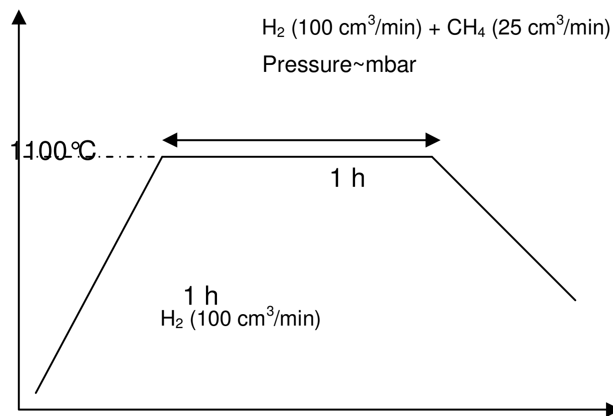


Figure 3.7 Diagram of process steps of Si NWs conversion to 3C-SiC NWs (X axis time, Y axis temperature).

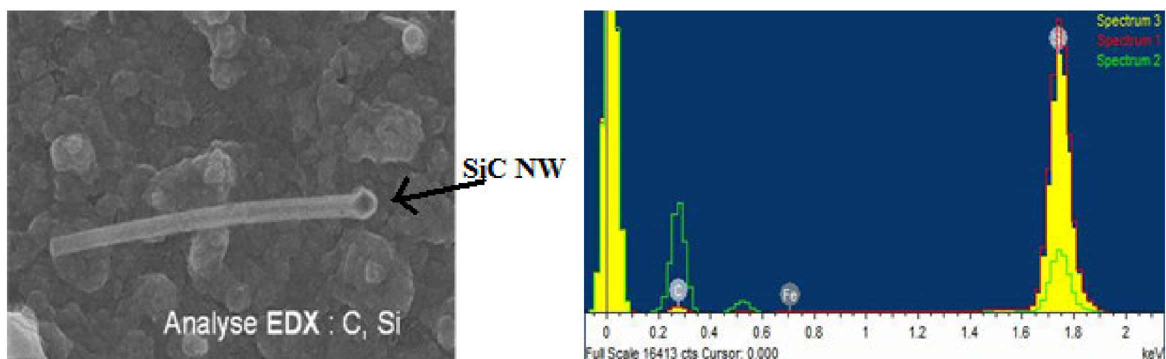


Figure 3.8 SEM and EDS spectrum of 3C-SiC NWs.

SEM and EDS characterization revealed in some places strong carburazation of the Si substrate surface covering in same cases the nanowires. This might be due to the long duration of the experiment (1 hour). Moreover, the surface roughness of the final product, 3C-SiC nanowires, is higher than the initial Si nanowires (figure 3.8). Raman spectroscopy confirmed the above findings (figure 3.9) and in addition revealed peaks from a-SiC. We can also observe a Si peak due to the substrate, and moreover carbon peaks due to carbon. For FET applications, these nanowires could be removed from the substrate by ultrasonication and to be placed in a solvent solution (to avoid oxidation).

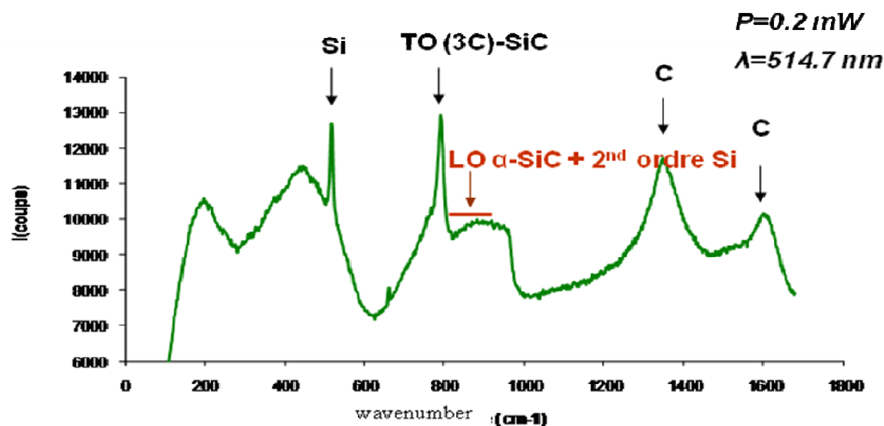


Figure 3.9 Raman spectroscopy of 3C-SiC NWs.

The first set of experiments revealed that the conversion is possible but an optimization of the process is needed in order to produce 3C-SiC nanowire, free from stacking faults and high surface roughness, suitable for FET applications. This surface roughness is expected to severely affect the electrical transport properties. The worst quality of these SiC NWs in comparison to that grown by the Koreans and Prof. Cornu group did not allow us to prepare devices based on them yet.

3.3 References

[3.1] T. Baron, M. Gordon, F. Dhalluin, C. Ternon, P. Ferret, P. Gentile, *Appl. Phys. Lett.* 89 (2006) 233111

[3.2] F. Dhalluin, P. J. Desré, M. I. den Hertog, J. L. Rouvière, P. Ferret, P. Gentile and T. Baron, *J. of Appl. Phys.* **102**, 094906 (2007)

Chapter four: Experimental 3C-SiC and Si nanowire FETs

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4.1 Introduction

In chapter two, we presented the upper limit of SiCNWFET by simulating devices operating in either ballistic or quasi-ballistic transport regime. Through this direct comparison with corresponding Si devices, we concluded that SiC is quite competitive to Si and experimental SiC NWFET could be realized and used in targeted applications. In this chapter, we present the operation of an experimental 3C-SiC nanowire FET. On the other hand, we analyzed the behaviour of NWFETs based on two different types of 3C-SiC nanowires, a) nanowires grown without catalyst in a convective furnace, and b) nanowires grown in a home-made CVD system based on VLS method (with catalyst assistance). These nanowire were grown and structurally characterized from our collaborators (Prof. S. K. Lee and D. Cornu). An analytical description of the NW growth method and 3C-SiC NWs physical characterization results are given in chapter 1 (section 1.4.2). We fabricated and electrical characterized devices based on these nanowires (section 4.2-4.3). Devices with either ohmic or Schottky contacts were observed leading to two different operation modes. Both types of nanowires led to similar device electrical behaviour. The similar NW quality explains the almost identical performance of these devices.

The Silvaco simulation package was used in order to fit the experimental output and transfer characteristics (section 4.4.1). This process allowed us to estimate, a) the quality of the nanowire/dielectric interface, b) the carrier concentration and carrier mobility along the nanowire in both types of nanowires (catalyst free grown and catalyst based nanowires). Beside this, the various shapes of experimental I-V characteristics, such as completely linear, non-linear symmetric, non-linear asymmetric were simulated by adjusting the SB at source and drain regions. Possible origins for the different values of SBs from contact to contact are proposed.

For cross checking of the fitting procedure, we also investigated the application of Silvaco simulation tool in Si nanowire FETs (4.4.2). More particularly, experimental FETs based on Boron-implanted Si nanowires were prepared (from Prof. Lee group). Both the process steps of device fabrication and the device operation were simulated using Silvaco simulation tool. Again, an agreement, in terms of electrical characterization, between Silvaco and experiment was noted down. This study was useful for two more reasons. The first one deals with the possibility of doping SiC NWs by ion implantation. This would be very useful for SiC NWs formed by conversion of Si NWs. The second one is related with the different electric behavior between ohmic and SB NWFETs. This study on Si NWs (with SB at contacts) incited us to investigate our SB-SiC NWFETs which, as it will be shown, exhibit better electrical performance compared to ohmic case.

4.2 Nanowire transistor fabrication

4.2.1 Nanowire solution preparation

In this part, we present the whole process of a NW FET fabrication starting from the manipulation of the NWs felt and ending up to the source and drain contacts formation. Although the fabrication process is common for both types of nanowires, we will focus on the catalyst-free grown 3C-SiC nanowires (some extra treatment in order to process the initial felt of nanowires is demanded). We received the as-grown nanowires in a felt form. The first step was to separate the NWs from the felt and disperse them one by one, if possible, over the substrate. Before doing this step, the oxide layer all around the nanowire should be removed. Below, we summarize the required preparation steps of the nanowires:

a) We put the 3C-SiC nanowires into pure ethanol and then we place the bottle with the solution in ultrasonic bath for 5 minutes in order to clean the silica layer from adsorbed organic species.
b) After that, the 3C-SiC nanowires are placed in HF (48%) for 96 hours (stick the nanowire felt between two porous plastic pieces in order to keep the whole felt inside the solution during the process) and then we clean them by dipping in pure water and ethanol (oxide removal step).
c) Immediately after the oxide removal, it follows the conversion of the 3C-SiC nanowire felt to powder (by mechanical milling). Next, we place the powder in ethanol and finally the bottle with the solution in ultrasonic bath for 1.5 minutes. In this point, we should mention that during the ultrasonic step, the nanowires are found to be broken mainly at the sections of stacking faults. This has as a result that from the initial nanowire length of few hundreds of micrometers, the final nanowire length was found to be only few micrometers (the majority of nanowires had length of 2-3 micrometers and only few over 10 micrometers).
d) The solution with the nanowires is ready for use. Before nanowire deposition, the solution is slightly shacked. Then, one or two droplets from the top of the solution are taken with the assistance of a micropipette and the nanowires are dispersed over the substrate.
e) The final step is to place the sample on a hot plate in order to evaporate the solvent.

4.2.2 Substrate preparation

In the first chapter, we presented the various nanowire based FET implementations. The most common device geometry is the back gated FET. In our experimental work, we followed this device fabrication geometry. The initial substrate is highly doped silicon, with a doping concentration around 10^{20} cm^{-3}, which serves as a back gate. The next step is a thermal oxidation which leads to the formation of the gate oxide of approximately 265 nm in thickness. In a back gated geometry, this thick oxide is common [1.46-4.4] due to the huge dimensions of the gate. In order to have a gate control the thickness of the gate oxide should be quite thick (this is a drawback for back-gated devices compared to front-gated where a very thin oxide can be implemented due to a small local gate of each device). After the oxidation, it follows a step of e-beam lithography to form the big metallic pads (for placing the electrical measuring tips), the alignment marks (for accurate e-beam lithography process) and the small geometrical features which are used to identify the position of each nanowire in the center of each field as shown in figure 4.1 and 4.2. Each sample has four regions, named as field 1, 2, 3 and 4. A zoomed in image of one field is shown in figure 4.2. At the corners of the pattern, there are four crosses, which serve as alignment marks.

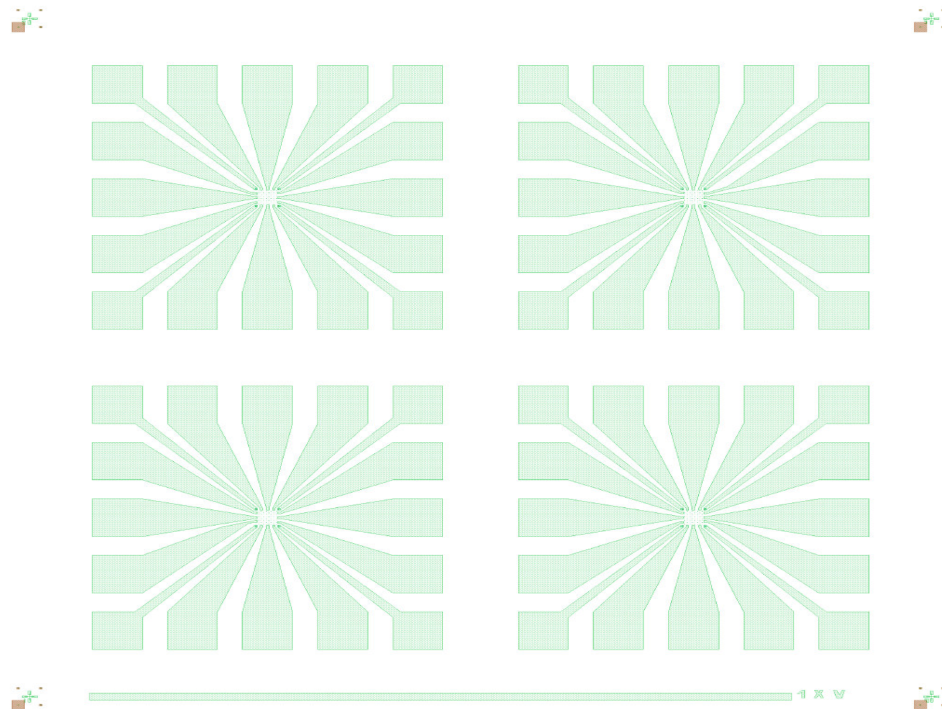

Figure 4.1 Pattern, which is used in the e-beam lithography process in order to define the big metallic pads, the alignment marks for the lithography and the geometrical features used to locate the NWs.

4.2.3 Metallic contacts fabrication; e-beam lithography

A field (a zoomed in view of the centre of one filed is shown in figure 4.2) is each one of the same four patterns in the mask design, containing a central area empty from metal regions where we expect to locate the nanowires (figure 4.1). The target is to locate abandoned nanowires in this region after their deposition over the substrate. This region is scanned with an AFM microscope in order to note down the exact position of each nanowire in relation with geometrical features which are generated on the substrate with the first e-beam lithography step. Along this central region, unique combinations of four geometrical features (like square, triangle, circle etc.) are able to specify the exact location of each nanowire. These geometrical features are indicated in figure 4.2.

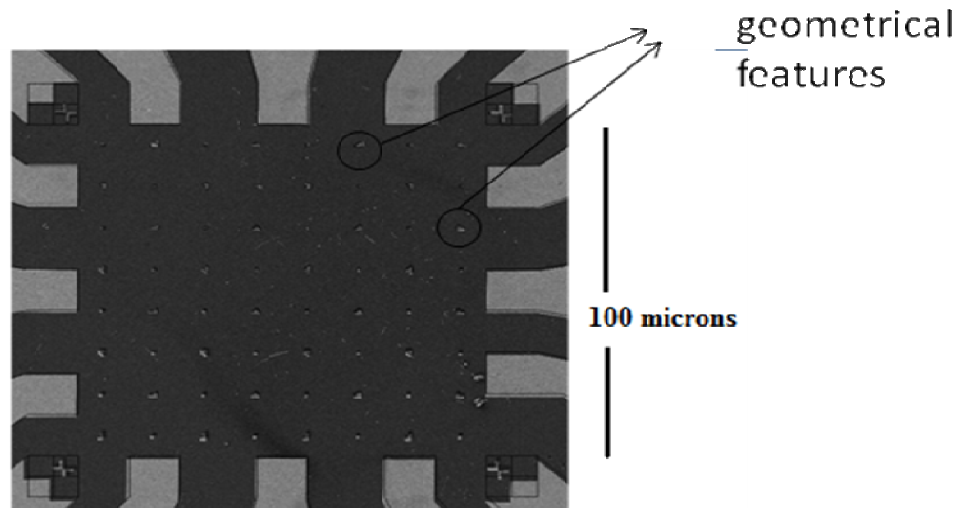

Figure 4.2 Zoomed in image of one field. Small geometrical features with a distance between them of 10 microns inside the 100x100 squared microns central region of the field are shown.

After the AFM image-based mapping of the substrate, we create the suitable mask design (example shown in figure 4.3). This design contains the initial metallic pads with the geometrical features at the center of each field, and the position of the nanowires after loading the AFM images into suitable design software. The aim of the design is to obtain at the end of the process, metallic lines of 2 μm width which will connect the edges of the nanowires with the neighbor big metallic lines as shown in figure 4.3. We end up to a structure shown in the SEM image of figure 4.4, after performing the second e-beam lithography step (based on the design mask of figure 4.3) and lift off process.

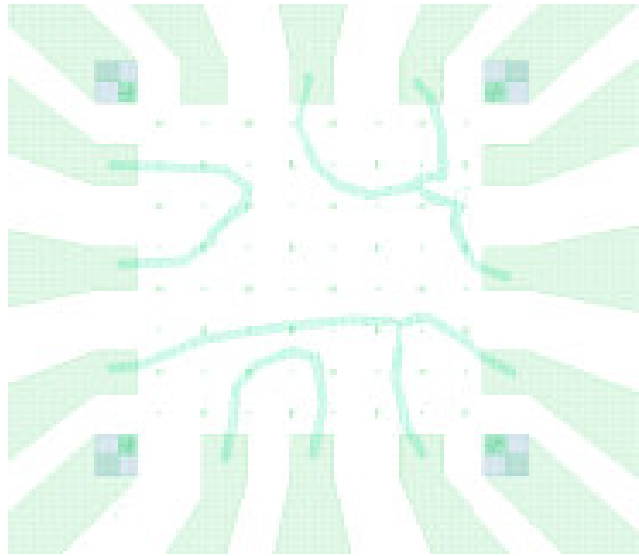

Figure 4.3 Field region after designing the small metallic lines and connecting the NW edges to the big metallic pads.

With the second e-beam lithography process, we just remove the PMMA from some regions (the PMMA is sensitive to electrons, and regions of PMMA exposed to electron beam are easily removed by appropriate chemical treatment), where we expect to deposit the metal and connect the nanowires. After this lithography on PMMA, a metal deposition (either Ni/Au or Ti/Au) by e-beam evaporator system followed by dipping the sample in acetone has as a result the formation of the metal lines. This process is named as lift off: the acetone removes the PMMA from the sample and in the same time the metal on top of the PMMA. Only at regions where the metal is contact with the SiO_2, metal is not removed after the lift off. In the SEM image of figure 4.4 the big metallic pads, the metallic lines created with the second e-beam lithography, the alignment crosses and the geometrical features are noted down.

The whole process is schematically summarized in figure 4.5. We start from the initial substrate (Si/SiO_2), with a first e-beam lithography step we form the metallic pads, the nanowires deposition and their AFM imaging are then followed. With a second e-beam lithography step we connect the nanowires with the metallic pads in order to be able to measure the I-V characteristics of the devices.

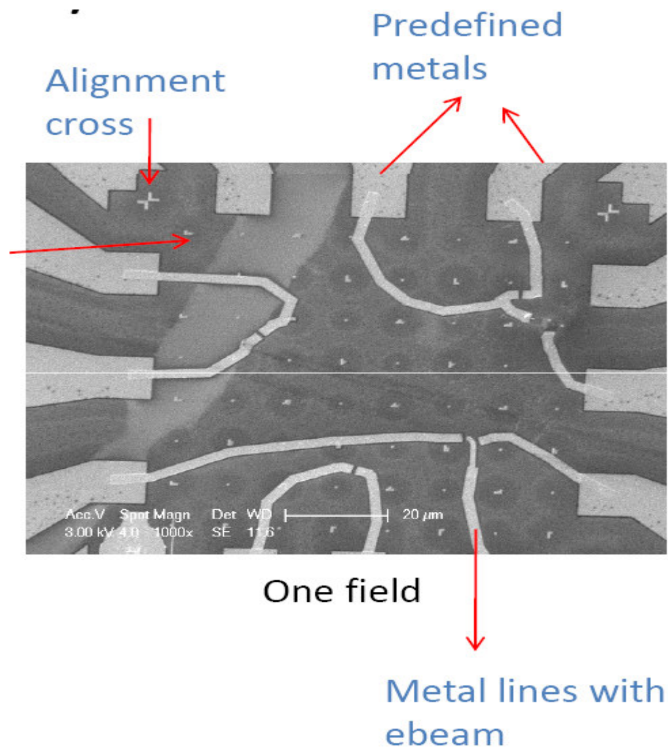

Figure 4.4 SEM image of the centre of one typical field after the e-beam lithography process. The alignment crosses at the edges, the predefined big metal pads and the metal lines fabricated withthe second e-beam lithography are noted down.

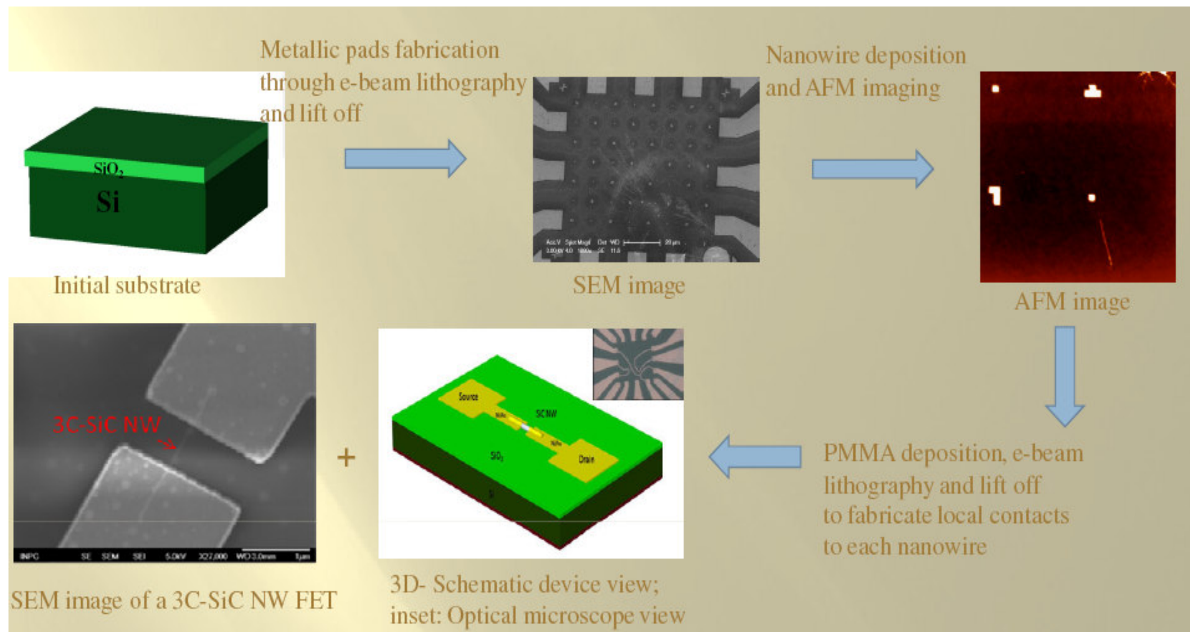

Figure 4.5 Process flow chart of 3C-SiC NW FET fabrication.

4.2.4 Device annealing and nanowire surface cleaning

It usually follows a step of oxygen plasma etching (power of 350 W and duration of 180 s) after the lift-off process. This cleaning procedure completely removes all the organics species from our sample e.g. PMMA remaining (circular nanoparticles in figure 4.6). PMMA remainings strongly affect the electrical transport properties of the nanowires. They act as virtual front gates which prevent the electrons to pass through. After oxygen plasma treatment, these particles are removed and the transfer characteristics are improved.

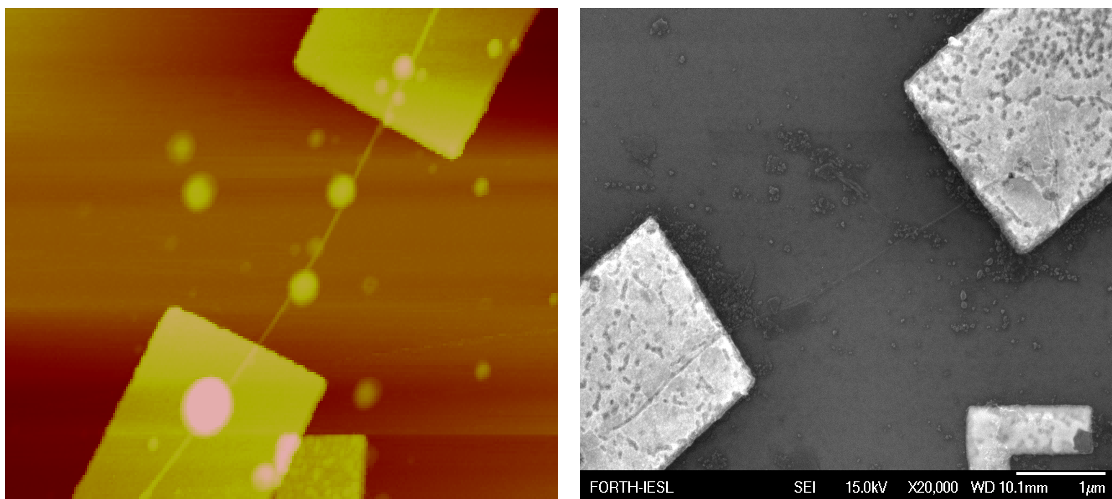

Figure 4.6 (a) AFM image of 3C-SiC NWFET; PMMA remaining particles after lift-off process.,(b) SEM image after RTA process. Voids and holes are shown in the metal lines surface

Apart from the above cleaning step, an annealing step always helps to improve the device performance. We electrically characterized our devices, before and after each rapid thermal annealing step (RTA) (60 s to raise up to 700 ^{o} C, dwell time 30 s and cool down in 60 s). The lowest RTA temperature was 500 ^{o} C and the maximum 700 ^{o} C. A general conclusion of the RTA process is that our devices are quite sensitive to this "violent" process. SEM (figure 4.6b)and AFM analysis revealed that many metal contacts were damaged and filled with holes and voids, especially at T>600 ^{o} C, and in some cases the initial distance (gap) of the contacts (around 400 nm) was tend to be zero (the contacts were melted and connected). Many devices after RTA (>600 ^{o} C) were not anymore operational. The high surface roughness and the visible physical damage of the metal contacts after RTA, in combination with the short nanowire length explain this finding. Another possible factor is the thermal stress appearing during RTA process.

4.3 Electrical characterization

The electrical characterization revealed a similar behaviour for devices based on catalyst-free and catalyst based grown nanowires. Beyond this point, we will not make a distinction between devices based on these two differently grown nanowires. The back-gated NWFETs have channel length varying from 500 nm to 4 microns (depending on the nanowire initially length) and the nanowires diameter is ranged from 20 to 40 nm (figure 4.7). As we have already mentioned in the introduction of this section, two different device's operation modes were observed depending on the nature of the S/D contacts, ohmic or Schottky.

4.3.1 3C-SiC NWFETs with ohmic contacts

Electrical characterization was performed before and after RTA and oxygen plasma etching steps in order to monitor the behaviour of the devices during these treatments. A general comment before the annealing step is that the I-V characteristics of the devices with Ti/Au metals were less stable in comparison with Ni/Au. In addition, self annealing through Joule heating was observed only for the case of Ti/Au by revealing the role of conductive titanium oxide that is easily formed at the interface of Ti and 3C-SiC (see section 4.3.3). After lift-off process, PMMA remaining were found on the nanowires and the contacts degrading in this way the I-V characteristics. After oxygen plasma treatment all the organics were removed and this led to better electrical performance.

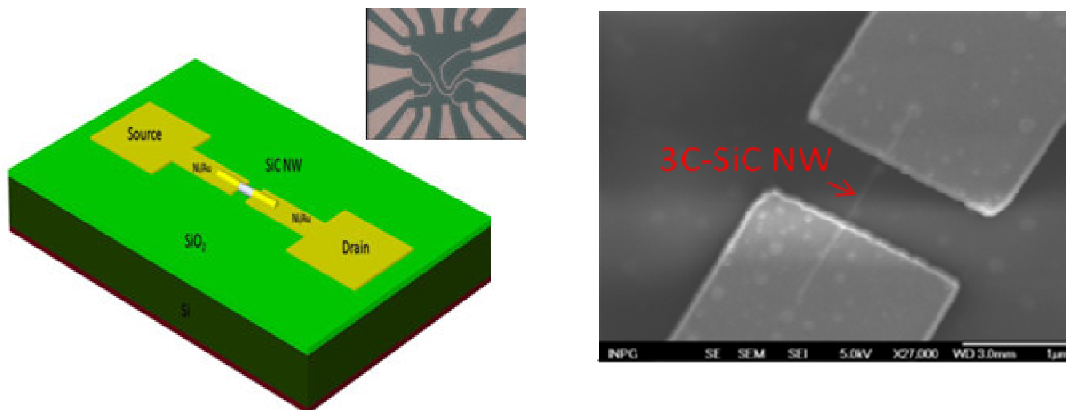

Figure 4.7 (a) 3D device schematic view (inset: optical image of devices), and (b) typical SEM image of the device.

Many devices presented linear output characteristics (figure 4.8a), revealing in this way the ohmic nature of S/D contacts. The gating effect, in other words the change of drain current by the gate voltage, is very weak. By increasing positively the gate voltage, the drain current is slightly increased, showing electron conduction through the nanowire. In addition, even in the case of very high negatively values of gate voltage the drain current could not be completely suppressed. This is a direct effect, as it will be also revealed from the parameter extraction, of the high carrier concentration along the nanowire that prevents depletion of the conduction channel.

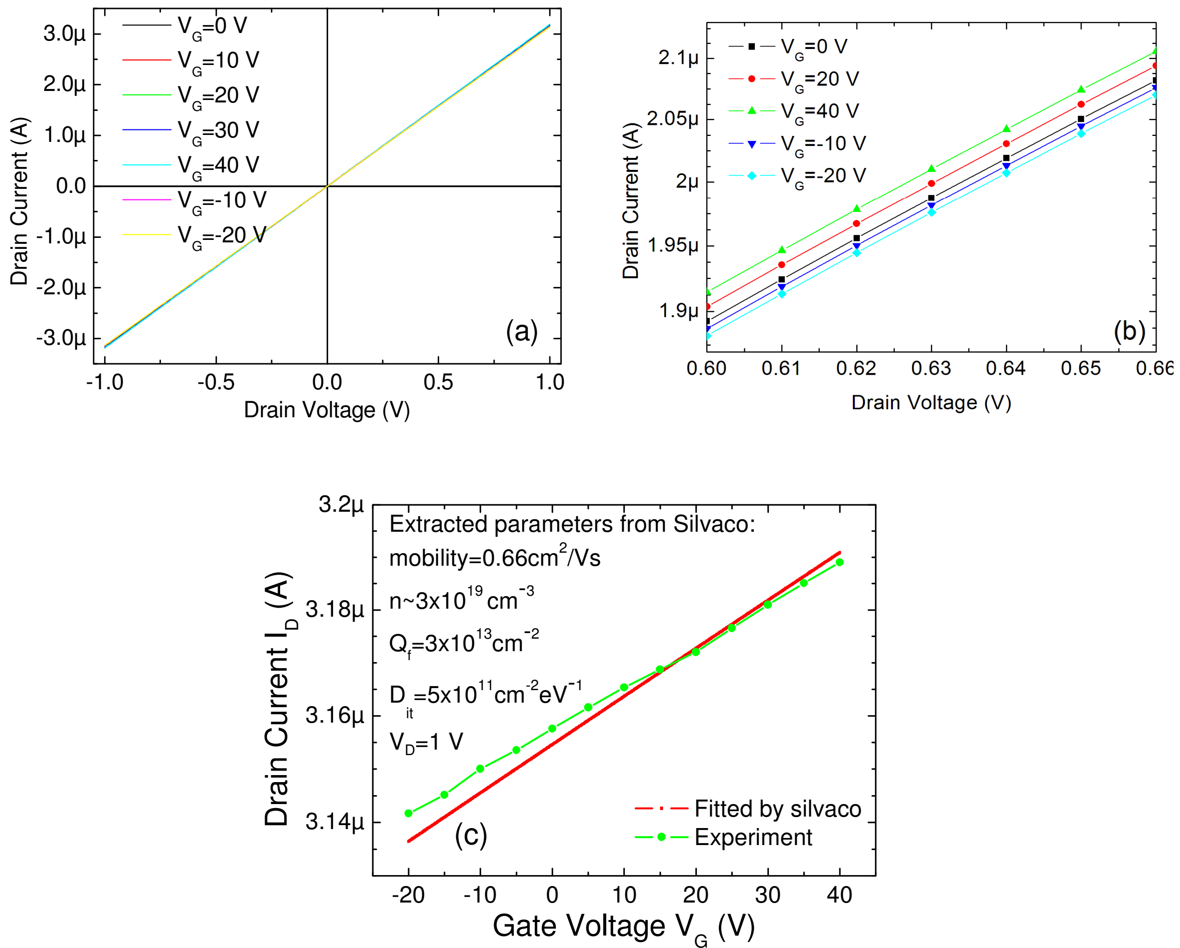

Figure 4.8 (a) Experimental output characteristics, (b) zoomed in view of (a) and (c) experimental and fitted with Silvaco transfer characteristics of 3C-SiC NWFET. The best fitting was obtained when mobility is equal to 0.66 cm^2/Vs, $n=3x10^{19}$ cm^{-3}, $Q_f=3x10^{13}$ cm^{-2} and $D_{it}=5x10^{11} cm^{-2} eV^{-1}$.

We followed the approximated extraction model which was presented in chapter one (eq. 1.1-1.3) in order to extract the mobility and the carrier concentration from the transfer and output characteristics. The transconductance of 3C-SiC NWFET was computed as g_m=0.7 nS. Following this commonly used approximation method, the estimated experimental electron mobility was 0.11

cm^2/Vs. Using eq. 1.3 the electron concentration was calculated equal to $6 \cdot 10^{19}$ cm^{-3}. This high carrier concentration, close to the metallic limit, explains the very weak gating effect. Our SiC NWFET with ohmic contacts has a comparable behaviour (mobility value in the same order of magnitude, same high carrier concentration etc) with the state of the art devices presented by other groups before the beginning of our thesis [1.46]. We fitted the experimental I-V characteristics with Silvaco simulation tool [4.2] with error less than 2% (figure 4.8c). Details on the simulation will be presented in section 4.4.

4.3.2 3C-SiC NWFETs with rectifying behaviour contacts

During our stay in Korea (Prof. S. K. Lee group, Chonbuk University) we investigated Si-based NWFETs with Schottky barrier at S/D contacts (see later section 4.4.2). The results of this investigation incited us to carefully study the electrical characteristics of all our 3C-SiC NWFETs and analyse the behaviour of devices with Schottky barriers at S/D contacts [4.1]. In figure 4.9, the I-V characteristics of one device (with Ti/Au 50/50 nm contacts) before and after a RTA annealing step (at 600 ^{o}C) are shown. By comparing the I-V characteristics before (figure 4.9a) and after RTA (figure 4.9b) of the rectifying (Schottky-like) behaviour contacts to the NWs, we observe that RTA converts a strongly asymmetric and non-linear I-V characteristic to an almost symmetric and linear one. A small remaining SB at S/D is the origin for this non-linear I-V [4.3] comparing to figure 4.8a-b. This time the gating effect is more effective and in addition, by applying a suitable gate voltage the device can be switched off. From the I-Vs the determined value of transconductance is 3.88 nS. Following the same procedure as previously described, the carrier mobility was estimated equal to 1.21 cm^2/Vs. Due to the SB at S/D, the device switching off is now possible (V_{th}~4 V) resulting to an $I_{ON}/I_{OFF} \sim \cdot 10^3$. Apart from the possible switching off of the devices, the SB-NWFET devices present a six-times higher transconductance and more than one order of magnitude higher electron mobility. The improvement will be more evident if we calculate the intrinsic transconductance, by taking in account the contact resistance, which in the case of SB-NWFET is higher than the ohmic case [4.4].

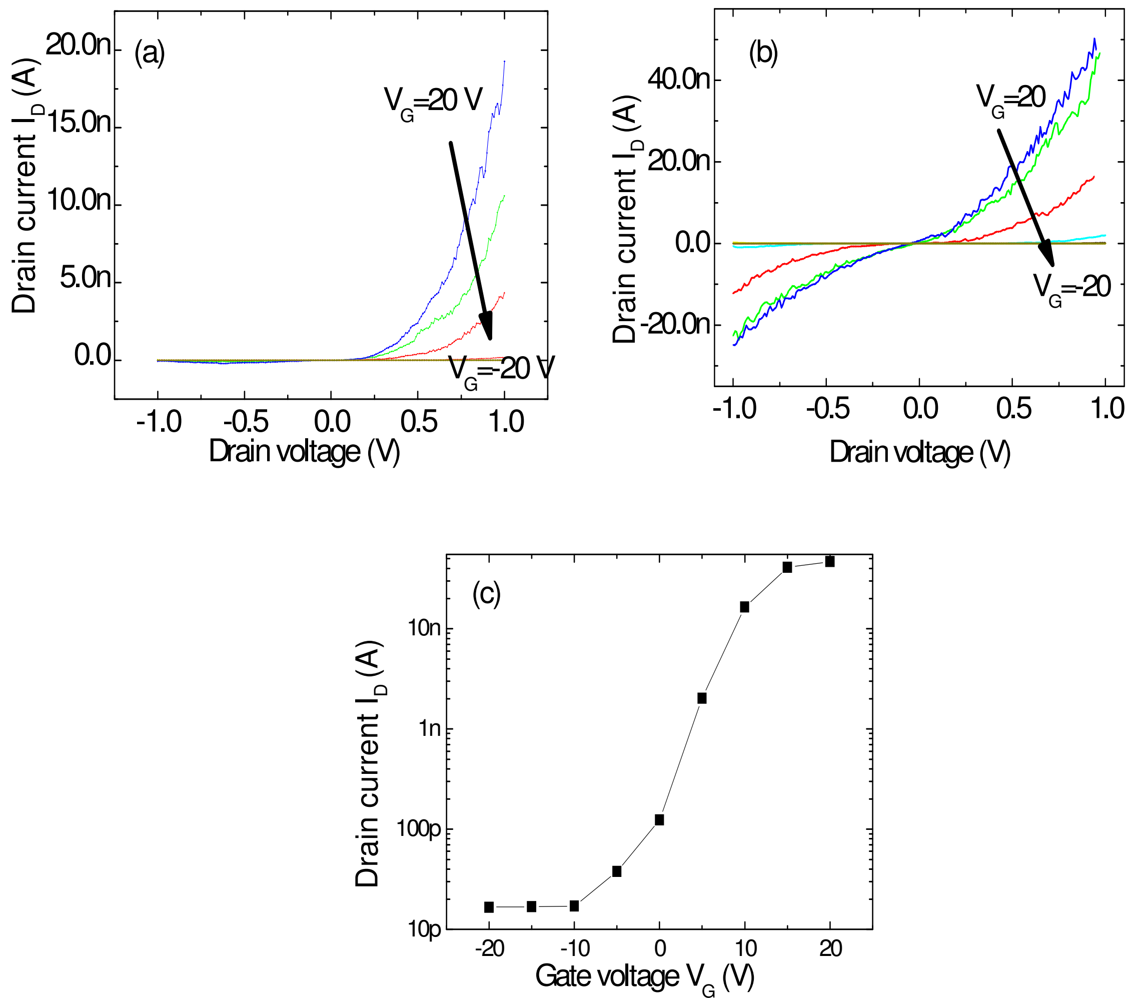

Figure 4.9 Output characteristics of a SB-NWFET before (a) and after RTA (b); (c) transfer characteristics (log scale) after RTA at V_D=0.01 V.

The weak gating effect of the ohmic-contact devices is a combined result of the high carrier concentration and the ohmicity of S/D regions that do not permit the modulation of the carrier concentration by the gate voltage either by adjusting the transparency of the barriers at S/D regions or by increasing the carrier density of the accumulation layer. In the case of ohmic contacts (zero SBs) even for V_G=0 V a significant current could pass through the nanowire by applying a small drain voltage, restricting somehow the V_G-dependent carrier modulation. When a non-zero SB is present, the gate voltage adjusts the transparency of the barriers by appropriately moving the potential bands (back gate FET geometry), leading to an indirectly modulation of the drain current (figure 4.10) [4.1].

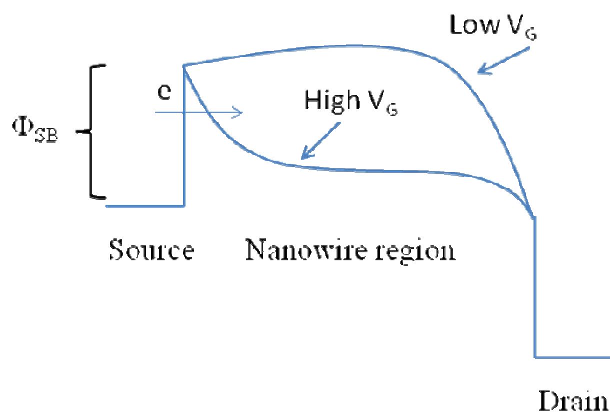

Figure 4.10 Potential profile along transport axis for low and high gate voltage in a SB-NWFET, where Φ_{SB} is the initial Schottky barrier height.

Schottky barrier at S/D regions acts beneficially for the FET performance by significantly suppressing the off current. At higher positive gate voltages, the Schottky barriers tend to be extremely transparent leading to high transconductance and I_{ON}/I_{OFF} ratio. In the case of unintentionally highly-doped nanowires, where the direct effect of the gate voltage on the accumulated carriers is negligible, SB-NWFET presents improved performance by suppressing the off-current and indirectly modulating the drain current through the control of Schottky barriers transparency at source and drain regions

4.3.3 Self heating annealing effect

During the electrical characterization of NWFETs prior to annealing we noticed a self-heating annealing of the contacts due to the Joule effect. This was observed only for devices with Ti/Au contacts by revealing the role of conductive titanium oxide that is easily formed at the interface of Ti and 3C-SiC. From the measurement sequence in figure 4.12, it is obvious an abrupt increase of the drain current at V_G=30 V. The fact that the device geometry is a back gated FET, allows the gate voltage to control also the contact regions except from the channel region. While the gate voltage increases at positive values, this result to thinner Schottky barriers at source and drain regions permitting more current to pass through (figure 4.10). This high current heats the nanowire and the contacts (Joule effect) and a self-heating annealing is observed. After many measurements, the output characteristics are stabilized, as shown in figure 4.13. A remaining Schottky barrier at source and drain region is the explanation of the non-linear I-V characteristics.

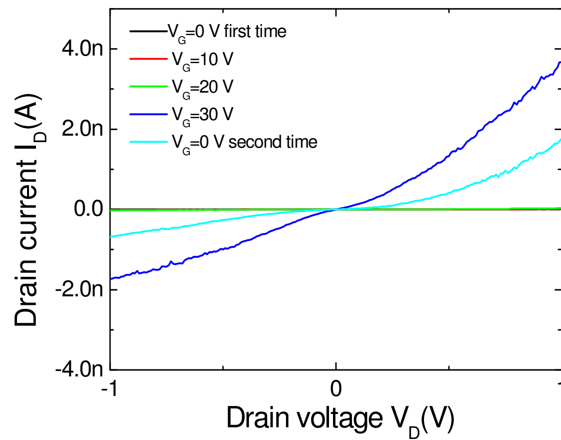

Figure 4.11 Output characteristics of 3C-SiCNWFETs with Ti/Au contacts prior to RTA annealing. The sequence of measurements was i) V_G=0 V (first time), ii) V_G=10 V, iii) V_G=20 V, V_G=30 V and V_G=0 V (second time).

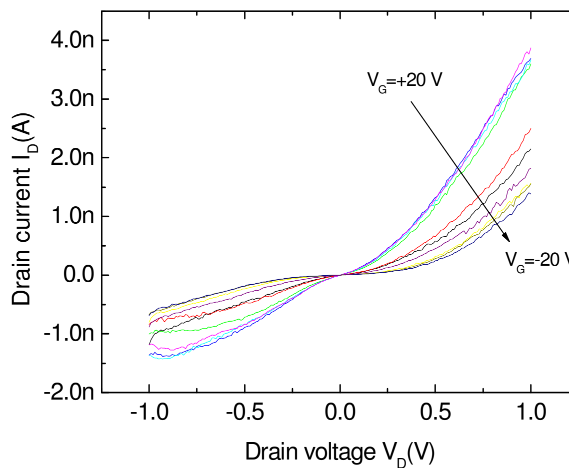

Figure 4.12 Output characteristics of 3C-SiCNWFETs with Ti/Au contacts after self-annealing through Joule heating.

4.3.4 Conclusions

We fabricated and electrically characterized back gated FETs based on 3C-SiC nanowires. Two different types of nanowires were incorporated, nanowires grown with and without catalyst assistance. Electrical characterization revealed no different behaviour between devices with different type of nanowires. This is in agreement with the structural characterization of the nanowires. Both types of nanowires contain many of stacking faults and defects and are probably nitrogen contaminated during the growth which results to an unintentional doped of approximately 10^{19} cm^{-3}. The high carrier concentration is the main drawback of the material.

By using nanowires grown with and without catalyst, devices with either ideal ohmic or Schottky barrier contacts were observed leading to two different device operation modes. Devices with ohmic contacts manifest very weak gating effect and a switch off is not achievable even for high negative gate voltages. In contrast, the small SB at source and drain regions acts beneficially for the device performance by suppressing the off current. At higher positive gate voltages, the Schottky barriers are transparent leading to higher (compared to ohmic contact devices) transconductance and I_{ON}/I_{OFF} ratio, 3.88 nS and $2.81 \cdot 10^3$, respectively. In the case of highly unintentionally doped nanowires, where the direct effect of the gate voltage on the accumulation carrier density is negligibly, SB-NWFET presents improved performance by suppressing the off current and indirectly modulating the drain current by adjusting the current transparence at source and drain regions.

4.4 Simulation of device fabrication process and electrical behaviour

4.4.1 3C-SiC nanowire FETs

Introduction

In chapter two, we presented in detail the modeling and the simulation of 3C-SiCNWFETs operating in ballistic and dissipative transport regime. The target was to investigate the upper limits of the device performance in the nanoscale. To this end, a sophisticated algorithm based on Poisson-NEGF formalism was incorporated. It was also shown, that for larger devices (>100 nm) a drift-diffusion model is capable to describe the electrical transport properties. Henceforth, we present the usage of a commercial simulation tool [4.2] in order to fit experimental I-Vs of devices based on 3C-SiC nanowires. Although the Silvaco module which we used is a 2D, we accurately calculate the 3D current through our devices but multiplying the 2D current by the width of the nanowire. This is a good approximation due to the fact that the dimensions of our experimental nanowires (diameter ~ 90 nm) allow us to neglect strong quantum effects. It is depicted, that this method is able to predict with accuracy the device operation and estimate the nanowire/dielectric interface quality, the nanowire carrier concentration and mobility and the

various I-V characteristic shapes by controlling the Schottky barriers height at the source and drain regions.

Apart from the case of 3C-SiC nanowires, this method was also applied to the case of Si nanowire FETs. Silvaco [4.2] (Atlas module) solves the Boltzmann transport equation within the drift-diffusion approximation self consistently with the Poisson equation (as presented in chapter 2). Indeed, at the micrometer scale the drift-diffusion model used in Silvaco is a well-adapted tool to describe electronic transport in semiconductor devices operating within a diffusive transport regime. To obtain accurate results for MOSFET simulations, it is necessary to account for the mobility degradation that occurs inside inversion/accumulation layers. The degradation normally occurs because of the substantially higher surface scattering near the semiconductor to insulator interface. It is well known that fixed charges near the gate side are responsible for the shift of the threshold voltage, and interface trap charges can change the subthreshold slope. The above are more critical in the case of a nanowire FET where the ratio surface to volume atoms is very high. In the present work, in order to have as much as more realistic simulation, a mobility model, which includes transverse field, doping dependent and temperature dependent parts was used. The mobility model that Silvaco uses is based on the Lombardi model [Lombardi et al, IEEE TCAD, 1988]. The total mobility is given from Matthiessen rule:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad \text{(eq. 4.1)}$$

The first component, μ_{AC}, is the mobility limited by scattering with surface acoustic phonons:

$$\mu_{AC}=B/E + C\times N^a/(T\times E^{1/3}) \quad \text{(eq. 4.2)}$$

where E is the electric field, N is the doping concentration, T is the temperature and B, C, A are equation parameters without a physical meaning. The third component, μ_{sr}, is the surface roughness factor and is given by:

$$\mu_{sr}=\delta/E^2 \quad \text{(eq. 4.3)}$$

where the value of $\delta=5.82*10^{14}$ V/s. This parameter value was obtained from TEM data [Lombardi et al, IEEE TCAD, 1988] (it is a measure of surface roughness fluctuations). Finally, the part that computes the mobility of the bulk material (or body mobility) and has the biggest impact (in our case) in the total mobility value is given by:

$$\mu_b= \mu_0 \exp(P/N)+ [\mu_{max}(T/300)^{-\gamma}-\mu_0]/1+(N/R)^k]-\mu_1/[1+(S/N)^b] \quad \text{(eq.4.4)}$$

where again the μ_1,P,R,S,γ,k and b are equation parameters without physical meaning, but in contrast μ_0 and μ_{max} have physical meaning and in fact they correspond to the surface and the bulk mobility respectively.

Apart from the modifications (we used μ_0 and μ_{max} as free parameters during the fitting process) in the mobility model, we inserted in our simulated devices interface defects, like fixed charges in the dielectric and interface traps. It is well known that fixed charges near the gate side are responsible for the shift of the threshold voltage, and interface trap charges can change the subthreshold slope. The above are more critical in the case of a nanowire FET where the ratio surface to volume is very high. The effect of the total charge on the threshold voltage is given by:

$$V_{\mathrm{G}}(\Phi_{\mathrm{S}}) = V_{\mathrm{FB}} + \Phi_{\mathrm{S}} - \frac{Q_{\mathrm{SC}}(\Phi_{\mathrm{S}}) + Q_{\mathrm{tot}}(\Phi_{\mathrm{S}})}{C_{\mathrm{ox}}} \qquad \text{(eq. 4.5)}$$

where $Q_{tot} = Q_{it} + Q_{ox}$ is the total fixed charge, which contains the interface trap and the fixed oxide charges. We have to mention at this point that in order to have change to the slope of the I-V due to the traps we should simulate transient measurement (by applying pulses) and not static measurement in Atlas.

We would like to mention, that we used commercial software instead of our custom drift diffusion code (results presented in chapter two), due to its better computational efficiency and the ability to incorporate various models for carrier mobility, nanowire/dielectric interface, defects etc. The only difference between experimental and simulated devices exists in the shape of the NW cross-section, which is square for the simulated devices whereas the experimental nanowires have a circular one. As shown in [4.20], the cross-section shape of the nanowire has a minor impact on the electron energy even for extremely narrow wires.

Effect of nanowire doping and interface quality

The target of this study is to simulate the behaviour of our experimental devices and by fitting the data to extract information about our transistors such as interface quality, carrier mobility and concentration etc. The experimental data are extracted from NWFET devices based on catalyst-assisted grown 3C-SiC using as a dielectric silicon nitrate (Si_3N_4). We used nitrate instead of silicon dioxide in order to investigate the NW/dielectric interface quality on device performance by

knowing that this interface is worse than the 3C-SiC/Silicon dioxide system. The device fabrication process is similar with that presented in section 4.2. The simulation of the experimental device was performed by varying the doping level of the NWs and by taking into account fixed charge and interface trap charge effects. A typical schematic view of our experimental devices is shown in figure 4.13.

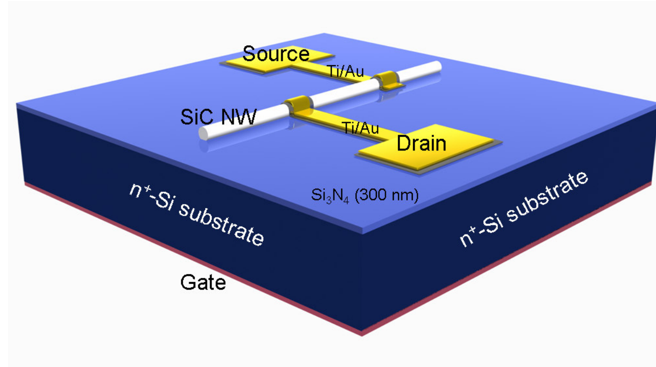

Figure 4.13 Schematic view of SiC NWFET.

Figure 4.14 shows the experimental (left column) and simulated (right column) I-V characteristics of 3C-SiC NWFETs with NW dimensions of 90 nm diameter and 4.4 μm in length [4.12]. By following the same procedure as previously described (using the approximated cylinder to plate capacitance model for the mobility extraction), the estimated electron carrier density and the field-effect carrier mobility for the single 3C-SiC NW FETs were estimated to be ~ 1.7×10^{20} cm^{-3} and ~ 0.5 $cm^2/V{\cdot}s$, respectively (eq. (1.1)-(1.3)). This experimentally estimated mobility is very low in comparison with that expected in bulk and/or thin film 3C-SiC. Silvaco was used in order to fit the experimental characteristics and by using a special module of Silvaco, the “optimizer”, we estimate the conditions of the best fitting. We used the nanowire doping level, the electron mobility value and the interface quality in terms of Q_f and D_{it} as our free simulation parameters. An agreement between experiment and simulation, as is shown in figure 4.14, is obtained when using in the simulation the parameter values below: (a) a n-type doping of NWs equal to 1×10^{19} cm^{-3}, b) maximum body mobility and surface mobility equal to 57.75 cm^2/Vs and 2.51 cm^2/Vs respectively, c) density of fixed charge Q_f=8.52 10^{13} cm^{-2} and, d) density of interface trap electron acceptor states D_{it} equals to ~1.5 10^{12} eV^{-1} cm^{-2} [4.13, 4.14]. In [4.14] a detailed analysis of 3C-SiC/SiO_2 system in terms of Q_f and D_{it} is presented and at the interface of n-type thin film 3C-SiC/SiO_2 MOS capacitors, the density of traps close to the conduction band edge reached values in the range of 10^{11} cm^{-2} eV^{-1} (by using suitable process such as special surface cleaning, strict control of the chamber atmosphere etc.). Our nanowire/dielectric interface has higher density of traps (by one magnitude of order) compared to bulk capacitors. As far as concerns the mobility

parameters, the maximum body mobility and the surface mobility, they belong to a build-in mobility model of Silvaco. This model assumes that at the center of the inversion/accumulation layer the mobility takes the maximum value equal to maximum body mobility and as we are approaching the surface the mobility degrades reaching the surface mobility value.

According to the above parameters, Silvaco calculates a total mobility value equal to ~ 3.5 cm^2/Vs. The difference between the value of total mobility that Silvaco predicts (~3.5 cm^2/Vs) and the estimated from the cylinder-plate capacitance model value (0.5 cm^2/Vs) could be justified by the lack of accuracy of the cylinder-plate capacitance model (interface traps and parasitic effects are neglected in equation (1.1) which leads to underestimated experimental mobility values (at least a factor of 2)) [4.14-4.17]. This remark might also explain the discrepancy between the estimated experimental value (~1.7×10^{20} cm^{-3}) of doping level (using eq. (1.3)) and the one resulting from Silvaco simulation ($1x10^{19}$ cm^{-3}). Another difficulty with nanowire FETs is the experimental estimation of the interface traps density and fixed charges. The classical C-V measurement approach is not suitable for nanowire FET configuration due to the very small device capacitance. New elegant experimental techniques have to be developed. Nevertheless, using the Silvaco software tool, and through the best fitting between experiment and simulation, the density of fixed charge and the density of interface trap states of our experimental devices were roughly estimated.

The effect of doping on the performance of the NWFET was studied by simulating the operation of devices with the same geometry as that of the experimental devices and with ideal (table 4.1, figure 4.15 and figure 4.16) nanowire/silicon nitride interface (zero defects). The simulation was performed from a maximum doping level of $1 \cdot 10^{19}$ cm^{-3} and it was gradually decreased down to a level of 10^{15} cm^{-3}. We assumed perfect 3C-SiC NW/nitride interface, so this time we used as maximum body mobility [ohmic (pure-lattice) electron mobility] the maximum value of bulk 3C-SiC electron mobility which is ~1000 cm^2/Vs (the model takes in account the doping dependence of the mobility so the mobility when the doping is ~10^{19} cm^{-3} is much lower than this value). Table 4.1 summarizes the results of the electrical devices' performance with ideal nanowire/dielectric interface in terms of transconductance and field effect (FE) electron mobility (using the approximate cylinder-capacitance model) for different nanowire doping levels. According to the simulations (table 4.1, figure 4.15 and 4.16), it is obvious that the control of the unintentional doping and nanowire/dielectric interface quality is necessary to obtain high performance NWFETs [4.12].

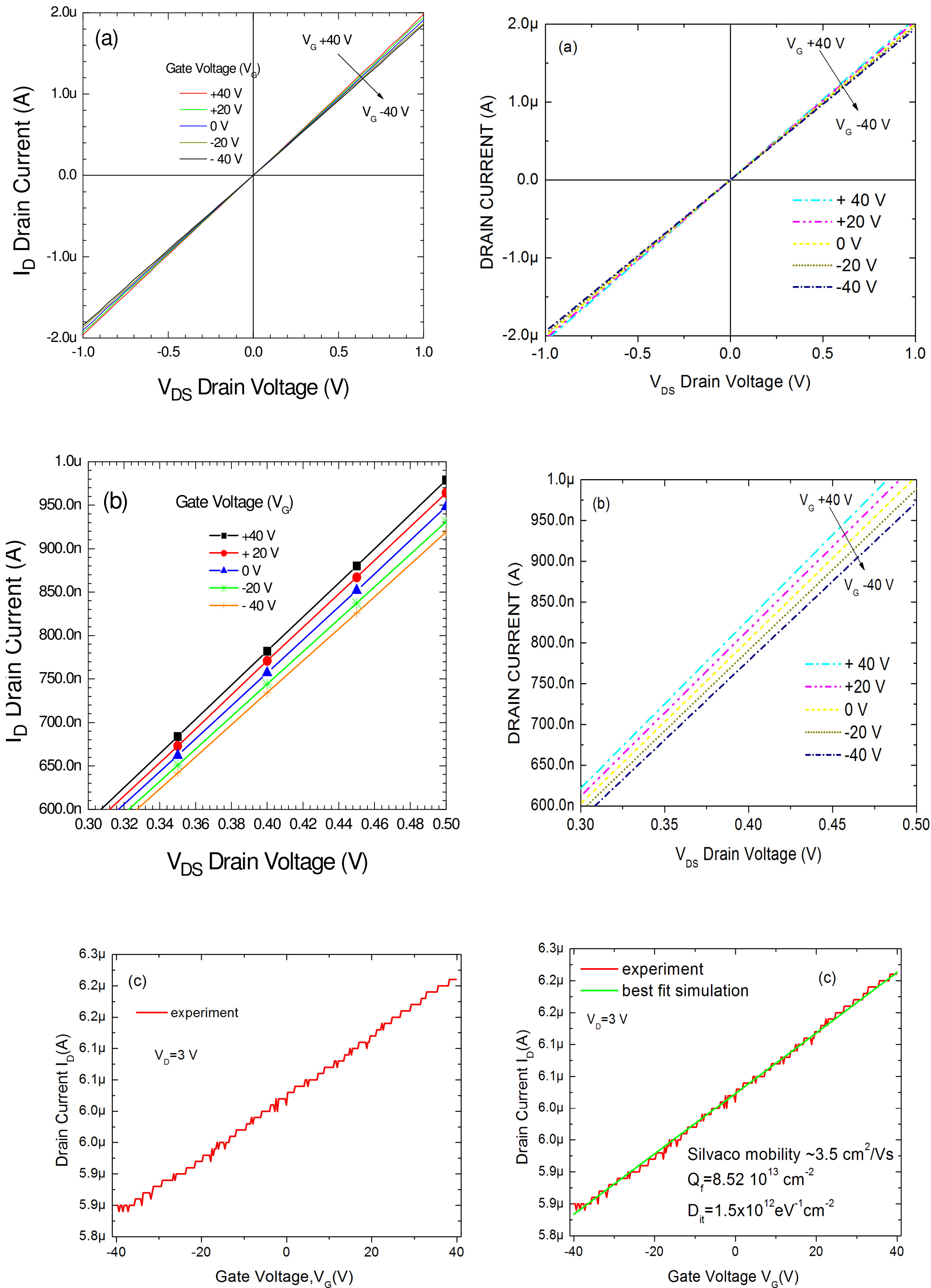

Figure 4.14 Experimental (left column) and simulated (right column) characteristics of single SiC nanowire FET: (a) I_D-V_{DS} characteristics curves for V_G values of +40, +20, 0, -20, and -40 V, (b) enlarged plot of (a), (c) I_D-V_G curve at V_{DS} of 3V [4.12]

Table 4.1 Comparison of the simulated device performances with ideal interface

NW n-type doping (cm^{-3})	FE Mobility at V_D=0.02 V (cm^2/Vs)	Transconductane (10^{-9}A/V)	V_{th} (V)
10^{15}	88.0	6.425	0.2
$5x10^{15}$	90.7	6.624	- 0.25
10^{16}	89.3	6.522	-0.30
10^{17}	60.5	4.418	-7
10^{18}	25.5	1.864	NSO*
10^{19}	10.8	0.792	NSO

*NSO: Non-Switched Off.

Indeed, the calculations showed that, in the absence of interface fixed oxide and interface traps, and at a doping level of 10^{17} and below, it is possible to have a good gating effect (figure 4.15) even for small V_D and the FET is switched-off with small negative gate voltage (V_{th} ~-0.5 V) (figure 4.15) . Optimum operation (highest μ and g_m) has been obtained for a NW doping level of $5x10^{15}$ cm^{-3} (as shown in table 4.1). Figure 4.15 and figure 4.16 show the corresponding 3C-SiC NWFET electrical characteristics. If very high values of fixed charge in dielectric and interface trap states are taken into account in the above simulation, it turns out that the device performance is poor, independently of the doping level. In this case, the NW FET cannot be switched-off (for high Q_f and D_{it} values) even for low doping concentrations. This shows that the effect of the interface quality is as critical for the device performance as the value of the doping level. A combination of a low doping level (lower than the 10^{19} cm^{-3}) and as better as possible nanowire/dielectric interface (as smaller as possible Q_f and D_{it} values) would lead to much better device performance.

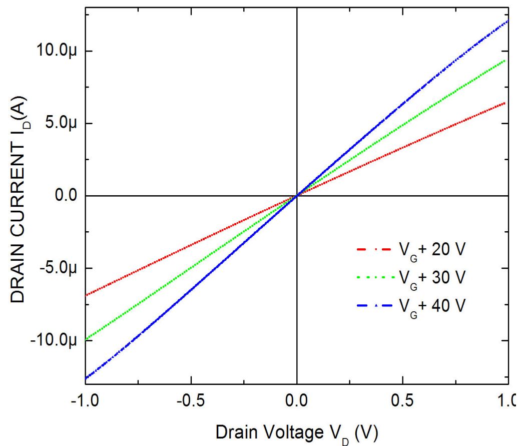

Figure 4.15 Simulated I_D-V_D characteristic for n-type doped SICNWFETs with $5x10^{15}$ cm^{-3} and ideal interface (no defects).

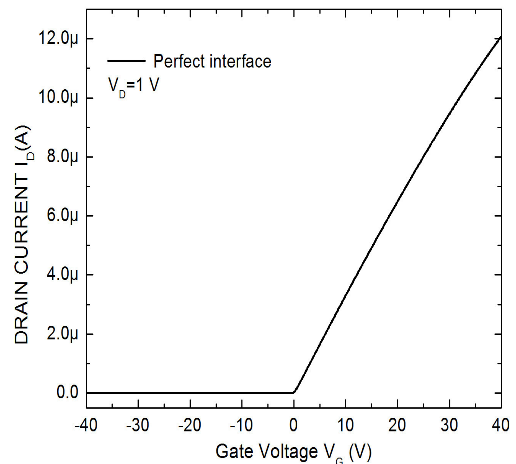

Figure 4.16 Simulated transfer I_D-V_G characteristic for n-type doped SICNWFETs with $5x10^{15}$ cm^{-3} and ideal interface.

SB-SiC NWFETs

In this study [4.34], we attempted to explain with the assistance of Silvaco, the various I-V characteristic shapes observed (linear, non-linear symmetric and asymmetric) even for devices belonging to the same initial wafer part. With the assistance of simulation, we showed that this is a result of different values of SBs at source / drain contacts of the FETs.

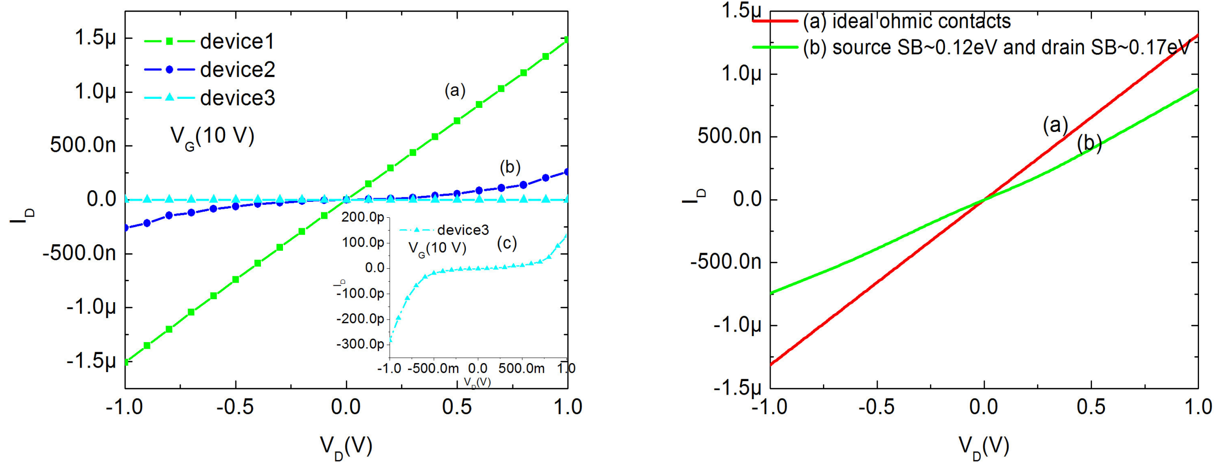

Figure 4.17 (left)Experimental I-Vs from various NWFETs of the same sample; inset: zoom for device, (right) Simulated I-Vs for (a) ohmic and (b) Schottky source and drain contacts with small difference in barrier heights.

The experimental I-V characteristics of three NWFETs of the same sample are shown in figure 4.17 (left). As it is obvious from the linearity of the I-V device 1 has ohmic contacts while devices 2 and 3 have non linear I-Vs. As depicted from simulation results (figure 4.17 right), the different SBs of S/D lead to these non linear I-V characteristics. By using ohmic or Schottky contacts (with a non-zero SB), we reproduced the non-linear shape of the experimental I-V. As shown in figure 4.17, the application of non-zero and not equal SBs at the S/D contacts has as result the non linear I-V shape (curve b in figure 4.17 right). When ohmic contacts are considered at the same device, Fig. 4.17right, curve (a), then a linear I-V is obtained. At this point, we have to mention that in the case of small difference between source and drain SBs, as in case of curve (b) of figure 4.17 right, the accurately fitting of the experimental results with Silvaco software is not possible. When ohmic contacts are considered and when the SB difference is quite big like in the case of B-implanted Si NW (see next section), then accurate fitting with the experimental results is achievable

Using Silvaco simulation tool, we investigated the effect of SB height on transfer characteristics of a device with similar geometry with our experimental NWFETs (our experimental

device presented in section 4.3.2) when only thermionic current over the barrier is included (black curves of figure 4.18) and when both thermionic and tunnelling current (red curves) through the barrier are taken in account. For this simulation, a nanowire doping level of $5x10^{15}cm^{-3}$ was assumed. Figure 4.18 shows that tunnelling current dominates for higher values of SB height (>0.25 eV). Returning back to our experimental devices and in figure 4.10, when a high gate voltage is applied the effective Schottky barrier at the contacts is modified leading to increased tunnelling current.

The fact that the devices with ohmic and rectifying-like contacts belong to the same wafer exclude all the other reasons such as different metallic material or different fabrication process in order to explain this different behaviour. Non-uniformity in annealing, NW doping level [4.6] and high interface traps density (that pins the Fermi level) as well as the high sensitivity of the metal-NW contact to local surface contaminations [4.7-4.10] might explain the different SBs between source and drain. In [4.8-4.10] the researchers noticed a similar behaviour with non-linear I-Vs of Carbon Nanotube (CNT) FETs. Lu et al. [4.9] used intentionally a chemical in the process of one of the two metal contacts surface of a CNTFET and they noted asymmetric I-Vs due to the different SB at source and drain contacts. Moreover, they presented ab-initio calculations and they showed the increased sensitivity of the metal work function to these chemicals. Kim et al. [4.10] showed that remaining from the PMMA (due to imperfect development) during the lift-off process step might have an impact to the SB of the contacts. Experiments that are more specialized should be performed in order to identify the origin of these different contact SBs of the same device. If not, a bottleneck in the mass production of nanowire FET devices will be present.

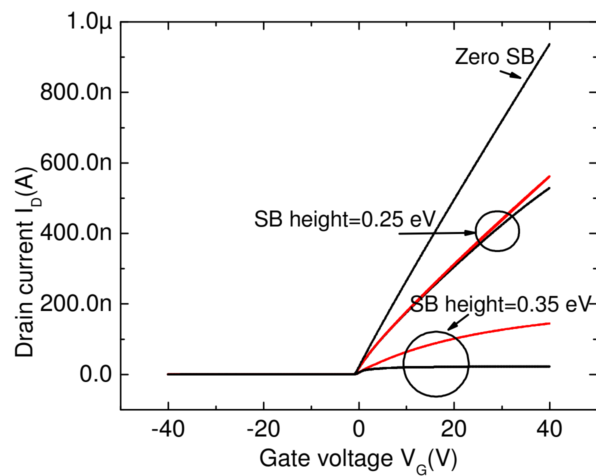

Figure 4.18 Simulated transfer characteristics with Silvaco for a similar device geometry to our experimental NWFET (V_D =1 V). For high SB height values, tunnelling current dominates (red lines include tunnelling effect).

4.4.2 Ion implanted Si nanowire p-FETs

Introduction

Our collaborators from Korea grew undoped Si NWs and through boron implantation they doped the NWs with holes. In this way, they fabricated a p –NWFETs [4.18]. This method allows to fabricate both n and p nanowire MOSFETs starting from undoped Si nanowires. This process seemed appropriate for our study since a problem of doping method would arise for the SiC NWs fabricated from Si NW conversion. Implantation is a convenient method for doping SiC NWs after their growth. Therefore we have been involved in this research with the aim to transfer the method to SiC NWs. Indeed, the electrical characterization of the 3C-SiC NWFET revealed that the control of nanowire doping is a very critical issue for the transistor performance. One route to control doping in nanowires is the chemical in-situ doping during the growth. The difficulty with this technique is to provide accurately the dopants in specific places, for example only in the channel or S/D regions. An alternative technique is the usage of ion implantation to dope nanowires either to form S/D regions or the channel region. Our effort was to simulate the fabrication process and the RTA annealing step and moreover fit the experimental I-V characteristics. Through this simulation, we estimated the suitable RTA conditions for the activation of the dopands, and moreover we explained the various shapes of the observed I-V characteristics. In addition, we could cross-check our Silvaco simulation with another more established technology like that of Si NWs.

At present, nanowire-based electronic devices are fabricated using semiconductor nanowires assembled onto contact platforms for field-effect transistors (FETs) [4.19- 4.21]. Previous studies demonstrated that p-n junction diodes were formed by the assembly of crossed nanowires with n- and p-type NWs even though these devices had a large leakage problem due to inefficient junction contacts between two assembled NWs [4.22- 4.25]. This problem can be potentially solved by the fabrication of in situ doped superlattice structures and sequentially dope linear p-n junction NWs [4.26, 4.27]. Gudiksen et al. demonstrated the superlattice structure of GaAs/GaP and in situ doped p-n junction structures (n-Si/p-Si and n-InP/p-InP) designed to minimize the interface junction problem [4.26]. Furthermore, the performance of the nanowire-based devices is limited by the lack of doping control of semiconductor NWs since the doping is the key process for controlling the conductivity and mobility of semiconductor crystals. In addition, the doped nanowires with a certain doping concentration (e.g. $>10^{15}$ cm^{-3}) are also required for the nanoscale sensor applications with two-terminal contacts as well as the nanowire-based devices such as Schottky diode, p-n junction diode, and bipolar junction transistors (BJT), etc. Previous studies have shown

that the doping of the Si NWs and other semiconductor NWs was only achieved by in situ doping during NW growth. However, it was difficult to provide the dopants into the selective area in semiconductor NWs from the in situ chemical doping. Ion implantation of the selective area in semiconductor NWs represents an interesting approach to address the above problems. Recently, Hayden et al. studied ion implantation to fabricate the source and drain in Si NW FETs [4.28]. A lateral n-channel MOSFET with normally-off enhanced mode device performance was successfully fabricated. Similarly, Cohen et al. also fabricated a Si NW FET with epitaxial doped source and drain contacts using selective area ion implantation [4.29]. Nevertheless, most previous works on ion implantation of the semiconductor NWs have not revealed enough information such as the effects on activation annealing and the dopant controllability for channel-doping purpose. In addition, there has been no systematic study on electrical characteristics of implanted Si NW FETs.

In conclusion, this last section reports on the fabrication and electrical characteristics of p-type Si NW FET prepared using boron (B) ion implantation. The ion implantation was performed on randomly dispersed intrinsic Si NWs with a dose of 1×10^{12} -1×10^{13} ions/cm^2 and energy of 10 keV. The influence of activation annealing on the electric characteristics of B-implanted Si NW FETs is also discussed. To support the electrical characterization and the effects on activation annealing of B-implanted Si NW FETs, a numerical simulation study was carried out. The Silvaco (2D-ATHENA and ATLAS) software was used to accurately simulate the device fabrication process and the electrical performance, respectively [4.2]. The aim was to build up a Si NW p-FET with an optimized ion implantation process for doping the channel and not only the source and drain contacts compared to previous studies.

Experimental details

Figures 4.19a-e show schematic diagrams of the fabrication processes (steps (a-e)) for the B-implanted Si NW FETs. Post-implantation annealing was performed at a temperature of 950°C for 30 and 60 seconds by rapid thermal annealing (RTA). Source and drain contacts (Ti/Au=50/150 nm) were defined by conventional electron-beam lithography and a lift-off process (figures 4.19d-e) after etching the native oxide by dipping in diluted hydrofluoric (HF) acid. To get low resistivity ohmic contacts to the Si NWs, the B-implanted Si NW FETs were annealed again at a temperature of 400 ^{o}C in a N_2 environment prior to the electric transport measurement.

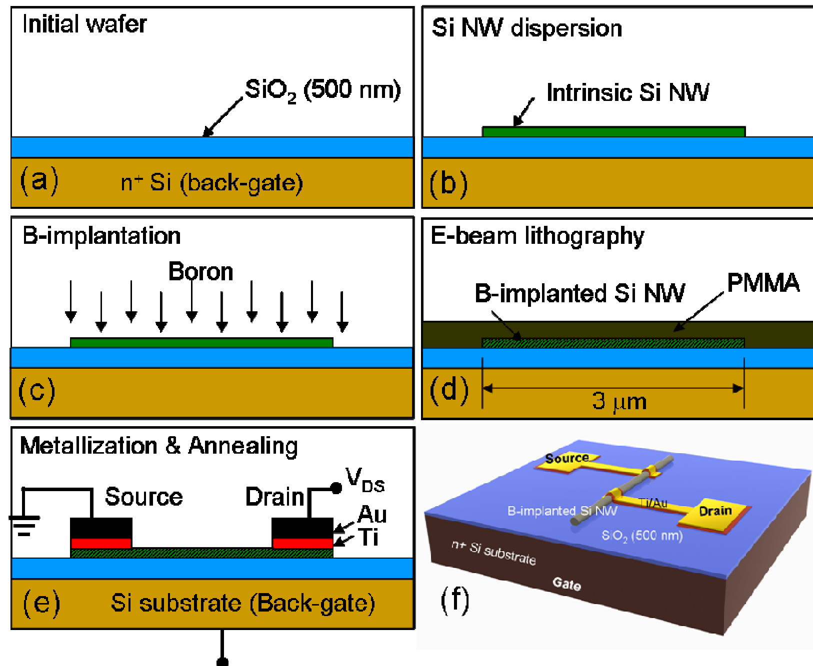

Figure 4. 19 Schematic diagrams showing the cross-sectional view of the fabrication processes (step (a-e)) for the B-implanted Si NW FET with three-probe scheme. (a) Thermal oxidation of the initial Si wafer, (b) Si NW dispersion on a Si wafer, (c) ion-implantation with B-ions and activation annealing at 950°C for 30-60 seconds, (d) conventional e-beam lithography, (e) S/D metallization and lift-off, (f) a schematic of the B-implanted Si NW FET.

Figure 4.20a shows the simulated B-dopant depth profile, which is generated by a SRIM simulation, for implanted B in Si NWs with a dose of 1 x 10^{13} ions/cm^2 and an energy of 10 keV [4.39].

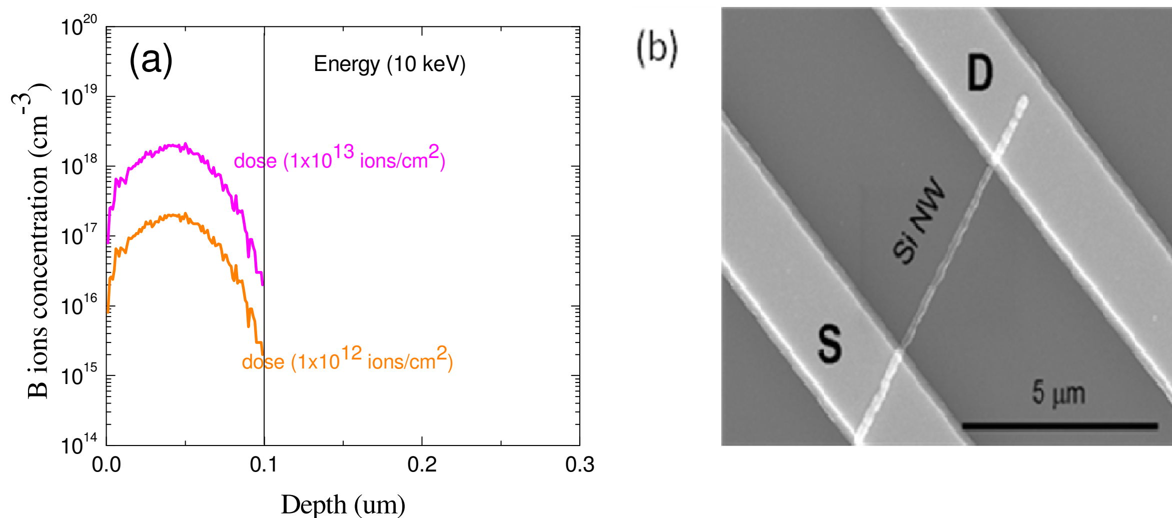

Figure 4.20 (a) Simulated depth profile of B ions in the Si nanowire. The dose and energy for ion implantation were 1×10^{13} ions/cm^2 and 10 keV, respectively, (b) a field-emission scanning electron microscope (FE-SEM) images of B-implanted Si NW FET.

Results and discussion

As shown in figure 4.20a, the SRIM simulation suggested that the implantation corresponded to a depth of ~100 nm, which was the same as the size of the Si NW that was utilized for the ion implantation, and a hole carrier concentration of $>2\times10^{18}$ cm^{-3} near the surface of Si NW. Figure 4.20b shows the FE-SEM image of the B-implanted Si NW p-FET. First of all, we present the electrical characteristics of B-implanted Si NW FETs after activation annealing at 950°C for 30 seconds (figure 4.21a) compared with the results of Si NW FETs annealed for 60 seconds (figure 4.21b) at the same temperature. The insets of figures 4.21a-b show the drain current versus the gate voltage (I_D-V_G) characteristics of Si NW p-FET annealing at a temperature of 950°C for 30 seconds and 60 seconds at different V_{DS}, respectively. A FET channel modulation was achieved by applying a bias to the Si substrate that was used as a large-area gate in the FET structure as shown in figure 4.19f. Moreover, the fabricated Si NW FETs show clear p-type semiconductor behaviour from the gate transport characteristics in all cases.

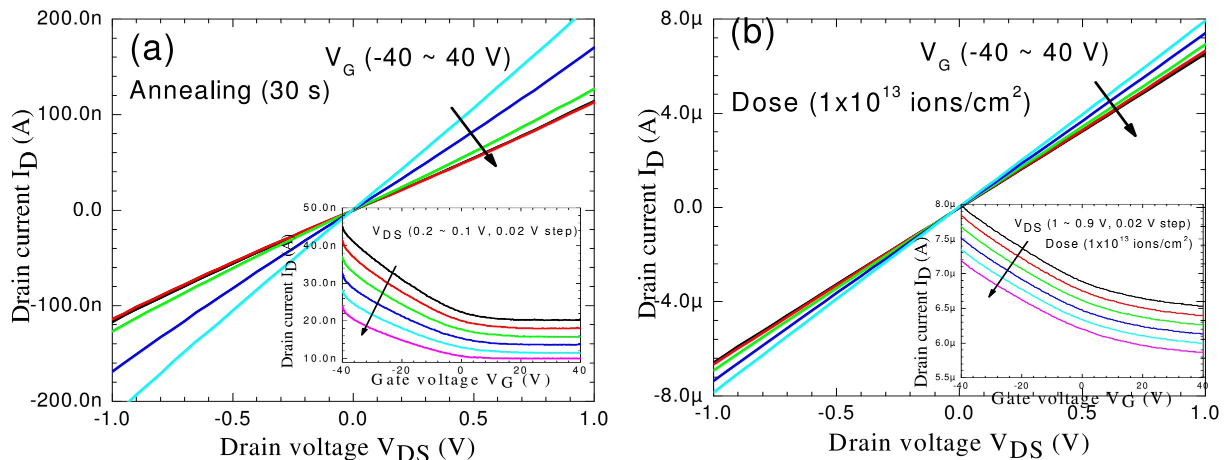

Figure 4.21 (a) I_D-V_{DS} characteristics curves as a function of V_G (-40, -20, 0, 20, and 40 V) for B-implanted Si NW FET annealed at 950 ^{o}C for 30 seconds. Inset of (a) shows the I_D-V_G curves as a function of V_{DS}, (b) I_D-V_{DS} curves at different V_G (-40, -20, 0, 20, and 40 V) for B-implanted Si NW FET annealed at 950°C for 60 seconds. Inset of (b) shows the I_D-V_G curves as a function of V_{DS}. All samples were prepared by ion implantation with a dose of 1×10^{13} ions/cm^2 and 10 keV.

As is shown in figures 4.21a-b, the I-V characteristics also suggested that the Si NW FETs annealed for 30 seconds show peak transconductance (g_m) of 3.5 ± 1.2 nS (standard error of the mean) at a V_{DS} of 0.1-0.2 V and in the range of V_G= -40 to +40 V while Si NW FET annealed for 60 seconds have a relatively weak gate effects with a g_m of 2.9 ± 0.7 nS (V_{DS}=1V and V_G=-40 to 40 V). Assuming the channel width equals to the diameter of the nanowire (~100 nm), the normalized transconductance for the Si NW FETs annealed for 30 seconds and 60 seconds were estimated to be

~35 nS/μm and ~29 nS/μm, respectively. These values are significantly lower than the state-of-the-art MOSFET devices (~0.6 mS/μm). It can be understandable in FET devices with relatively high hole concentration in the channel. Moreover, the Si NW p-FETs annealed for 30 – 60 seconds have an extremely low I_{ON}/I_{OFF} ratio of ~1.2 – 2.5 owing to the high hole concentration as expected by the SRIM simulation. The detailed information from the electrical measurements of B-implanted Si NW p-FETs is summarized in table 4.2.

The estimated hole carrier density and the field-effect carrier mobility of B-implanted Si NW FETs annealed for 30 seconds with a dose of 1×10^{13} ions/cm^2 were determined to be ~$6.3 \times 10^{17} \pm 3.4 \times 10^{17}$ cm^{-3} and ~ 11.8 ± 10.3 cm^2/V·s, respectively (see table 4.2). The estimated hole concentration for Si NW FET (annealed 30 seconds) is lower than the values expected by the SRIM simulation as shown in figure 4.20a. We could expect that the duration of activation annealing is not enough to completely activate the implanted B-ions in Si NWs. Thus, it is important to explore the effects of the activation annealing. To this end, we have carried out the activation annealing studies on Si NW p-FETs performance with different annealing time from 30 to 60 seconds. To illustrate the distribution and repeatability on FET device performance, we fabricated two sets of samples (7 samples in total, See table 4.2). Figures 4.22a-b show the distribution of the hole mobility and hole carrier concentration of the B-implanted Si NWs FETs annealed for 30 seconds and 60 seconds. The p and μ changed to ~$1.1 \times 10^{19} \pm 1.0 \times 10^{18}$ cm^{-3} and ~6.9 ± 2.7 cm^2/V·s, respectively after increasing the annealing time from 30 to 60 seconds (see table 1 for more detailed information of the calculation). The SRIM simulation suggested that the hole carrier concentration (p) of the Si NWs with a dose of 1×10^{13} ions/cm^2 corresponded to ~2×10^{18} cm^{-3} at the Si NW surface. It is worth noting that our experimental results on the hole concentration were slightly higher than the values expected by the SRIM simulation. Additional studies are required to further understand this phenomenon.

Table 4.2 Detailed electrical information from the calculations for B-implanted Si NW FETs.

Dose (ions/cm^2)	Samples[1]	Channel Length (μm)	Capacitance C (F)	Transconductance		Hole mobility μ (cm^2/Vs)	Hole concentration p (cm^{-3})
				g_m (nS)	V_{DS} (V)		
1×10^{13}	A1	5.3	3.8×10^{-16}	4.8	0.2	18	1.2×10^{18}
	A2	6.3	4.6×10^{-16}	2.6	0.1	23	5.2×10^{17}
	A3	7.0	5.1×10^{-16}	4.9	3	1.6	2.9×10^{17}
	A4	2.2	1.6×10^{-16}	3.1	0.2	4.6	4.9×10^{17}
	B1	1.1	8.0×10^{-17}	3.2	1	4.9	1.1×10^{19}
	B2	2.2	1.6×10^{-16}	3.3	1	10	1.2×10^{19}
	B3	2.0	1.5×10^{-16}	2.1	1	5.7	1.0×10^{19}

[1] Samples A1, A2, A3, and A4 were annealed at 950°C for 30 seconds.
[1] Samples B1, B2, and B3 were annealed at 950°C for 60 seconds.

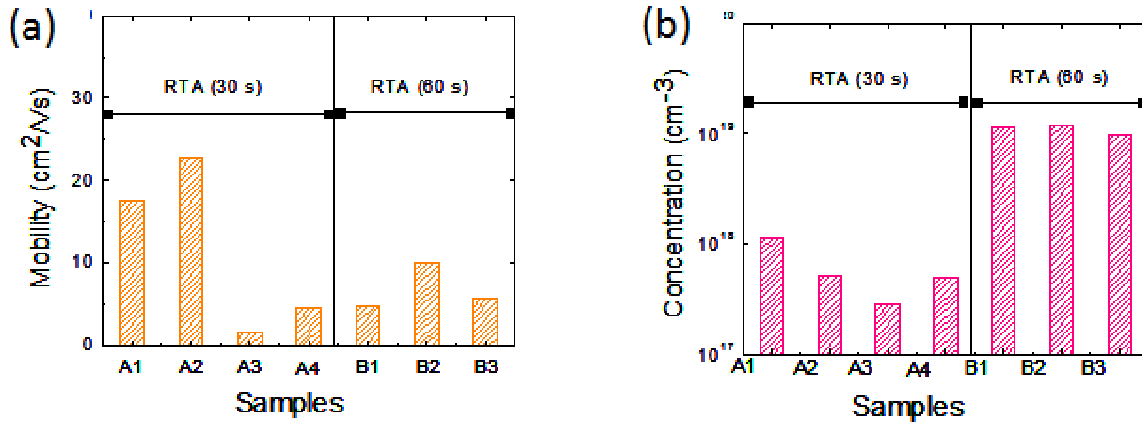

Figure 4.22 The distribution of the estimated hole mobility (a) and hole carrier concentration (b) of B-implanted Si NW FETs annealed at 950°C for 30 and 60 seconds (samples A and B series).

To further support the previous conclusion on the activation of the hole carriers in the Si NWs, a 2D numerical simulation was carried out using the commercial ATHENA simulator (SILVACO Inc.). Figure 4.23 a-b show the simulated hole concentration profile (~ 2 x 10^{18} cm^{-3}) of the hole carriers along the nanowire for various annealing times (30 and 60 seconds). The figure shows that the sample annealed at a temperature of 950°C for 30 seconds has a small peak of concentration at the middle of the nanowire. After 30 seconds more annealing, the profile is more uniform along the nanowire. These results confirms our experimental results, indicating 60 seconds RTA are enough for the dopants activation in Si NWs. Apart from the exploration of the carrier concentration dependence on annealing time, we proceed to the device electrical behaviour simulation using ATLAS simulator. Recently, Hang et al. showed that ATLAS simulator is able to produce a rough estimation of the nanowire/interface quality (estimation of fixed charge density (Q_f) and interface trap density (D_{it}) values) and carriers mobility value by correctly fitting the experimental with simulated I-Vs. Figure 4.23c shows the simulated I_D-V_D and I_D-V_G characteristics of the B-implanted Si NW FETs with a dose of 1×10^{13} ions/cm^2. In the simulation, a diameter of 100 nm and a channel length of 2 μm were used for the calculations. An excellent agreement between experiment and simulation is obtained for a) maximum body hole mobility and surface mobility equal to ~ 400 cm^2/Vs and ~ 22 cm^2/Vs respectively, b) density of fixed charge Q_f ~3×10^{10} cm^{-2} and, c) density of interface trap D_{it} ~3×10^{11} eV^{-1} cm^{-2}. According to the above mobility parameters, ATLAS calculates a total mobility value equal to ~60 cm^2/Vs. The parameters maximum body hole mobility and surface mobility are specific to the model of mobility in MOSFETs used by SILVACO. In our case, these values are lower than the corresponding ones used for fitting bulk silicon MOSFETs. The lack of bibliography data for the mobility value in Si based

NW FETs does not allow us, for the time being, to attribute this reduction to a physical effect like increased surface to volume ration, increase surface roughness, high interface traps etc.

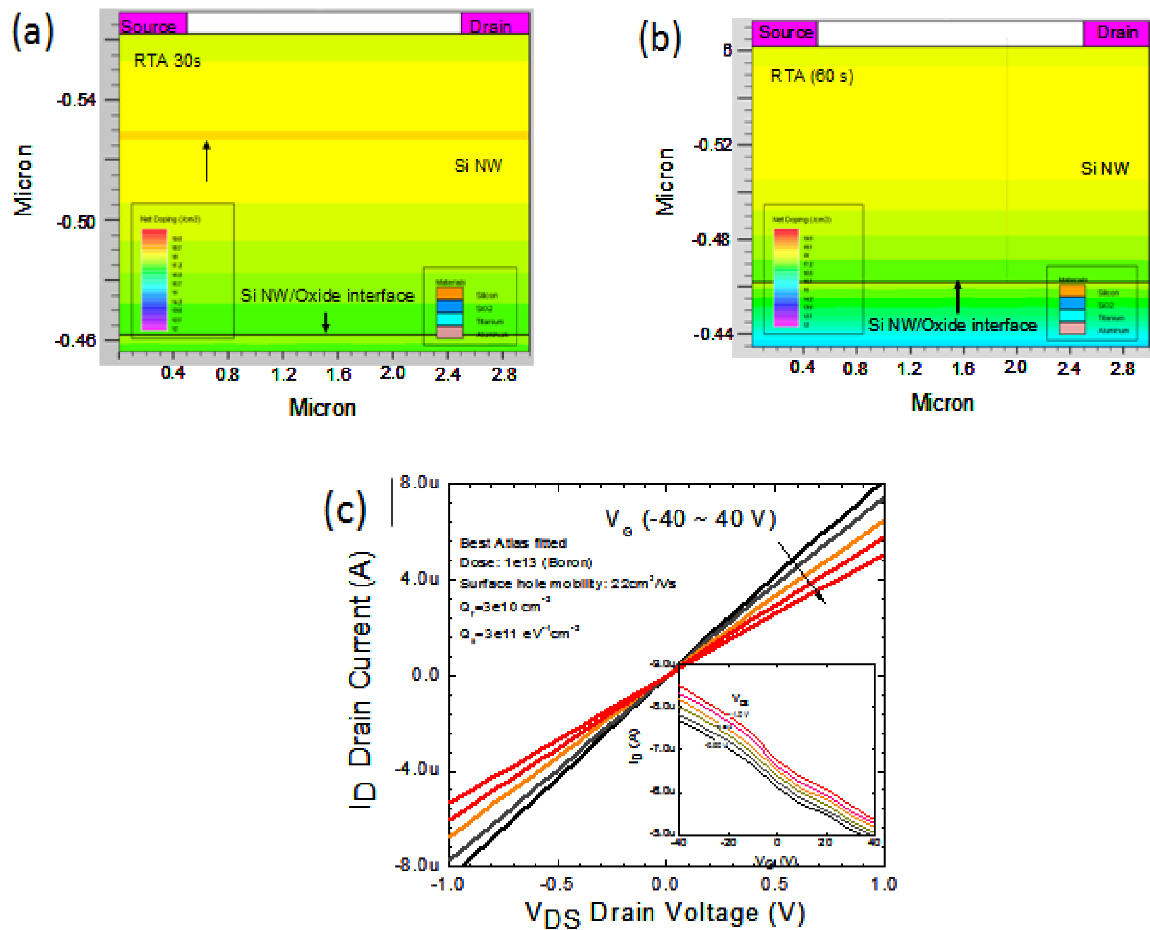

Figure 4.23 The simulated hole concentration profile along nanowires for B-implanted Si NWs annealed at a temperature of 950°C for (a) 30 seconds and (b) 60 seconds, (c) the simulated I_D-V_{DS} characteristics curve as a function of V_G of -40, -20, -10, 0, 20, 10 and 40 V for B-implanted Si NW p-FET. Inset of (c) shows the simulated I_D-V_G curves of B-implanted Si NW FETs at the different V_{DS} (-0.9 – -1.0 V).

Effect of Schottky barriers at source and drain regions

Apart from the previous devices, we prepared implanted Si NWFET with implantation dose of $1x10^{12}$ ions/cm^2 and energy of 10 keV [4.10]. In this case, our results indicated that the nature of the metal-contacts on the source/drain electrodes had a significant impact on the I-V characteristics for B-implanted Si NW FETs. Devices with both linear symmetric and non-linear asymmetric I-V characteristics were reported. The output characteristics for the B-implanted Si NW FETs with a

symmetric I-V behaviour exhibited a clear p-channel FET behaviour with a field-effect mobility of ~0.4 cm^2/Vs and a hole concentration of ~1.7 x 10^{17} cm^{-3}. Again, a 2D ATLAS simulation (SILVACO Inc.) with two different Schottky barrier heights of source/drain contacts to the Si NW well supported the experimental results.

Figure 4.24a and b show the output and transfer characteristics for the boron (B) implanted p-Si NW FET with ohmic source/drain contacts. The inset of figure 4.24a shows a field-emission scanning electron microscopy (FESEM) image of a typical B-implanted p-Si NW FET. The figures suggest that these B-implanted Si NW FETs showed a well-defined gate effect indicative of a p-type semiconductor. Gate transfer characteristics, as shown in figure 4.24b, exhibit an on/off current ratio (I_{ON}/I_{OFF}) of ~10^3 at V_{DS} of -0.1 V and at a V_G from -40 to 40 V. The low value of the I_{ON}/I_{OFF} in the B-implanted Si NW FETs compared to the previous reports in Si NW FETs could be explained by the scattering effect in Si NWs resulting from the incompletely activated B-ions, which could block the carrier flowing from the source to the drain in a FET. Additional studies with dependence of the activation of the carriers on the FET characteristics are required for further understanding this phenomenon.

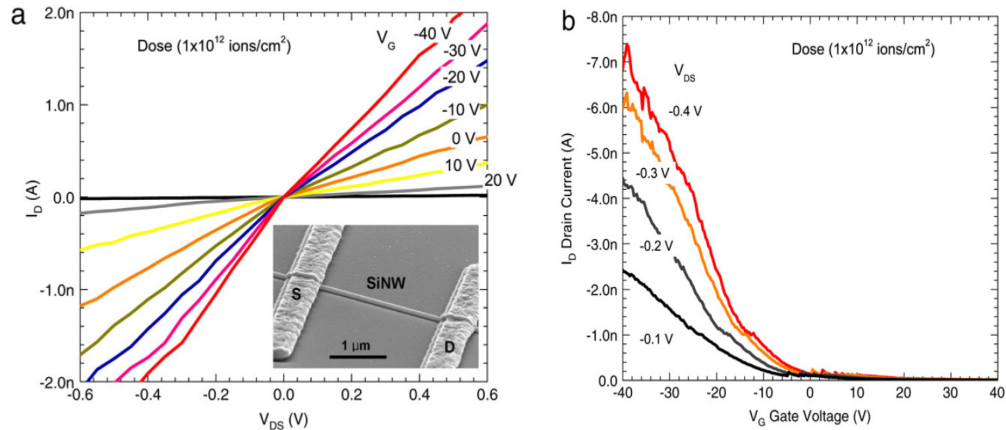

Figure 4.24 (a) Output characteristics at different V_G (-40, -30, -20, -10, 0, 10, and 20 V) for the B-implanted Si NW FETs with a dose of 1 x10^{12} cm^{-2}. (b) Transfer characteristics at different V_{DS} (-0.4, -0.3, -0.2, and -0.1 V). The inset shows a field-emission scanning electron microscopy (FE-SEM) image of a B-implanted p- Si NW FET. All measurements are performed at room temperature.

The estimated hole carrier density and the field-effect mobility for lightly B-implanted SiNW FETs were ~0.4 cm^2/Vs and a hole concentration of ~1.7 x 10^{17} cm^{-3}, respectively. The estimated hole carrier concentration corresponds well with the values expected by SRIM simulation [4.30]. We also found large variations in the output characteristics of lightly B-implanted SiNW FETs. For instance, asymmetric I_D-V_D characteristics of B-implanted SiNW FET devices, which

were prepared in the same batch, are shown in figure 4.25a and inset of figure 4.25a. The figures indicate that the I_D-V_{DS} curve at V_G=0 shows a clear rectifying behaviour with a clear indication of p-type semiconductor as seen in standard Schottky diodes. We found that the I_{ON}/I_{OFF} and carrier concentration are ~10^3 and 2.3×10^{16} cm^{-3}, respectively from the transfer characteristic of the inset of figure 4.25a. These asymmetric output characteristics could result from the different Schottky barrier heights (SBHs) of the source/drain contacts. Similar rectifying behaviours in FET and Schottky diodes were reported in ZnO nanobelt/nanowire-based FETs and Schottky diodes [4.31, 4.32]. We observed that some of the Si NW FETs have severe surface-morphology changes (i.e. size depression and partial melting etc.) after 950 ^{o}C activation annealing process as shown in figure 4.25b. These could be caused by the high surface energy and area of the nanoscale Si NW since it is well documented that the melting point of a solid material will be greatly reduced when it is processed as nanostructures [4.33].

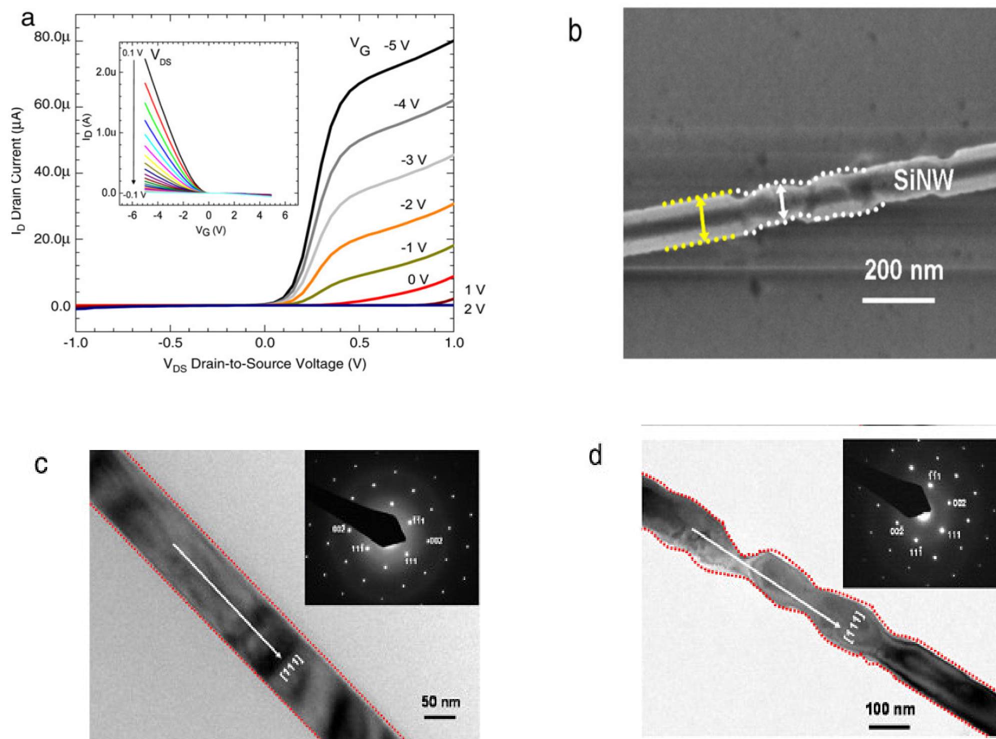

Figure 4.25 (a) Output characteristics at different V_G (-5, -4, -3, -2, -1, 0, 1 and 2 V) for a B-implanted SiNW FET. The inset shows a plot of I_D-V_G curves at different V_D (0.1 to -0.1 V), (b) FE-SEM image of a B-implanted SiNW FET after high-temperature activation annealing (950 ^{o}C, 60 s), (c) TEM image of as-implanted SiNW, (d) TEM image of SiNW after high-temperature activation annealing process. The insets of (c) and (d) show the selective area electron diffraction (SAED) patterns.

Furthermore, to study the structural characterization of the B-implanted Si NWs before and after 950 ^{o} C activation annealing, TEM measurements were performed. Figure 4.25c and d show TEM images of the B-implanted Si NWs before and after activation annealing with selective area electron diffraction (SAED) patterns. As shown in figure 4.25c and d, both Si NWs were highly crystalline in nature with a preferred orientation in the [111] direction without any defect and structural changes after high-temperature activation annealing process although the surface-morphology of the Si NW after activation annealing process was much rougher than as-implanted Si NWs. We suggest that the different Schottky barriers form on the surface of Si NWs because of non-uniform surface of Si NWs as shown in figure 4.25b and d. Moreover, to further explain the asymmetrical behaviours of output characteristics with a different Schottky barrier at the source/drain contacts of the B-implanted SiNW FET, we carried out a 2D numerical simulation using commercial Silvaco Inc. Figure 4.26 shows the simulated I_D-V_D characteristics of the B-implanted Si NW FETs with different SBHs (SBHs~ 0.3 eV and ~0.15 eV for the source and drain contacts, respectively). In the simulation, the hole carrier concentration of ~2.3x10^{16} cm^{-3}, which was extracted from the I_D-V_G of the B-implanted Si NW FET shown in the inset of figure 4.24a, was used. As is shown in figure 4.26, the output characteristics highly depend on the Schottky barrier height on source/drain contacts in the Si NW FET. We have to note that there is a big difference between the simulated and experimental drain current if we compare their absolute values. In order to lift this discrepancy, we could increase the mobility value used in Silvaco, which would lead to increased drain current. This would be unphysical, at least to the time being, where we cannot explain in a physical manner the huge current of the experimental B-implanted SiNWFETs. Despite this point, Silvaco succeeded in reproducing this strongly asymmetric I-Vs shape by appropriate adjustment of contact SBs.

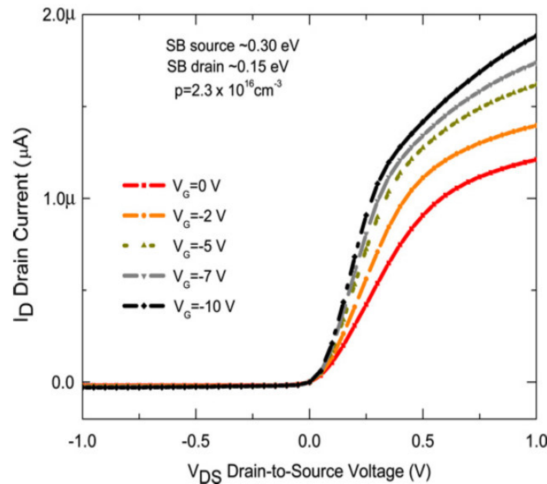

Figure 4.26 The simulated I_D-V_D characteristics curve as a function of V_G of 0, -2, -5, -7 and -10 V for a Si NW p-FET using the 2D ATLAS simulator.

Conclusions

The goal of this study was to simulate the electrical behaviour of our experimental 3C-SiC NWFET devices and by fitting the data to extract information about our transistors such as NW/dielectric interface quality, carrier mobility etc. We varied the dielectric material in order to study the effect of NW/dielectric interface quality to device performance. We used both silicon dioxide and silicon nitrate as dielectric material. As it was expected, devices with silicon dioxide presented better performance having a better interface in terms of fixed charges and interface traps density. Even in the case of oxide as the dielectric, the values for Q_{fix} and D_{it} are found to be increased in comparison with corresponding SiC/SiO_2 capacitors. This is due to the presence of a thin native oxide all around the nanowires, which is in contact with the thermally grown gate dielectric. A possible thermal oxidation of the nanowires, right after the HF treatment for the oxide layer removal (before preparing the solution of the NWs), might lead to dielectric with higher quality. In any case, the highly unintentional doping is more critical than the oxide quality for the device performance. We showed that at lower doping levels and assuming ideal perfect nanowire/dielectric interface, the device performance is significantly increased.

We have successfully fabricated p-type Si NW FETs using B-ion implantation with a dose of 1×10^{12} ions/cm^2 and 1×10^{13} ions/cm^2 and energy of 10 keV. For the case of the heavily implanted nanowires, the experimental linear I_D-V_D characteristics for B-implanted Si NW FETs after 950° C annealing for 60 seconds exhibited clear p-channel FET behaviour with hole mobility of ~ 6.9 cm^2/Vs, a hole concentration of ~1.1 $\times 10^{19}$ cm^{-3}, and a transconductance of ~29 nS/μm at a V_D of 0.1V. For the case of lightly implanted nanowires, our results indicated that the FET I-V characteristics were strongly dependant on the Schottky barrier height of the source/drain contacts. The experimental I-V characteristics of B-implanted Si NW FET corresponded well with the numerical simulation results (2D ATHENA and ATLAS simulation) and a roughly estimation of NW/oxide interface quality was presented. A study on the optimized implantation process in Si NW FETs is being initiated for fully depleted and high I_{ON}/I_{OFF} ratio FETs for the high performance bipolar device applications. The results reported here should have significant implication in fabricating and designing highly efficient future nanoscale devices such as Junction FET (JFET), BJT, and p-n junction diodes.

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5. Chapter five: Conclusions and prospective for future work

A combination of experiments and simulation were presented relative to the study of 3C-SiC nanowire transistors. In the purely theoretical part, we presented a theoretical comparison between Si and 3C-SiC GAA nanowire-based FETs operating both in ballistic and non-coherent transport regimes using a Poisson-Schrödinger self consistent simulation scheme within NEGF formalism. Our results revealed that Si and 3C-SiC NW FETs have comparable electrical behaviour in ballistic regime. They have the same subthreshold slope (69.4 mV/dec for SiC and 69.8 mV/dec for Si devices for 3 nm NW cross section size) and almost comparable on-current [I_{ON}/I_{OFF} (SiC) ~83 % I_{ON}/I_{OFF} (Si) for 4 nm NW cross section size]. The ballistic or apparent mobility of 3C-SiC devices is about 90 % of Si ones which is a direct result of the transverse effective mass difference of the two semiconductors.

The picture is quite similar when phonon scattering processes are included in the simulation since their relative comparison reveals an extra degradation for 3C-SiC mobility as a consequence of a larger acoustic deformation potential. A smaller difference for surface roughness (SR)-limited mobility was found for equivalent parameters of spatial fluctuations. Moreover, for 3C-SiC slower mobility degradation was observed for increasing gate voltage, revealing that the performance gap between Si and 3C-SiC devices is reduced in the operation regime (higher gate voltages). Analysis of the backscattering coefficient versus carrier density was derived based on mobility extraction. The decrease of the effective mobility as a function of electron density originates from the carrier degeneracy and both phonon and surface-roughness scattering result in an increase of the backscattering coefficient at large gate overdrive. A larger amount of backscattered electrons was found for 3C-SiC devices compared to Si ones, mainly due to the different acoustic deformation potential of the two materials.

From the aforementioned simulation results, we conclude that 3C-SiC NWs except the standard advantages compared to silicon ones such as the higher thermal conductivity, wider band gap, higher breakdown electric field, higher electron drift velocity and better chemical and physical stability, appears to be also competitive in terms of electrical transport properties and could be an excellent candidate for future high temperature nanoelectronics. This theoretical prediction allowed us to proceed to the fabrication of the experimental SiCNWFET.

In the experimental part, we fabricated and electrically characterized back gated FETs based on 3C-SiC nanowires. Two different types of nanowires were incorporated, nanowires grown with and without catalyst assistance. Electrical characterization did not reveal different behaviour

between devices with different type of nanowires. This is in agreement with the structural characterization of the differently grown nanowires. Both types of nanowires contain many stacking faults and defects and are probably nitrogen contaminated during the growth which results to an unintentional doping of 10^{19} cm^{-3}. The high carrier concentration is the main drawback of the material. In order to resolve this issue, we followed an alternative grown technique. We grew pure, undoped, high crystalline Si nanowires, and then by exposing them in carbon source e.g. methane, we converted them to 3C-SiC nanowires. The experimental set-up was designed and the results of the first experiments were presented. EDS and Raman analysis confirmed the SiC formation but the lower quality of these nanowires compared to the nanowires from our Korean and French collaborators prevented us from using them in FET applications. Optimization of the growth process should be firstly accomplished.

By using nanowires grown with and without catalyst, devices with both ideal ohmic and Schottky barrier (SB) contacts were observed leading to two different device operation modes. Devices with ohmic contacts manifest very weak gating effect and a switch-off is not achievable even for high negative gate voltages. In contrast, the small SB at Source (S)/ Drain (D) regions acts beneficially for the device performance by suppressing the off-current. At higher positive gate voltages, the Schottky barriers are extremely transparent leading to high transconductance and I_{ON}/I_{OFF} ratio, 3.88 nS and $2.81 \cdot 10^3$, respectively. In the case of highly unintentionally doped nanowires, where the direct effect of the gate voltage on the accumulation carrier density is negligibly, SB-NWFET presents improved performance by suppressing the off current and indirectly modulating the drain current by adjusting the transparence at source and drain regions.

The fitting of the experimental results was accomplished with the assistance of the commercial simulation software Silvaco. The goal of this study was to simulate the electrical behaviour of our experimental 3C-SiC NWFET devices and by fitting the data to extract information about our transistors such as NW/dielectric interface quality, carrier mobility etc. Even in the case of silicon dioxide as the dielectric material (the other choice was silicon nitrate) the values for Q_{fix} and D_{it} were found to be increased in comparison with corresponding bulk SiC/SiO_2 interface. This is due to the presence of a thin native oxide all around the nanowires, which is in contact with the thermally grown gate dielectric. A possible thermal oxidation of the nanowires, right after the HF treatment for the oxide layer removal (see experimental methods of chapter 4), might lead to interface with higher quality. In any case, the highly unintentional doping is more critical than the oxide quality for the device performance. Silvaco simulations showed that at lower doping levels and assuming ideal perfect nanowire/dielectric interface, the device performance is significantly increased.

For cross checking our Silvaco-based fitting of experimental results, we also investigated the application of Silvaco simulation tool in Si nanowire FETs. More particularly, experimental FETs based on Boron-implanted Si nanowires were prepared. We successfully fabricated p-type Si NW FETs prepared using B-ion implantation with a dose of 1×10^{12} ions/cm^2 and 1×10^{13} ions/cm^2 and energy of 10 keV. For the case of the heavily implanted nanowires, the experimental I_D-V_{DS} characteristics for B-implanted Si NW FETs after 950° C annealing for 60 seconds exhibited clear p-channel FET behaviour with hole mobility of ~6.9 cm^2/Vs, a hole concentration of ~1.1×10^{19} cm^{-3}, and a transconductance of ~29 nS/μm at a V_{DS} of 0.1V. For the case of lightly implanted nanowires, our results indicated that the FET characteristics were strongly dependant on the Schottky barrier height of the source/drain contacts. The experimental current-voltage characteristics of B-implanted Si nanowire FET were fitted with Silvaco and a rough estimation of NW/oxide interface quality was presented. This process seemed appropriate for our study since a problem of doping method would arise for the SiC NWs fabricated from Si NW conversion (implantation would be a useful technique to control the doping). In addition, these experiments on Si NWs incited us to investigate our SB SiC NWFETs, which as exposed in the manuscript, presented better electrical characteristics compared to ohmic contact devices.

In conclusion, two main parameters hinder the 3C-SiC nanowire transistors performance. The first is the nanowire/dielectric interface quality and the second is the high unintentional doping of the nanowires. Although, a controlled dry oxidation and HF treatment for oxide removal might be an easy way to overcome the issue with the nanowire/dielectric interface, the control of the carrier concentration along the nanowire is more complicated. The growth of the nanowires should be carried out in a strictly controllable atmosphere; otherwise, the nitrogen presense will contaminate 3C-SiC. When nanowires with controllable carrier concentration (suppression of unintentional doping) will be grown, more advanced nanowire FET geometries like double gated or GAA will lead to better electrical performance. As far as concerns the theoretical part, new comparative simulations between Si and SiC could be realized this time not at room temperature but at higher ones where SiC is expected to have superior performance compared to Si (wider band gap). In the present version of the code, the temperature is included in the Fermi distribution and in the scattering rates for the phonons. No dependence of Eg and effective mass on temperature is included, which should play an important role at high temperature, when comparing Si and SiC. Another effect important at higher temperature could be the self-heating, which is not also included in the present version of the code (a further self-consistent cycle with the heat equation is required to capture this effect).