

Study of nano-rectifiers based on carbon nanotubes and fullerenes

**for the academic title
of
Master in Science**

By
Alexandros Provias

Supervisor: Dr Georgios Deligeorgis

Examination Committee: Dr Georgios Deligeorgis, Dr Alexandros Georgakilas, Dr
Eleftherios Iliopoulos

Table of Contents

Acknowledgments.....	3
Abstract.....	4
Acronyms.....	5
Chapter 1 – Theory.....	6
1.1 Nanomaterials.....	6
1.1.1 Carbon Nanotubes.....	6
1.1.2 Indene-C ₆₀ Bisadduct.....	8
1.2 Fabrication of Nanomaterials.....	9
1.2.1 Fabrication of Carbon Nanotubes.....	9
1.2.2 Fabrication of Indene-C ₆₀ Bisadduct.....	10
1.3 Carbon-based electronics.....	10
1.3.1 Conventional semiconductors limitations.....	10
1.3.2 Carbon materials potential.....	11
1.3.3 Carbon nanotubes and Indene-C ₆₀ Bisadduct interaction.....	11
1.4 Diode Theory.....	12
1.4.1 Ideal Diode.....	13
1.4.2 Non-ideal Diode.....	15
1.4.3 Extracting Diode Parameters.....	15
1.5 High Frequency Diodes.....	18
1.5.1 Capacitance Problem.....	18
1.5.2 Resistance Problem.....	19
Chapter 2 – Experimental Techniques.....	20
2.1 Device processing.....	20
2.1.1 Spin Coating.....	20
2.1.2 Electron Beam Evaporation.....	20
2.1.3 Lithography.....	21
2.2 Experimental Material Deposition.....	21
2.2.1 CNT films.....	21
2.2.2 ICBA & Pd/Pt/Au deposition.....	24
2.2.3 PTCK ₄ deposition.....	24
2.3 Characterization techniques.....	25
2.3.1 Transmission Line Modeling.....	25
2.3.2 Vector Network Analyzer.....	26
Chapter 3 – Results.....	28
3.1 Device Fabrication.....	28
3.2 TLM measurements.....	31
3.2.1 First case: CNTs only.....	32
3.2.2 Second case: CNTs/ICBA.....	33
3.2.3 Third case: CNTs/ICBA/PTCK ₄	35
3.2.4 Fourth case: CNTs/PTCK ₄	37
3.2.5 Contact & Sheet Resistances.....	38
3.3 Diode I-V measurements.....	39
3.4 High Frequency measurements.....	40
3.5 Conclusions.....	42
Bibliography.....	43

Acknowledgments

This thesis would not have been possible without the constant and precious help of some people. Throughout this one-year journey I gained much more than knowledge. I learned that making mistakes, most of the time, proves to be beneficial for realizing and overcoming something that was once an obstacle in this thesis and, in extend, in life as well.

First, I would like to express my gratitude to my supervisor Professor, *Dr Georgios Deligeorgis* that despite his excessive workload he managed to aid and support me whenever I felt the need for help and none of this would be possible without him. His enthusiasm and dedication for what he is doing is truly inspiring.

Furthermore, I would like to thank the committee members *Prof. Alexandros Georgakilas* and *Prof. Eleftherios Iliopoulos* for the time and energy they devoted to read my thesis and examine me in the presentation.

Last but not least, *Dimitris Kosmidis's* excellent work on the chemistry and materials aspect of this thesis is something to be grateful about. Moreover, I would like to thank *George Fanourakis* and *Alexia Papadopoulou* for the constant advice and help they were providing me when things were not going as I was expecting.

Abstract

Nanomaterials offer new possibilities to extend functionality of electronics towards higher frequencies due to their drastically reduced capacitance, a property that stems from their reduced dimensionality and corresponding density of states. In this work we demonstrate a rectifying structure based on two type of nanomaterials namely a fullerene derivative Indene- C_{60} Bisadduct (ICBA) and semiconducting single-wall carbon nanotubes (SWCNTs). The fabrication approach and preliminary characterization will be presented showing rectification properties. Key electrical parameters of the device can be extracted such as the Schottky barrier, the ideality factor and the series resistance by using the current voltage measurements performed.

Acronyms

AC	Alternating Current
CNT	Carbon Nanotube
CPW	Coplanar Waveguide
CVD	Chemical Vapor deposition
EBD	Energy Band Diagram
FET	Field Effect Transistor
HiPco	High Pressure Carbon Monoxide
HOMO	Highest Occupied Molecular Orbital
ICBA	Indene-C ₆₀ Bisadduct
ICMA	Indene-C ₆₀ Monoadduct
LED	Light Emitting Diode
LUMO	Lowest Unoccupied Molecular Orbital
MCE	Mixed Cellulose Ester
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCBB	[6,6]-phenyl-C ₆₁ -butyric acid benzyl ester
PC ₆₀ BM	[6,6]-phenyl-C ₆₁ -butyric acid methyl ester
PC ₇₀ BM	[6,6]-phenyl-C ₇₁ -butyric acid methyl ester
PCBO	[6,6]-phenyl-C ₆₁ -butyric acid octyl ester
PTCDA	Perylene-3,4,9,10-tetracarboxylic dianhydride
PTCK ₄	Perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt
PVD	Physical Vapor Deposition
RCF	Relative Centrifugal Force
SBH	Schottky Barrier Height
SDS	Sodium dodecyl sulfate
SEM	Scanning Electron Microscope
SWCNT	Single Walled Carbon Nanotube
TCBM	Thienyl-C ₆₁ -butyric acid methyl ester
TLM	Transmission Line Model
UV	Ultraviolet

Chapter 1 – Theory

1.1 Nanomaterials

Over the last 25 years, slowly but steadily, a revolution has happened regarding the materials that were being used for integrated circuits. The need for these materials arose from the fact that some researchers predicted that silicon based nanocircuits would soon face problems in scaling down. More specifically, in 1965 Moore's law is predicting an ever increasing number of transistors as we move on technologically [1] and some years later it became widely accepted that a limit was about to be reached with the solution being to use new types of materials. These materials are called nanomaterials. Nanomaterials is a class of materials that range in the nanoscale from 1 to 100 nm in at least one of the material's dimensions. Many nanomaterials are now well known and widely used in devices such as fullerenes and its derivatives (0D), carbon nanotubes (1D), graphene, silicene and hexagonal boron nitride (2D) [2]. In this study, a more detailed description will be given about CNTs and ICBA, a fullerene derivative, the materials that will be used for this study.

1.1.1 Carbon Nanotubes

In 1991, Sumio Iijima managed to do something that no one has ever achieved. He conducted an experiment that introduced the world to a material so strong that it could change the perspective of how engineers approached design. Using two electrodes made of graphite, Sumio applied a current across the rods. By approaching the two electrodes together, a spark arched between them and a cloud of carbon gas was created, vaporizing the anode rod tip. When the carbon gas settled on the walls of the chamber, a new material was born, tiny single walled carbon nanotubes, or as Sumio called them, helical microtubules of graphitic carbon [3]. Since then, a number of researchers have tried to take advantage of the special properties of this material by creating electrical devices like Schottky diodes [4], field effect transistors [5] and pn diodes [6].

It was easily understood by scientists how the atomic orbitals of the carbon work, but there was a significant obstacle regarding the carbon-carbon bonds. Carbon in its ground state has the 1s and 2s orbitals filled with electrons and the other two electrons go to 2p_x and 2p_y orbitals. This is simple to understand and it is expected if you know the basics of atomic orbital theory. What is not so profound is the way carbon bonds to itself and some other elements. Take as an example the diamond. Diamond is consisted of carbon atoms bonded with each other and what is special about that is that one of the two 2s electrons is moved up in energy and now occupies the 2p_z orbital. In that way, an imbalance is created in energies and thus in order to compensate, a hybrid orbital is created called sp³, which is a combination of s and p orbital shapes. This type of hybridization forms tetrahedral structures. But the peculiar properties of carbon nanotubes are not coming from sp³ hybridization but from sp². sp² hybridization once again occupies the p_z orbital but this time, only two of the p-orbitals are hybridized with the 2s orbital. This means that now we have 3 sp orbitals (1 s-orbital and 2 p-orbitals) and 1 p orbital, giving a new arrangement of the three sp orbitals shaping a 120° angle and the p orbital perpendicular to the sp orbitals, allowing the planar hexagonal graphene lattice to be formed.

Carbon nanotubes, are characterized by many as rolled up graphene, but it is important to understand that this is not the way the nanotubes are made. An analytical fabrication process is described in Section 1.2.1. The truth is that the CNT structure is comprised almost entirely by sp² hybridized carbon atoms but due to the curvature along its radius there is a small part of sp³ hybridization. This results in somewhat weaker force constants in the circumference than along the axis of the nanotube. The shape of the CNT results in a type of quantum confinement and because of this some properties emerge, different than its closely related material graphene [7].

Generally, there are several ways in which you can categorize carbon nanotubes such as chirality, number of nanotube walls, diameter and whether it is metallic or semiconducting. As a matter of fact, chirality and metallic/semiconducting properties are immediately related. More specifically, chirality can be determined using two integer numbers, (n,m) called chiral numbers. Let us take the crystal lattice of graphene as shown in Figure 1. Depending on the axis it is rolled as a CNT, we have a different chirality. For example, when we choose the axis $(n,0)$ as the axis along the tube, then we'll get the zigzag configuration, which is defined as angle $\theta=0^\circ$. Respectively, if $\theta=30^\circ$, then we get the armchair configuration. Of course, there is the case of $0^\circ < \theta < 30^\circ$ where it is just called chiral and is easily distinguishable by using the (n,m) indication and is described by the graphene lattice vector $C_h = a_1n + a_2m$ where a_1 and a_2 are unitary vectors. Because of the hexagonal symmetry, it is not necessary to talk about the case of $\theta > 30^\circ$ since the pattern repeats itself.

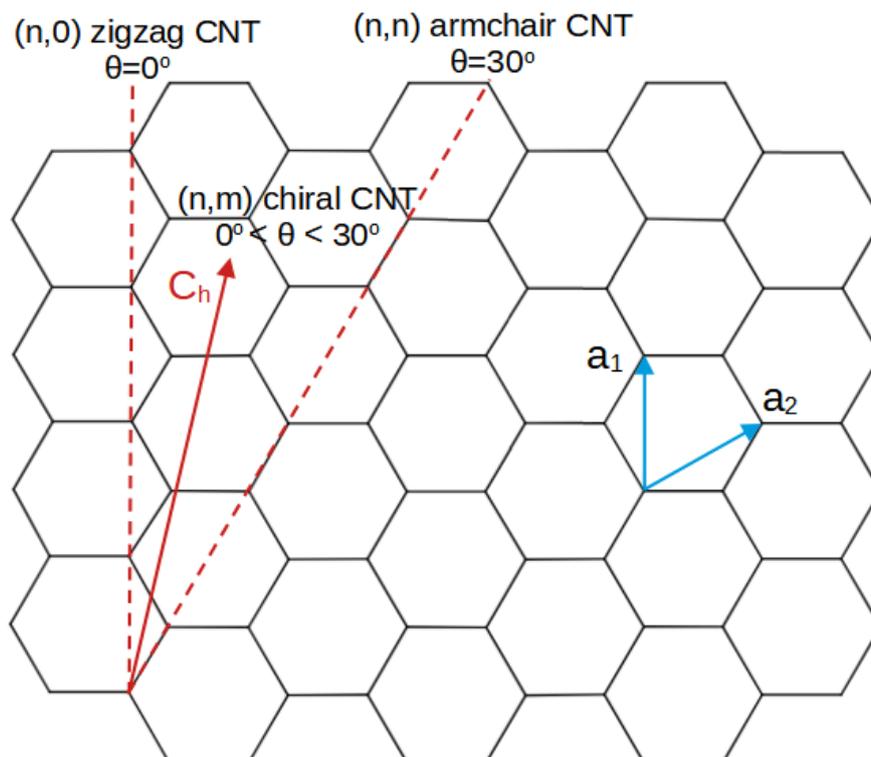


Figure 1: Chirality of CNTs based on the rolling of graphene sheet.

Depending on the (n,m) numbers, one can get semiconducting or metallic carbon nanotubes. More specifically, if $n=m$ or $n-m$ is divisible by 3, then the nanotube is metallic or quasi-metallic respectively. All the other cases of nanotubes are semiconducting [8]. Of course, there are some exceptions in each case when the radius of the tube is small enough, unless the nanotube is armchair type where it remains metallic [9].

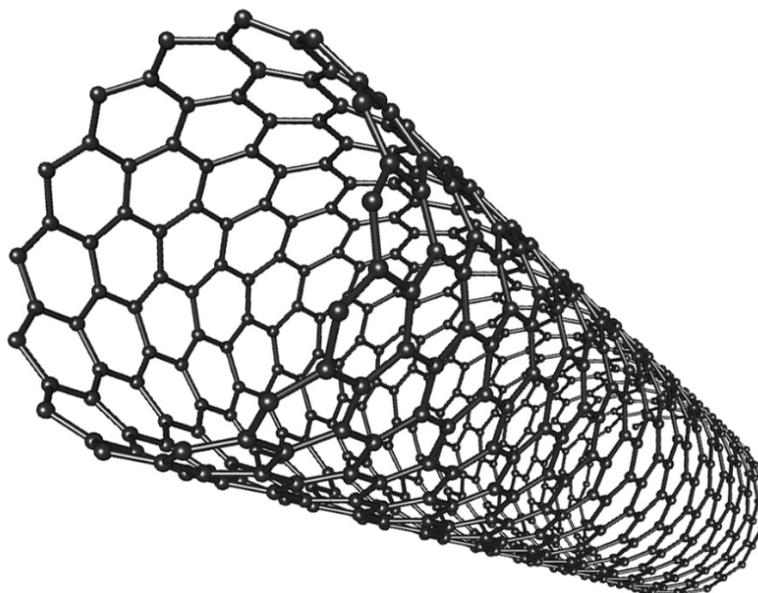


Figure 2: A single-walled carbon nanotube. [63]

Although carbon nanotubes are band-folded states of graphene, they exhibit some exceptional electronic properties. First of all, SWCNTs have a carrier mobility of $\sim 10,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ but due to the difficulty of depositing the nanotubes and integrating them in a device, sometimes the mobility is reduced to $\sim 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ because of the random orientation of the nanotubes. Moreover, an exceptionally high electrical current density is observed of $\sim 4 \times 10^9 \text{ A cm}^{-2}$ [10]. Besides electronic properties there is also interesting behavior of the nanotubes regarding the optical [11], the thermal [12] and the mechanical [13] properties. The carbon nanotube can be seen in Figure 2.

Last but not least, since our carbon nanotubes will be used in a diode it is necessary to clarify the doping type of the material. According to some researchers, CNTs show their p-type characteristics due to oxidization from water molecules and oxygen atoms, although this can be easily altered by using other materials as dopants; semiconducting carbon nanotubes have a LUMO level of about -4.22 eV and a HOMO level at -4.74 eV [14]. The LUMO and HOMO levels are an analogous to the conduction and valence band of the semiconductors, respectively, but for molecules.

1.1.2 Indene- C_{60} Bisadduct

In the 1980's, Harold Kroto was investigating some long and flexible chains of carbon that form clouds in interstellar space and he wanted to study them. In 1985, he and his colleagues shot some graphite with a powerful laser. The carbon atoms reorganized themselves into molecules and luckily the long carbon chains were formed, but along with these chains, another extremely stable molecule with 720 protons was discovered and the only way that this could happen was with exactly 60 carbon atoms with 12 protons each atom. This molecule was not so reactive to other substances, which was weird at the time for a carbon structure since carbon has 4 spare electrons that can be used for bonding so this lead Kroto to believe that this molecule could be spherical. After further investigation, the hypothesis was confirmed and a new material was born, fullerene or Buckminsterfullerene (C_{60}) [15].

Of course, after that discovery, it became clear that C_{60} and C_{70} were not as soluble as other materials in organic solvents. Thus, several other fullerene derivatives emerged such as PC_{60}BM , bis PCBM , PCBB , PCBO , TCBM , PC_{70}BM , ICMA and ICBA . Compared to other fullerene derivatives, Indene- C_{60} Bisadduct (ICBA) has caught the attention of many due to its high Lowest Unoccupied Molecular Orbital (LUMO) energy level and the fact that its Fermi level is pretty close to the LUMO level making it a good candidate to be used as an n-type semiconductor [16]. More specifically, ICBA has a LUMO level of -3.63 eV and a HOMO level of -6.0 eV [14]. ICBA , has been first synthesized in 2010 and has a solubility of $>90 \text{ mg/mL}$ [17]. The ICBA molecule can be seen in Figure 3.



Figure 3: The chemical structure of Indene-C₆₀ Bisadduct. [17]

It is important to note that ICBA, amongst some other organic semiconductors, has the advantage of trap-free electron and hole transport. This was verified by Kotadiya *et al.* [18], where it was shown that if a material has ionization energy higher than 6 eV, then hole trapping would be dominant and thus the hole transport would be limited. On the other hand, if electron affinity was lower than 3.6 eV, then electron trapping would occur leading to lower electron mobilities. Luckily, ICBA is marginally between the trap-free window making it suitable as a higher mobility material and both as a p-type and an n-type semiconductor.

1.2 Fabrication of Nanomaterials

The need of scaling down devices came from the ever rising demands of higher frequency electronics and it became clear that although silicon technology was offering a lot, and to this day still is, a limitation started to emerge. Silicon FETs can no longer be miniaturized further mostly because of undesired leakage current from source to drain due to tunneling [19]. Moreover, miniaturization of the semiconductor has to be followed by a miniaturization of the dielectrics that are used to increase the performance of the devices [20]. The most promising candidate for this job are 2D materials and nanomaterials. Therefore, it is crucial to understand how these materials are fabricated and later in Chapter 2, the deposition techniques will be presented.

1.2.1 Fabrication of Carbon Nanotubes

There are several techniques that are used to fabricate carbon nanotubes, although four of them seem to be the most promising in producing good quality material: arc discharge (mentioned in Section 1.1.1), laser ablation and chemical vapor deposition (CVD). The first two methods are capable of producing CNTs in a form of powder, making it necessary for further processing, while CVD-fabricated CNTs are deposited directly on top of the wafer [21].

The fourth method that seems to be the most prevailing in producing bulk quantities of nanotubes is the high pressure carbon monoxide process or HiPco for short. The entire process requires a reactor made of thick aluminum cylinder and inside the aluminum chamber, there is a thin quartz wall. The concept is that Fe(CO)₅ and CO are injected into the reactor and are rapidly heated to enhance the formation of nanotubes. Also, there is a graphite preheater to introduce hot carbon monoxide to the Fe(CO)₅/CO mix. After the mixing, the iron atoms are decomposed and Fe clusters are formed. These clusters then play the role of catalytic particles which carbon nanotubes grow on. Finally, iron particles, single walled CNTs and carbon monoxide are travelling inside a tube through

the hot gas created at the beginning. Then, the gas flow passes through several filters and cooled surfaces, helping the carbon nanotubes to condense. The remaining gas is then cleaned and sent again to repeat the cycle from the start. Of course, the above procedure is possible by using high pressure inside the chamber to help the formation of the CNTs, hence the name of the process [22].

After the fabrication, an obstacle appears since the carbon nanotubes are tangled together and the product is comprised of both semiconducting and metallic tubes. There is an easy way to separate the two different kinds of CNTs simply by using sodium dodecyl sulfate solution and some liquid agarose to turn the mixture into a gel and mixing all the nanotubes together. Then, the application of a small current causes the metallic nanotubes to be transferred to the solution and leave from the agarose gel, a process called electrophoresis. Now that the two types of SWCNTs are separated, there are several ways to extract the semiconducting nanotubes, like squeezing the solution manually out of the gel or through centrifugation. The gel containing the semiconducting nanotubes can be removed by heating, centrifugation and then redispersion [23].

1.2.2 Fabrication of Indene-C₆₀ Bisadduct

Indene-C₆₀ Bisadduct is a pretty novel material, since it was fabricated in 2010 and is comprised of 78 carbon atoms and 16 hydrogen atoms with a molecular weight of 953.0 g/mol [24]. The difference with C₆₀, which has a molecular weight of 720.66 g/mol [25], is that ICBA contains two indene molecules on each side of the fullerene cage, changing its reactivity and thus its doping. It is clear that in order to obtain ICBA, C₆₀ needs to be fabricated first, so a few words about that are necessary.

There are two main ways in which C₆₀ can be produced. The first one is by creating a molecule that contains 60 carbon atoms, 75 of the 90 carbon bonds needed and 13 of the 20 benzene rings required to form C₆₀, that is a polycyclic aromatic hydrocarbon, C₆₀H₃₀. By activating a powerful laser, cyclodehydrogenation can be induced and the molecule can be “stitched” together creating the desired fullerenes. The only problem is that through this procedure, a mix of C₆₀ and C₇₀ are produced making the isolation of the different molecules a little more time and money consuming [26]. The other process that shares the same philosophy is through flash vacuum pyrolysis. More specifically, a precursor is again made with the formula C₆₀H₂₇Cl₃ and by introducing the halogen atoms, i.e. Chlorine, resulted in the production of isolated C₆₀ [27].

The synthesis of ICBA is as simple as it gets. A solution of the molecules Indene and C₆₀ are dissolved in 1,2,4-trichlorobenzene, and then the process of refluxing takes place by applying heat until there is dry residue. The application of heat and the mixing of the solution with methanol repeatedly, removes the solvents and, eventually, all the liquids are evaporated leaving the residue filled with ICBA, ICMA (Indene-C₆₀ Monoadduct) and unreacted C₆₀. Of course this mixture is not useful on its own so it is evident that separation and purification is needed. This process is easily done by silica gel column chromatography and the desired molecule, Indene-C₆₀ Bisadduct, is obtained [17].

1.3 Carbon-based electronics

In the last decade, it is becoming obvious that a drastic change is over the horizon. The need for devices that surpass the expectations of the consumers is ever growing but the limitations are also emerging. There is a necessity for novel materials that surpass the current difficulties with relative ease, meaning that the integration in modern applications will be as simple as with the previous materials used. A new class of materials started emerging: the carbon-based materials. Carbon-

based materials offer extraordinary features that are possible candidates for both electronic and optoelectronic applications. Of course, as mentioned before the reason that carbon-based materials attracted many scientists attention is due to the fact that scaling down with the conventional semiconductor materials is laborious for both in a scientific and a technical manner.

1.3.1 Conventional semiconductors limitations

In the 80's, researchers first saw these limitations appear, when short-channel effects were observed in MOSFETs [29], [30]. This would mean that further miniaturization of the channel would lead to tunneling effect, making the transistor unusable, at least for its initial purpose of working as a 1 and 0 switch, the known modern digital logic. Of course there are some efforts to utilize these effects with tunnel-FETs [31], [32] but these devices don't seem to correspond to the requirements of this era. Part of this problem that gets in the way of miniaturization is what is called drain-induced barrier lowering, where by reverse biasing the one part of the junction, a field pattern is created which results in lowering of the potential barrier, leading to unwanted diffusion in the adjacent junction [32]. Indeed, the problems do not cease there. As the silicon and other bulk semiconductors become thinner and thinner, new effects like scattering with acoustic phonons of the surface and scattering due to surface roughness are emerging which all seem to lead to the conclusion that the electron and hole mobility is being affected [33]. More specifically, silicon as a 3D bulk material has an electron mobility of about $1350 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a hole mobility of about $480 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [34], which was enough for many years to cover the speed needs of most of the hardware, but as the shrinking of the silicon films was occurring, to achieve higher frequency operations, the mobility of the material was starting to decrease. The reason this happens is because by reducing the film in size, the electrons are getting confined which increases the phonon-scattering rate leading to a mobility decrease [35].

1.3.2 Carbon materials potential

Therefore, is it becoming clear that short-channel effects must be suppressed and the best way to do that and improve the performance of the device is to make the channel and the gate dielectric very thin [36]. One way to do that is by replacing the conventional bulk semiconductors with new carbon materials.

Graphene has caught the attention of many due to its special linear density of states, its potential of reaching ultra high speeds due to ballistic transport, its outstanding carrier mobility and of course the smallest possible thickness, that of one single atom [37]. Nevertheless, the fact that graphene has a zero bandgap, makes it a bad choice for logic applications, meaning that a transistor made of graphene cannot be switched; graphene nanoribbons can also be used but the mobility drops dramatically [38].

The next big candidate with promising features is the carbon nanotube. Carbon nanotubes offer exceptionally high mobilities making them ideal for high frequency devices like FETs and sensors [39]. Unlike graphene, semiconducting CNTs possess a bandgap of 0.52 eV and exhibit p-type or ambipolar characteristics depending on the material that is in contact with the CNTs [14]. Carbon nanotubes will be the main focus of our study since they offer a lot of novel properties like ballistic transport and due to the 1D nature of the tube, small angle scattering is forbidden. Moreover, a quantized resistance is emerging as a consequence of the 1D configuration of the tube in contact with 3D materials, i.e. the metal contacts [40].

Finally, an increasing interest in fullerenes and its derivatives has been observed mainly due to the exceptional properties that make them ideal as electron acceptors in organic solar cells. The most famous fullerene derivative that is currently used is phenyl- C_{61} -butyric-acid-methyl-ester or PCBM for short, although ICBA seems to be the successor of PCBM in the coming years due to easier fabrication and higher electrical currents with certain materials [41]. Of course, many fullerenes can

be used both as donor and acceptor, depending on the materials in contact with them. For ICBA, for example, there is evidence that it is an ambipolar semiconductor, meaning that it can be used both as p-type and n-type material, a conclusion that was drawn from the fact that the electron and hole mobilities were both in the range of $10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, a mobility 100-1000 times higher than C_{60} and about the same mobility as PCBM [42]. As a matter of fact, these values can be altered based on the metal contacts and the interface between them and other materials and the processing methods of the fullerenes. More specifically, it was shown that by using the appropriate dielectric material grown on SiO_2 , the molecule-molecule and molecule-substrate interaction could be modified. Furthermore, proper annealing temperature showed that an early stage of crystallization was being formed in the ICBA thin film. This resulted in an electron mobility that approached $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, one of the highest ever recorded for ICBA [43].

1.3.3 Carbon nanotubes and Indene- C_{60} Bisadduct interaction

Although it is a very useful practice to understand the properties and the behavior of each material separately, a great virtue stands in the process of understanding the interaction between two materials as well and in our case: SWCNTs with ICBA. The interaction between these two semiconductors is not yet examined extensively, given the fact that ICBA is a relatively new material. Nevertheless, horizontally-aligned carbon nanotube FETs have been fabricated with ICBA on top of the CNTs and it was confirmed that ICBA induces n-doping to the single-walled CNTs although the effect was negligible compared to the atmospheric oxidation due to water molecules and oxygen which resulted in p-doping of the CNTs [14]. Moreover, fine tuning of CNT energy levels seems to be very crucial for many applications such as light emitting diodes, field effect transistors and solar cells and fullerenes are appropriate for this job [44].

Furthermore, to have a clearer picture of the interaction between the two materials the energy levels are useful. As seen in Figure 4, the Energy Levels at zero bias is presented with x-axis showing the row in which the metal contacts, the CNTs and the ICBA were deposited. The thicknesses of the materials are not in scale. The y-axis indicates the energy levels of the metals and the semiconductors with the numbers on the axis being negative. The vacuum energy level E_0 is set at 0 eV. Also, the values for the work functions of the metals were retrieved from [45] and for CNT and ICBA from [14]. The black circles are electrons and the white circles are holes. Another thing that needs to be mentioned is that the band bending between the semiconductors and the metals is difficult to be calculated and, hence, this is not an Energy Band Diagram (EBD).

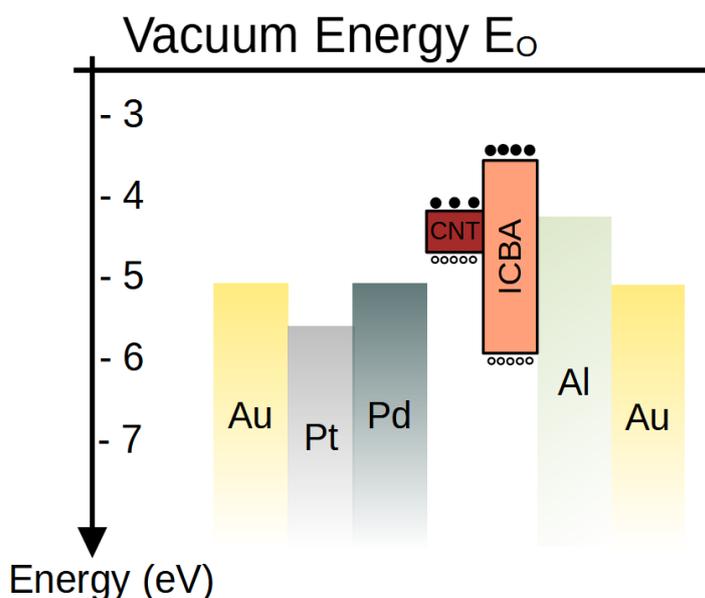


Figure 4: Energy levels of the fabricated device at zero bias.

1.4 Diode Theory

A diode is an electrical component that conducts current in a unidirectional way, meaning that it conducts electricity in one direction known as forward bias and blocks the current in the opposite direction known as reverse bias. Ideally, in the conducting direction, there is zero resistance and in the blocking direction there is infinite resistance. Realistically, the ideal case is not achieved in any of the two directions. Diodes are mostly made with conventional semiconductors like silicon, germanium and gallium arsenide but as explained in 1.3.1 there are many limitations to these kinds of materials.

1.4.1 Ideal Diode

The main function of a diode is to rectify. For example, diodes can be used to convert alternating current into direct current. There are many kinds of diodes such as pn diodes, LEDs, Schottky diodes, tunnel diodes etc. but the feature of unidirectionality is almost universal. But to understand better how a diode works, seeing the way current behaves with the application of voltage, is extremely helpful. In 1949, William Shockley was the first to publish the ideal pn diode equation [46] which was later named after him as the Shockley equation and it gives the diode current as follows:

$$I = I_S \cdot \left(e^{\frac{qV_D}{nkT}} - 1 \right) , \quad (\text{Eq. 1})$$

where I_S is the saturation current that is attained when the diode is reverse biased and is expressed as $I_S = A \cdot A_R T^2 e^{-\frac{q\Phi_B}{kT}}$, with A the effective area of the contact at the junction, A_R is the Richardson constant, T is the temperature and Φ_B is the Schottky barrier height (SBH) that is formed at the metal-semiconductor interface between the two Fermi levels [47]. Extraction of these parameters will be discussed in Section 1.4.3., V_D is the voltage across the diode, k is the Boltzmann constant, T is the temperature, q is the electron charge and n is the ideality factor which describes the current transport mechanism: it can take the value of 1 if the mechanism is diffusion, 2 if the transport mechanism is recombination of charge carriers, a value between 1 and 2 if both of the mechanisms exist and finally if $n > 2$ then other mechanisms are involved in the current transport [48].

One can observe that by applying negative voltage ($V_D < 0$) the exponential term approaches zero, leading to a diode current: $I = -I_S$. On the other hand by forward biasing the diode, the exponential term grows fast making the “-1” term negligible and the diode current now is: $I = I_S \cdot \exp(qV_D/nkT)$. Of course, it is important to note that current does not only depend on voltage but on temperature as well, as shown in Figure 5. Also, the reverse current reaches very small values, compared to the forward bias current, but is also affected when temperature increases. The values for the plot were chosen arbitrarily but within the realm of possibility. The temperatures were 300 K, 350 K and 400 K and the Schottky barrier was 0.51 eV with an ideality factor of 2.

In order to understand why the graph below has this behaviour, one needs to see what is going on on the nanoscale between the p-type and the n-type surfaces. As seen in Figure 6a, when no voltage is applied between the two sides, a region is formed where both materials are stripped away from their charge carriers due to recombination of holes and electron, leaving behind negative ions on the p side and positive ions on the n side. This region is called depletion layer and it can be seen below as the light-coloured area in each side. Of course, the ions that remain are atoms of each semiconductor. Naturally, no current is flowing in this mode of operation.

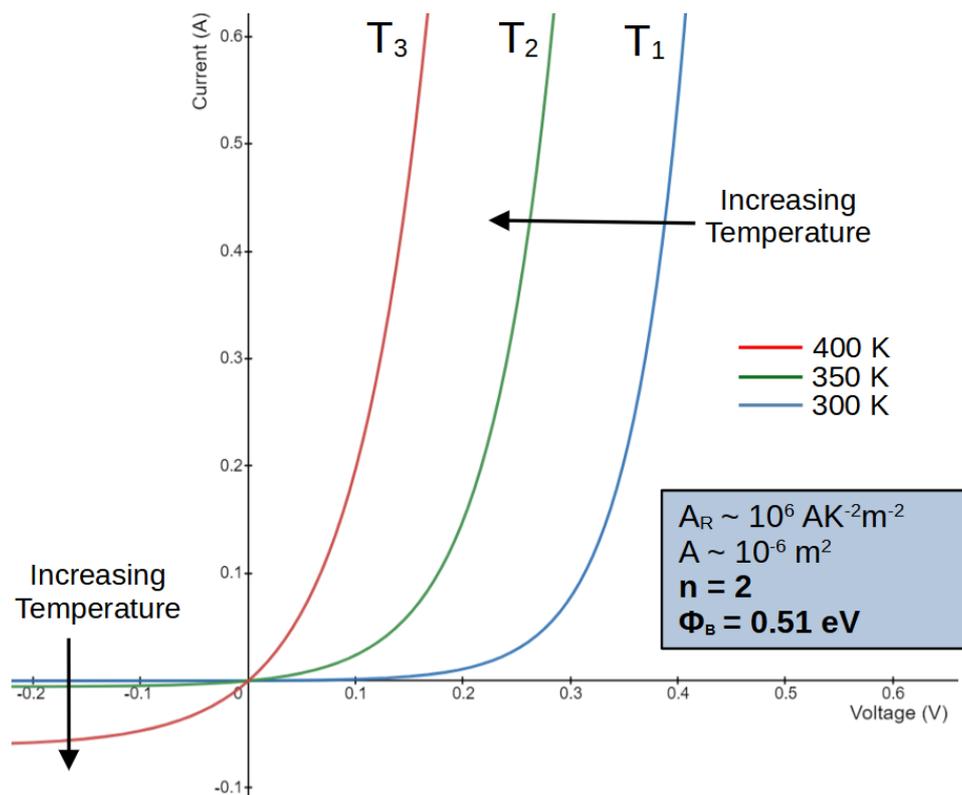
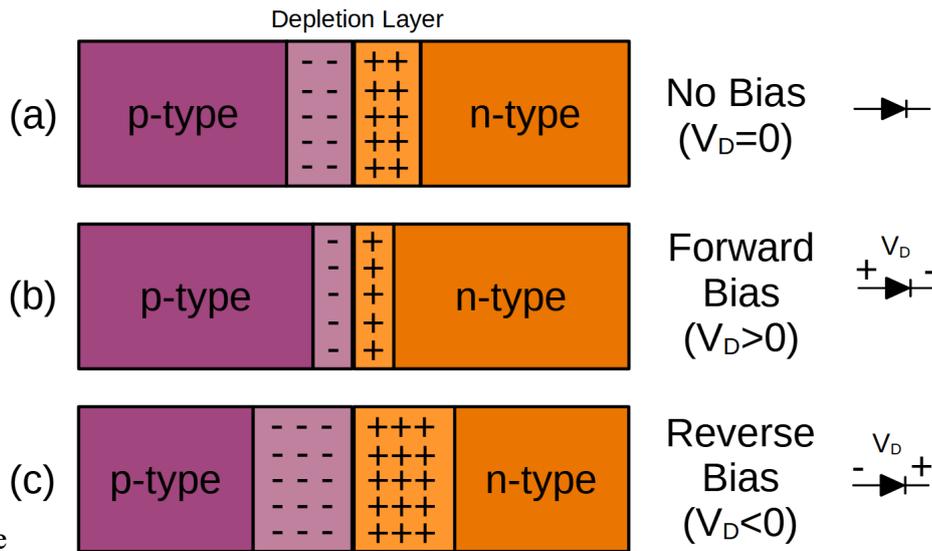


Figure 5: Temperature dependent current-voltage characteristics of a pn diode.

When a positive diode voltage (forward bias) is applied, then the width of the depletion layer shrinks, as expected, because carriers are starting to fill the two sides: holes in p-side and electron in n-side. Nevertheless, recombination is still happening in the contact area so the depletion layer cannot disappear entirely as seen in Figure 6b. In this mode of operation, the highest values of the currents are achieved as seen in Figure 5, for positive voltage.

Finally, when a negative voltage is applied, carriers opposite to the ones before are starting to flow and the recombination rate increases, or another way to look at it, which is also correct, is to think that the charge carriers are pulled away from the pn junction making the depletion layer wider. Of course, it is obvious that this will result in a current close to zero because the majority carriers cannot pass through the depletion layer due to the large electric field created. This electric field is seen as a barrier for the holes and the electrons making their passage from the one side to the other almost impossible. The schematic of this mode is depicted in Figure 6c. Almost, because some

manage to go through the depletion region, resulting in a small reverse current, called leakage current, as seen in Figure 5 for negative voltage.



1.4.2 Non-ideal Diode

Although the above give a good sense of how a diode

Figure 6: Schematic of the three modes of operation of a pn junction: (a) No Bias, (b) Forward Bias and (c) Reverse Bias.

works, unfortunately it does not depict reality. In reality, there are a series of reasons that contribute in the divergence from the ideal case.

First of all, generation and recombination of electrons and holes need to be taken into account. Moreover, high injection conditions, tunneling between bandgap states and surface effects are also important. Another non-ideal effect occurs when inducing high electric fields, i.e. high voltages in the reverse biased mode of operation, leading to avalanche or tunneling breakdown. Last but not least, the diode, with respect to circuitry, has an extra voltage drop due to a non-ideal series resistance [49]. Taking that into account, Equation 1 must be changed into:

$$I = I_s \cdot \left(e^{\frac{q(V_D - IR_s)}{nkT}} - 1 \right), \quad [50] \quad (\text{Eq. 2})$$

where every parameter is the same as Equation 1, except R_s which is the series resistance.

To see the difference from the ideal, it would be helpful to understand what is the equivalent circuit of a non-ideal diode. Fundamentally, no diode can be perfect when it comes to its conductivity, meaning that there will always be some minor resistance even if the fabrication process is perfect, because the materials used have different interfaces, manifesting potential barriers, contributing in the series resistance. The series resistance in general is comprised of the resistance of the semiconductors, the resistance between metal and semiconductor contacts and the contact resistance at the junction. Furthermore, due to the depletion of the junction region, a depletion capacitance will be formed that will be in parallel with the ideal diode and a part of the series resistance, R_D i.e. the diode resistance. That is because only a part of it will play a role when the diode is forward biased [51]. There is also the resistance due to the capacitance, R_{Cap} . When one measures the circuit from one terminal to the other, the series resistance R_s , mentioned above, is retrieved. The role of the depletion capacitance and the series resistance will be explained in Sections 1.5.1 & 1.5.2. The schematic of the non-ideal diode circuit is depicted in Figure 7.

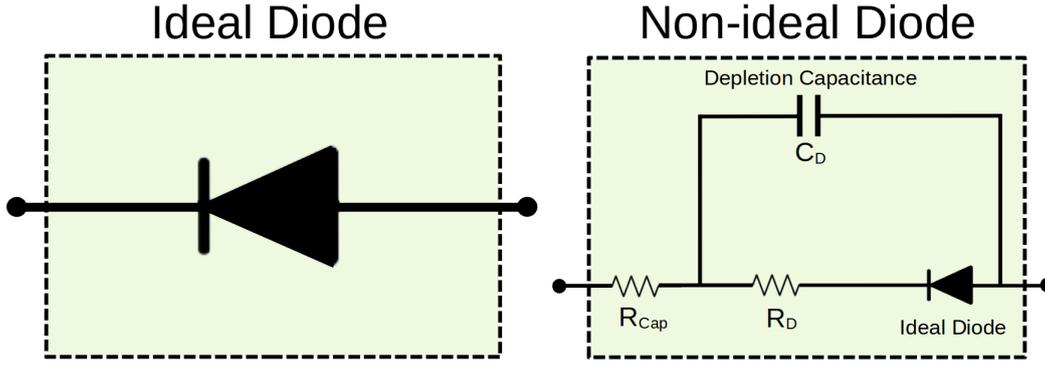


Figure 7: Equivalent circuit of an ideal (left) and a non-ideal (right) diode circuit.

1.4.3 Extracting Diode Parameters

Although theory is necessary to do good research, proving how good the performance of the device is, one needs to present the results of the experiment as well. Therefore, extracting certain parameters from the diode is both desirable and needed. The parameters of interest are three: the series resistance, the Schottky barrier height and the ideality factor. Generally, there is one way in the bibliography that is widely used to extract diode parameters without the use of complicated computer models.

One of the firsts to attempt extracting these parameters was Cheung in 1986 [52]. He showed that with a single I-V characteristic and a few tweaks of Equation 2, all these parameters could be obtained. More specifically if current is replaced by current density and Equation 2 is solved with respect to voltage then:

$$V = \frac{nkT}{q} \cdot \ln\left(\frac{I}{AA_R T^2}\right) + IR_S + n\phi_B \quad , \quad (\text{Eq. 3})$$

After, by calculating the derivative of voltage with respect to $\ln I$ we get:

$$\frac{dV}{d(\ln I)} = IR_S + n \frac{kT}{q} \quad , \quad (\text{Eq. 4})$$

By plotting $dV/d(\ln I) - I$, the series resistance R_S can be calculated from the slope of Equation 4 and the ideality factor from the y-axis intercept. Furthermore, by defining the functions:

$$H(I) = V - \frac{nkT}{q} \cdot \ln\left(\frac{I}{AA_R T^2}\right) \quad , \quad (\text{Eq. 5})$$

and

$$H(I) = IR_S + n\phi_B \quad , \quad (\text{Eq. 6})$$

$H(I)$ can be calculated from Equation 5 and then it can be plotted with current density from Equation 6 to calculate the Schottky barrier from the intercept with the y-axis. The problem that comes in the way is calculating the Richardson constant for Equation 6 because there are cases that the materials that are used have not been well studied and there is not enough evidence in the literature. It has been explained at [53] that Richardson's plot, can be used to calculate the Richardson constant by plotting $\ln(I_S/T^2)$ versus q/kT on the following equation:

$$\ln\left(\frac{I_S}{T^2}\right) = \ln(AA_R) - \frac{q\Phi_B}{kT} \quad , \quad (\text{Eq. 7})$$

This equation is simply the saturation current written in another form. It is obvious that Schottky barrier height can be extracted from the slope and the Richardson constant from the y-axis intercept. The linear fittings of forward current are used in order to extrapolate I_S at $V=0$. Of course for

different values of I_s , I-V characteristics at different temperatures must be taken. Taking advantage of Equation 7, gives us the freedom to neglect Equations 5 and 6, although one can use Equation 6 to confirm R_s and Φ_B , after evaluating $H(I)$ with the Richardson constant calculated from Equation 7. This method of using the Richardson's plot was also used by others recently [54], [55] both for pn diodes and Schottky diodes and the parameters were extracted successfully.

An example is going to be insightful; the values of which were chosen based on the expected values of the literature and are arbitrarily set for illustrative purposes only. First, by using equations 3 & 4, a plot of $dV/d(\ln I) - I$, will result in something like Figure 8, where after the analysis, series resistance R_s was found to be $125.8 \pm 4.2 \text{ m}\Omega$ and the ideality factor n was 1.12 ± 0.09 .

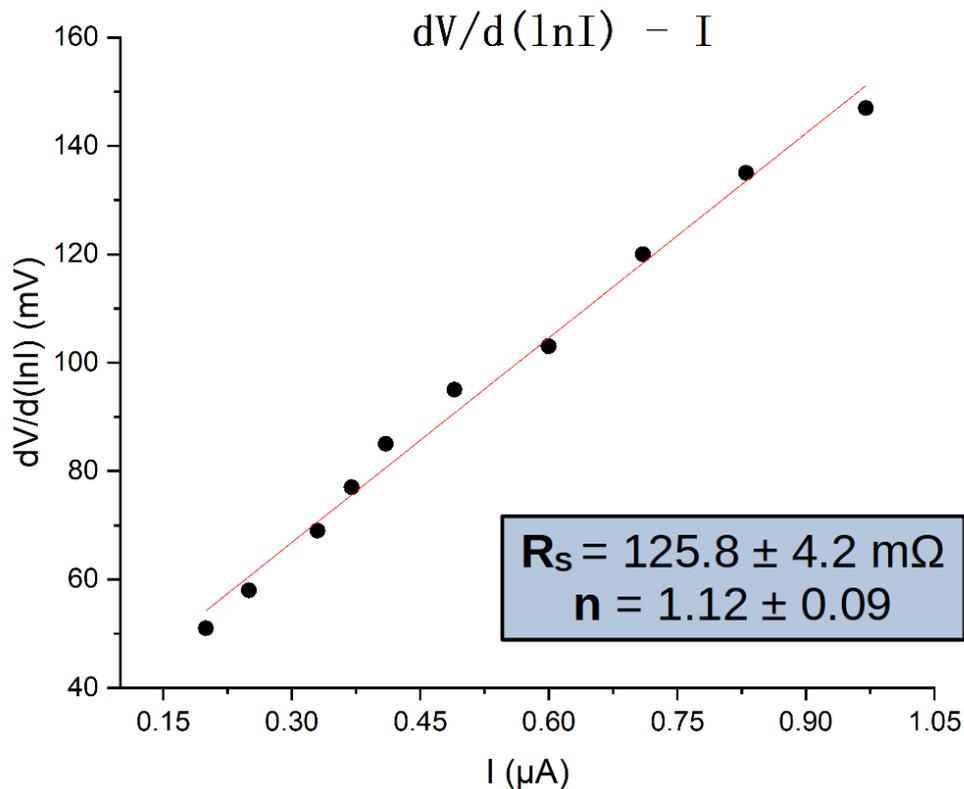
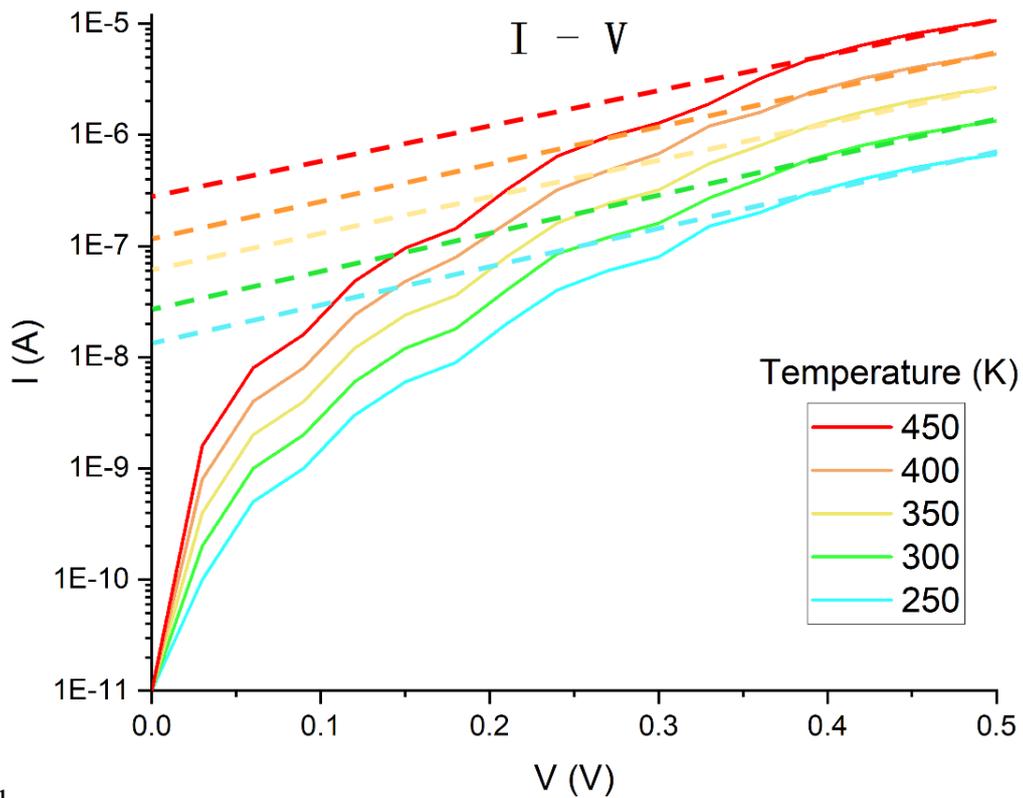


Figure 8: Illustrative plot of $dV/d(\ln I) - I$ with R_s and n extracted.

After calculating R_s and n , a forward bias I-V characteristic is taken in five different temperatures as shown below in Figure 9, in order to attain different values of saturation currents. This is

achieved by extrapolating to $V=0$ the linear region of the characteristic. The y-axis is logarithmic in order to see the saturation region, otherwise the plots would appear as exponential.



The final step after attaining the five saturation currents is to use equation 7 and create a plot of $\ln(I_S/T^2) - q/kT$. Doing that will result in Figure 10, where we can calculate Φ_B by the slope and A_R by the y-axis intercept. Φ_B is found to be 0.08 ± 0.01 eV and A_R is $(8 \pm 3) \cdot 10^{-4} \text{ A cm}^{-2} \text{ K}^{-2}$.

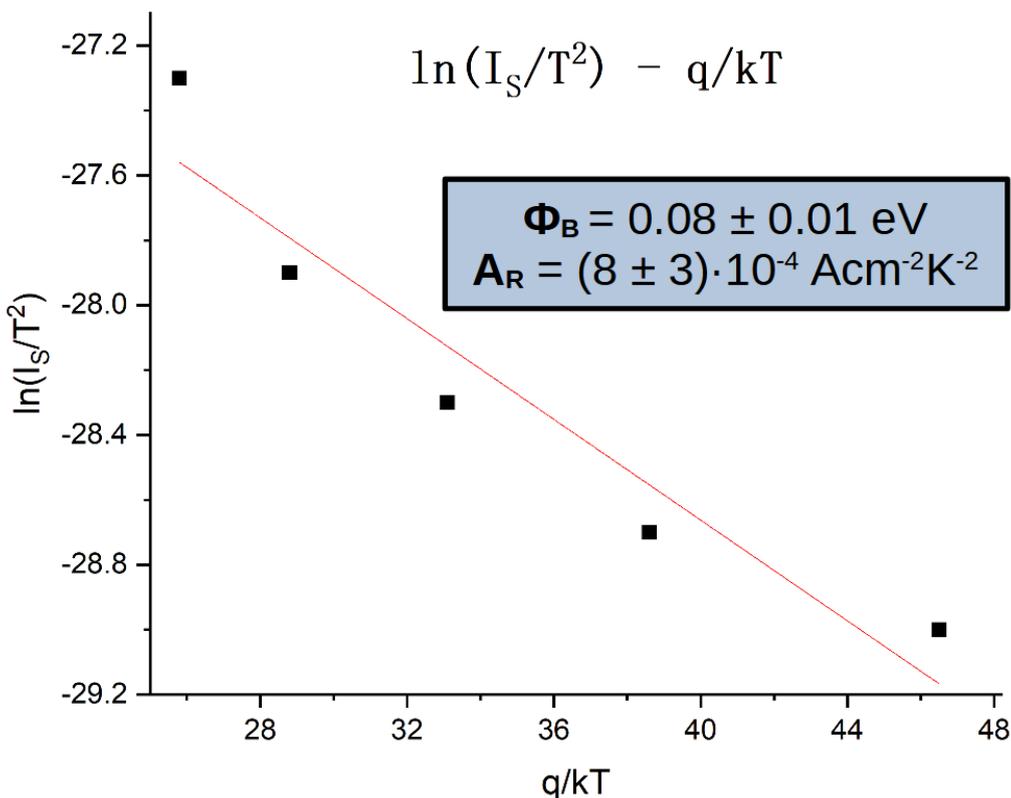


Figure 10: Illustrative plot of $\ln(I_S/T^2) - q/kT$ with Φ_B and A_R extracted.

1.5 High Frequency Diodes

The ultimate goal of this work is to demonstrate the performance of our diodes in high frequencies. There is a high demand in such applications which stems from the ever increasing needs of the market to achieve higher speeds and easier interconnection between electrical devices, the so-called 5G and 6G networks, which span across several GHz and THz respectively. Unfortunately, as luring as it may sound to have devices working at the Terahertz range, it is yet a technology that is far from publicly commercializing and although many efforts are being made some physical limitations arise. The main factors that pose a threat to the idea of increasing in frequency are two: capacitance and resistance. These concepts are unwinded in Sections 1.5.1 & 1.5.2.

1.5.1 Capacitance Problem

In general, the total capacitance of a pn junction consists of two parts: the diffusion capacitance and the depletion layer capacitance i.e. $C_{tot}=C_D+C_{diff}$. The origin of the depletion layer capacitance is easy to comprehend; the two semiconductors at the junction vicinity have positive and negative net charge at the n-region and the p-region respectively, when the diode is forward biased and a depleted layer is formed. This difference in charge creates a capacitance. The diffusion capacitance is a little bit more complicated. Essentially, it arises because of the accumulation of minority carrier during the recombination process [56]. To make this even clearer, imagine that when AC signal is applied, the charge accumulation becomes ever increasing with every increase in voltage leading to a gradient of charge across the depletion region. This gradient is enough to result in a small capacitance. Mathematically, diffusion capacitance is $C_{diff} = dQ/dV$. Therefore it is logical to think that when voltage rises rapidly the derivative goes to zero. This means that when the diode is used in high frequencies, diffusion capacitance is no longer able to follow the AC signal, so C_{diff} is negligible and the remaining capacitance is the depletion layer capacitance [57].

The theory considers a capacitor as a high pass filters, meaning that in high frequencies, it stops behaving as a capacitor and starts behaving as a wire. Now, in some cases this would be a useful characteristic to have, but in our case it is a problem. Having in mind the non-ideal diode circuit of Figure 7, and ignoring the series resistance for now, the capacitance is in parallel with the diode. But the picture is changing now that the depletion capacitance is acting like a wire. As shown in Figure 11, when the AC signal has a high frequency, the impedance of the capacitor drops to zero, allowing all the current to pass through this path and essentially no current through the diode's path. This result makes the circuit unable to rectify, rendering the diode useless.

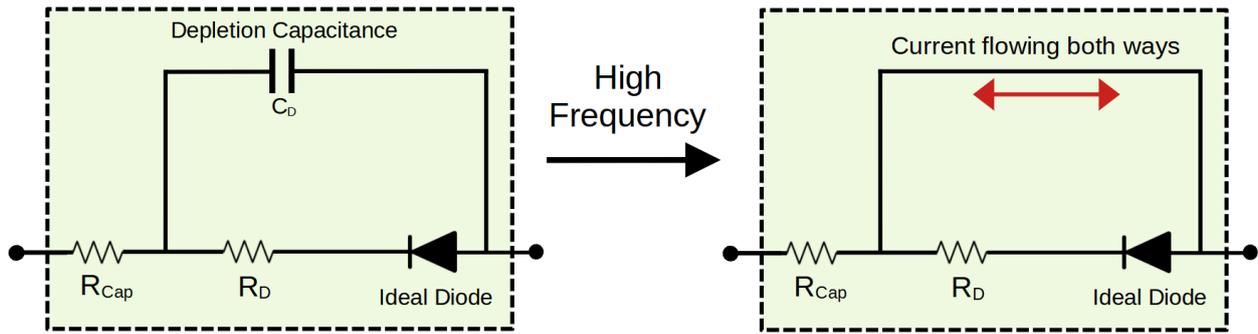


Figure 11: Equivalent circuit of a low frequency (left) and high frequency (right) pn diode.

Therefore, it is apparent that the capacitance needs to be eliminated or at least minimized in order to avoid the degradation of the performance of the device. Limiting the capacitance is not an easy task. The capacitance of two plates of area A and distance d is given by:

$$C = \epsilon \cdot \frac{A}{d} , \quad (\text{Eq. 8})$$

,where ϵ is the permittivity. One can draw the conclusion from Equation 8 that by decreasing the contact area between the two semiconductors, lower capacitance can be achieved. Nevertheless, increasing the distance between the two plates will not be helpful at least in a resistance perspective, creating a larger barrier for the charge carriers to overcome.

1.5.2 Resistance Problem

The final obstacle that comes in the way is the series resistance. It would be illogical for someone to think that when applying high AC signal, the resistance would not be affected. As a matter of fact, when the frequency is increased the resistance is increased as well. There is also another effect that increases the resistance when the current is alternating rapidly called skin effect, where the current is reduced inside the conductor and increased near the surface due to the electric and magnetic fields created but the increase is very subtle compared to the overall series resistance although considering this effect leads to more accurate results i.e. closer to the experimental values [58]. Hence, it is clear that having a lower resistance is beneficial for the overall performance of the device. Moreover, having a lower resistance aids in the lowering of the power consumption since $P=I^2R$.

- End of Chapter 1 -

Chapter 2 – Experimental Techniques

2.1 Device processing

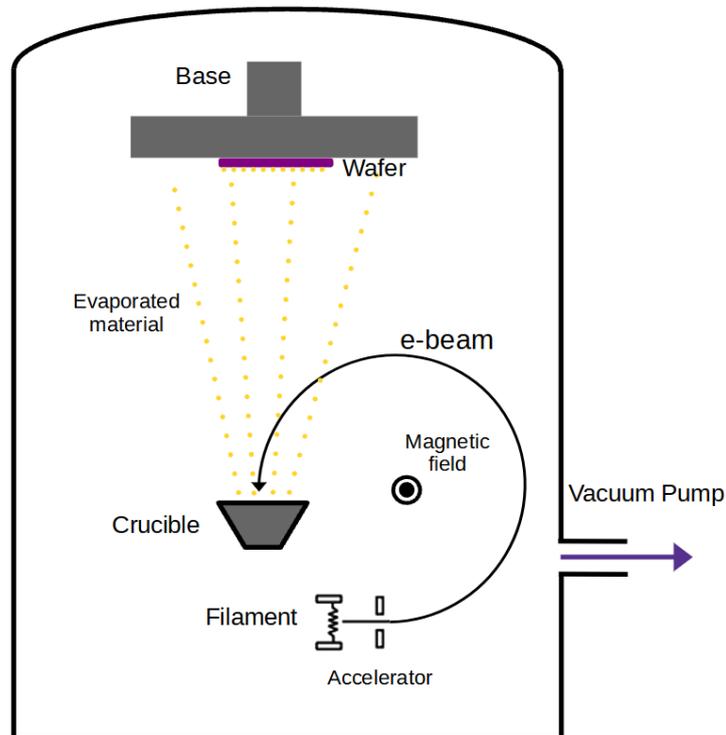
The most important step to achieve the highest performance is to ensure that the device processing is done correctly. Doing that, requires common techniques that will be analyzed further in the following sections. The main goal is to miniaturize the device to the point that it is desired, to make it reliable meaning that the behavior is repetitive without any degradation of the performance and to achieve easy integration with the current technology and its requirements. The most common techniques are three: lithography, spin coating and e-beam evaporation.

2.1.1 Spin Coating

Thin films can be deposited from a solution with a technique called spin coating. The deposited material is usually a photoresist, which is diluted in a proper solvent. The solution is applied on the wafer and then it is spun with high speeds. The centrifugal forces, combined with the viscosity and the surface tension, help the material spread uniformly. Also, increasing the surface that the material is spread, allows the evaporation of some of the solvent. In order to remove the entire solvent, heating the wafer is needed.

2.1.2 Electron Beam Evaporation

Physical Vapor Deposition or PVD, includes two main methods of deposition: electron beam evaporation and sputtering. The method that will be used in this project will be the e-beam evaporation, hence it is logical to explain only this method further. Electron beam evaporation is mostly used for metals. A metallic material, placed inside a crucible which is a holding case usually made of graphite, is heated by an incident electron beam as seen in Figure 12. The electron beam is produced by a metallic filament and then the electrons are accelerated. The beam is curved with the help of a magnetic field and hits its target at the crucible. The material that is hit with electrons is now getting warmer, to a point where the metal can no longer maintain its solid state, hence evaporation occurs. The vapor now travels upwards where the wafer is placed at a spinning base filling the surface of the wafer with the desired material. Of course, the entire process is possible by attaining a high vacuum through the vacuum pump. This ensures that the deposited material will not contain any contaminants from the air in the chamber. The electron beam evaporation is a directional deposition process and is considered one of the most reliable techniques of metal deposition.



2.1.3 Lithography

Figure 12: Electron beam evaporation process schematic.

Photolithography or just lithography is a process resembles that of the photographic negative development process. The materials used for lithography are photoresistive, sensitive polymers that are deposited on the surface of the wafer with centrifugation. After the spinning, the resist is baked in low temperature to help the solvent evaporate, in which the resist was initially diluted. The resist is not fully hardened, so by exposing the resist-covered wafer in UV light, some parts are hardened,

depending on the type of the resist: negative or positive. In Figure 13 the difference of positive and negative photoresist is shown. After the UV light exposure, the wafer is submerged into a chemical solution in order to remove the remaining “softer” resist; a process called development. After that, the etching happens, where certain chemicals are used to etch the layer under the photoresist. The last step is the photoresist removal. Hence, the desired pattern is created.

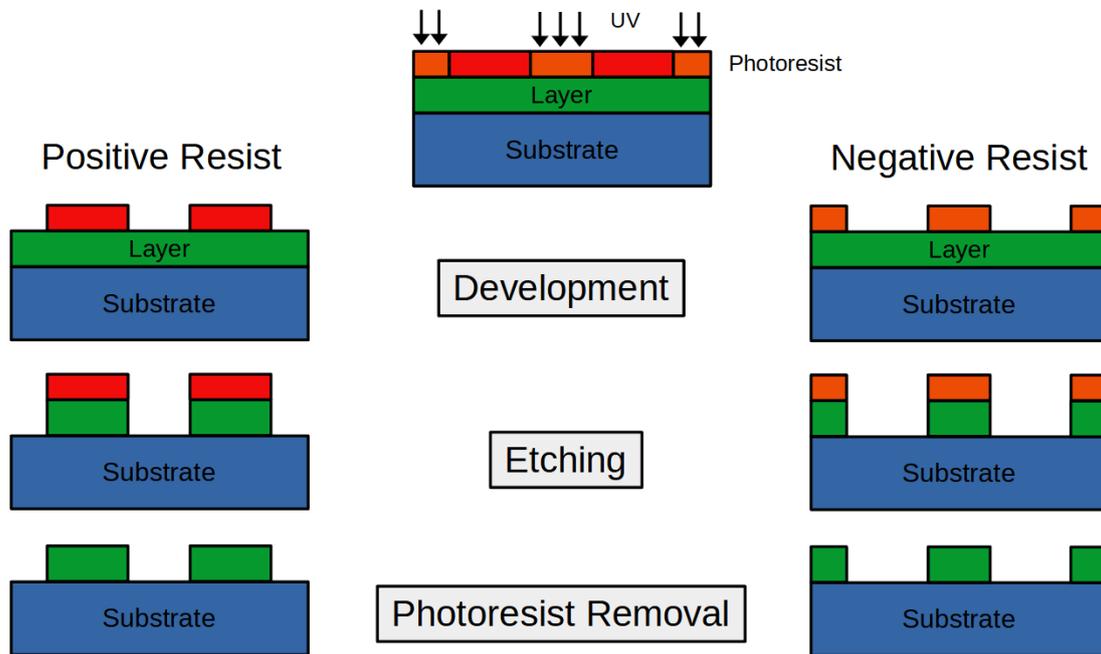


Figure 13: Process of lithography.

2.2 Experimental Material Deposition

The materials that were utilized for this project varied from metals and semiconductors to dielectrics. Naturally, the metals were used as pads for the realization of measurements and the deposition was accomplished via e-beam evaporation as detailed in 2.2.2. As semiconductors, thin films of single-walled Carbon Nanotubes and Indene- C_{60} Bisadduct were deposited as explained in 2.2.1 & 2.2.2 respectively. Moreover, in order to dope the CNTs properly, Perylene Tetracarboxylic acid Tetrapotassium salt was synthesized and deposited with a method described in 2.2.3. Lastly, 100 nm of Silicon Nitride (Si_3N_4) as a dielectric in order to minimize the contact area of CNTs and ICBA and to keep the materials outside the contacts separated. The deposition was made with PECVD at 150°C.

2.2.1 CNT films

The following section consists of the description of the CNT preparation steps. These steps include the preparation of the CNT dispersion and the preparation of the CNT membrane onto SiO_2 substrates.

First, the CNT dispersion was prepared. CNT dispersions were bought from NanoIntegris Technologies Inc.. The first part of the process is the cleaning of the CNT solution to get surfactant-free CNTs. Then, a known surfactant was added to disperse the CNTs in water. More analytically, the steps for removing the NanoIntegris surfactant were:

- Dispersion of the tubes with sonication (2 min at 20% power)
- Mix 2 parts of CNT solution with 1 part of acetone

- Sonication 5 min at 20% power
- Sitting of the solution for 1 hour
- Centrifuge for 1 hour at 10 000 RCF
- Remove solution and keep CNTs
- Dissolution of the CNTs in 2 parts of distilled water and 1 part of methanol
- Sonication 5 min at 20% power
- Sitting of the solution for 1 hour
- Centrifuge for 1 hour at 10000 RCF
- Remove solution and keep CNTs
- Repetition of the cleaning process a second time or more if needed

Preparation of aqueous CNT dispersion

- Drying the tubes
- Collect the tubes with water concentration = 0,24mg CNTs/mL water
- Bath sonication for 10 min at 20% power
- Add 0,5 mg/mL of SDS surfactant
- Sonication at 50% power for 1 hour



Figure 15: 12 mL of NanoIntegris solution after dispersion.

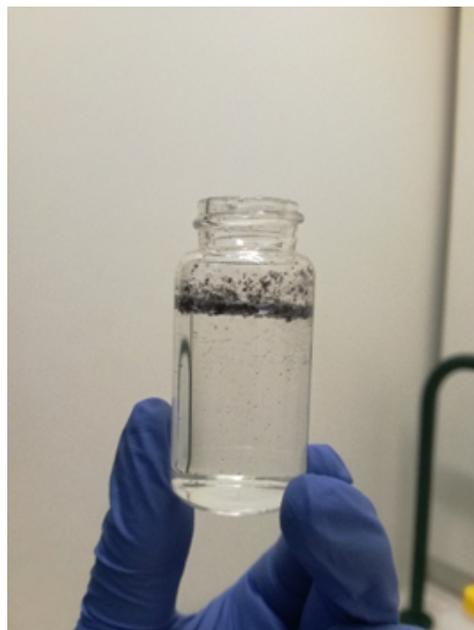


Figure 14: NanoIntegris CNT solution after cleaning process.

Preparation of the CNT membrane onto SiO₂ substrates

CNT membranes were deposited onto SiO₂ substrates using two methods:

1. vacuum filtration method in order to produce a mixed cellulose ester (MCE) membrane coated with CNTs
2. transferring method of CNTs onto SiO₂ substrates

Vacuum filtration

- The previously reported CNT dispersion was bath-sonicated for 10 min
- 1 mL of the aqueous CNT dispersion was added to 3 mL of distilled H₂O
- The resulting mixture was sonicated using a QSONICA CL-18 sonicator with a 2 mm sonication tip (Probe 4423) at 25% AMP for 5 minutes in order for the dispersion to be de-bundled
- A vacuum filtration apparatus was assembled as presented below using a MCE membrane (0.025 μm porosity)
- The filter was wetted with ~ 4 mL of distilled H₂O using a marked Pasteur pipette
- Vacuum was applied to the vacuum filtration apparatus in order for ~2 mL of distilled H₂O to pass through the filter
- The CNT dispersion was added to the vacuum filtration apparatus
- The solution was degassed
- The CNTs were washed with 4 mL of isopropanol and 60 mL of distilled H₂O while the solution was frequently degassed
- An MCE membrane coated with CNTs was produced

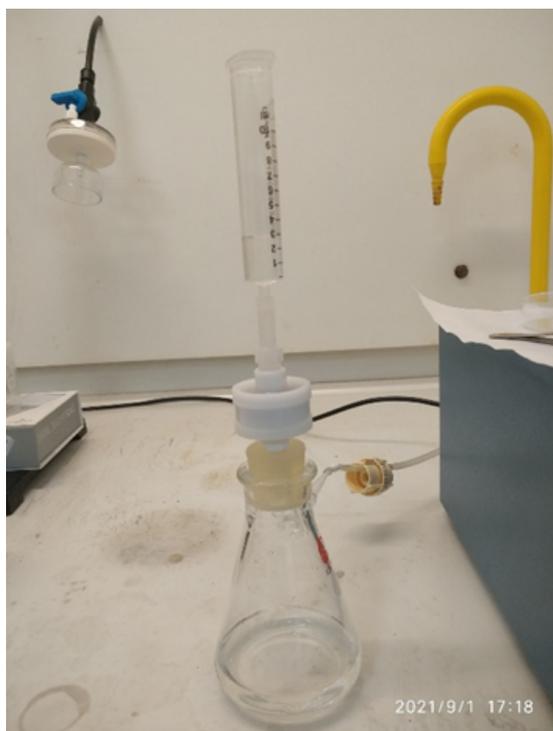


Figure 16: Vacuum filtration apparatus.



Figure 17: Mixed cellulose ester membrane.

Transferring of CNTs onto SiO₂ substrates

- The CNT-coated MCE membrane was dipped in ethanol for ~15 seconds
- The wet MCE was pressed carefully onto SiO₂ substrates
- The substrate was carefully placed onto a custom washing apparatus
- The substrate was washed with acetone in order for the MCE to be dissolved
- The CNT coated SiO₂ substrate was dipped into acetone for 3 minutes

The completed membrane of carbon nanotubes deposited onto the SiO₂ wafer can be seen in Figure 18.

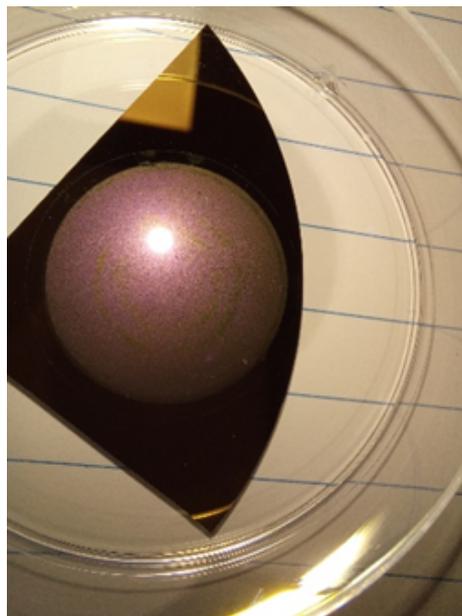


Figure 18: CNT membrane deposited onto SiO₂ substrate.

2.2.2 ICBA & Pd/Pt/Au deposition

Palladium, platinum and gold were deposited by the method described in 2.1.2, e-beam evaporation by using a high vacuum and the thicknesses were 50 nm, 20 nm and 100 nm respectively. The reason Pd was used in contact with CNTs is because it is previously reported that palladium forms an ohmic contact when in contact with CNTs for p-type carriers [59]. Moreover, platinum was used as a barrier between gold and palladium in order to avoid diffusion or in other words to compensate for the thermodynamic instability of the metal contacts and slow down the equilibrating process. This will eventually increase the lifetime of the contact [60].

Similarly, ICBA was deposited with the same method with a thickness of 50 nm.

2.2.3 PTCK₄ deposition

To create Perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTCK₄) several steps were followed shown in Figure 19 below. To begin with, 213,8 mg of Perylene tetracarboxylic dianhydride (PTCDA) were added in a recrystallization petri dish, followed by the addition of 238 mg of KOH and 100 ml of distilled H₂O. The petri dish was capped and the mixture was heated overnight at 50°C under stirring. PTCA was precipitated with the addition of ~20 ml of 1M HCl in the reaction solution. The precipitate was filtered, washed thoroughly with water and dried in a recrystallization petri dish. Then, 3 eq of KOH were added in the dish, followed by stirring and heating overnight at 50°C. The reaction solution was centrifuged and the supernatant was collected, containing the product, PTCK₄.

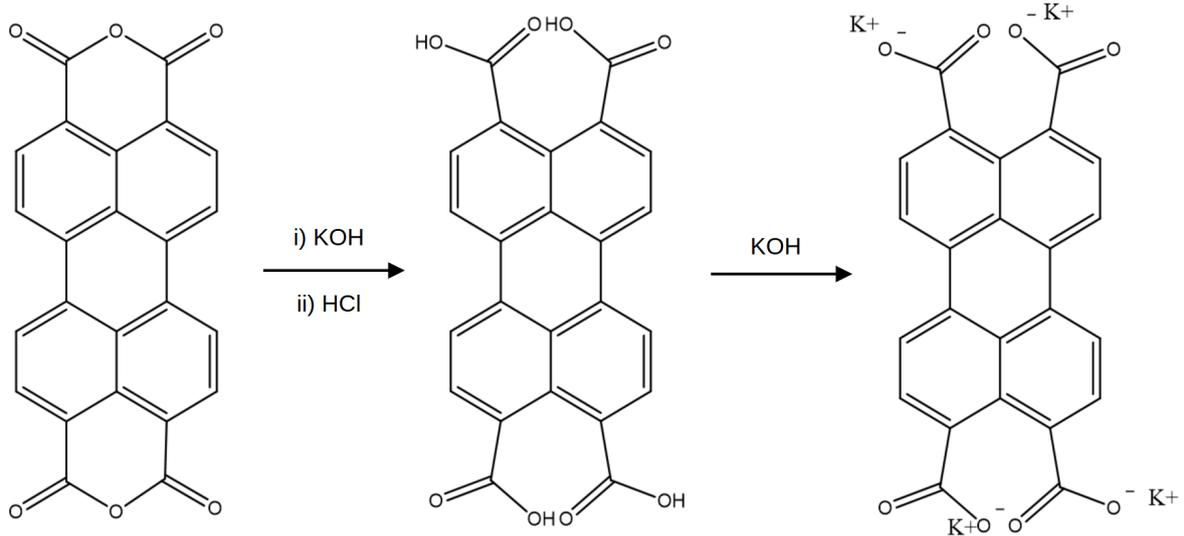


Figure 19: The steps to synthesize the Perylene Tetracarboxylic acid Tetrapotassium salt.

2.3 Characterization techniques

In order to find out whether the experiment had the desired result one needs to choose the right characterization techniques. More specifically, the techniques that were exploited for this project were: the Transmission Line Modeling, high frequency measurements and parameters extraction via Current-Voltage characteristics. The latter will not be further analyzed since it was extensively examined in Section 1.4.3. As for the other two, a few words are necessary.

2.3.1 Transmission Line Modeling

Transmission line modeling or TLM, is a method used to extract certain parameters of the fabricated device. The configuration of the device needs to be in a certain way. To be specific, as seen in Figure 20a, a semiconducting material (purple) is deposited over the substrate (green) and on top of the semiconductor, metal contacts (gray) are fabricated. What needs to happen in order to use this method successfully is to place the contacts at different distances, L_i as noted in Figure 20a, where $i: 1,2,3,4$. Measuring the resistance at different distances, allows us to create a plot of resistance versus distance, which in turn can give some parameters away. The plot is shown in Figure 20b. More specifically, the total resistance of the given configuration can be expressed as:

$$R_T = 2R_C + \frac{R_{SH}}{W} \cdot L, \quad [61] \quad (\text{Eq. 9})$$

where R_C is the contact resistance, R_{SH} is the sheet resistance, W is the width of the device and L is the distance between two contacts. Therefore, having in mind Equation 9, it can be seen that the slope can give us R_{SH}/W and from the y axis intercept $2R_C$ can be extracted.

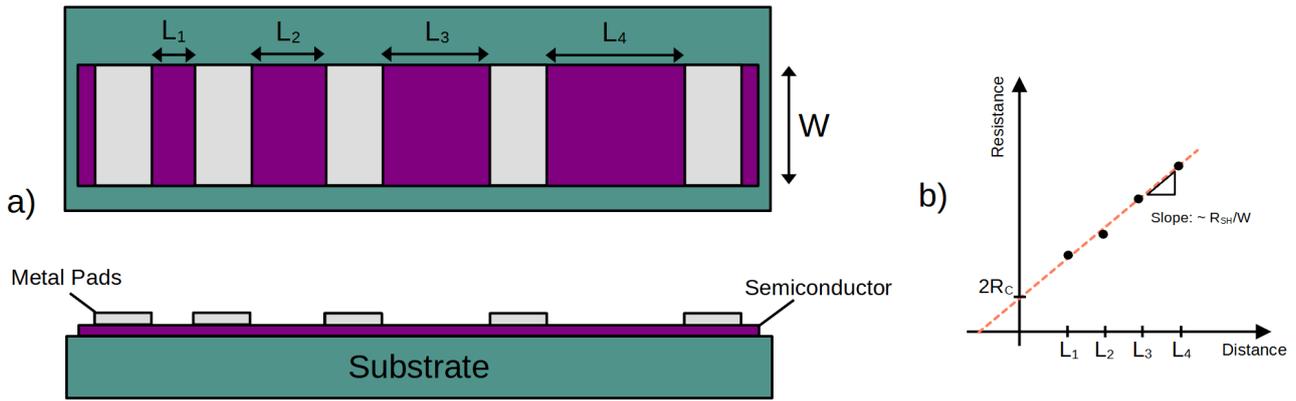


Figure 20: a) TLM schematic top view (up) and cross section (down). Green indicates the substrate, purple is the semiconducting material and gray are the metal pads. b) Measurements of resistance at given length with the y-axis intercept giving the R_C and x-axis intercept giving the L_T .

2.3.2 Vector Network Analyzer

The last experimental method that will be used on our device will be high frequency measurements. The instrument for this job is called a vector network analyzer and it is suitable for extracting the S-parameters of the diode. S-parameters or Scattering parameters are a set of values which are quite useful for electronics. Every device, depending on the frequency, has different values of S-parameters. Moreover, the number of ports also play a significant role. For example, as seen in Figure 21, a 2-port device will have 4 S-parameters: S_{11} , S_{22} , S_{21} and S_{12} , all representing elements of a 2×2 matrix with the first subscript denoting the port where the energy emerges and the second subscript the port where the energy enters. S_{11} and S_{22} are both called reflection coefficients and indicate the input and the output return loss, respectively. S_{21} and S_{12} are called transmission coefficients and represent the gain or loss that occurs. When one of those parameters is positive, it means that there is a gain and when it is negative there is a loss in the device. Ideally, when the device is unidirectional, S_{12} is usually preferred to be near zero; the parameter is then called as the reverse isolation.

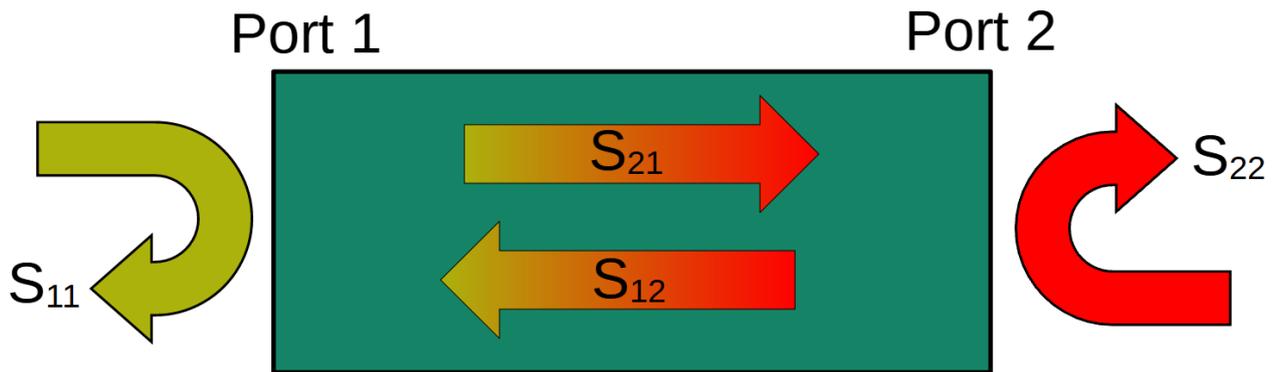


Figure 21: Schematic of a 2-port device showing the S-parameters S_{11} , S_{22} , S_{21} and S_{12} . Port 1 is the input and port 2 is the output of the device.

S-parameters are voltage ratios so it is necessary to see how they accrue. More specifically, these parameters can be expressed as:

$$S_{11} = \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+ = 0}, S_{22} = \left. \frac{V_2^-}{V_2^+} \right|_{V_1^+ = 0}, S_{21} = \left. \frac{V_2^-}{V_1^+} \right|_{V_2^+ = 0}, S_{12} = \left. \frac{V_1^-}{V_2^+} \right|_{V_1^+ = 0}$$

which arise from the following equations:

$$\begin{aligned} V_1^- &= S_{11} V_1^+ + S_{12} V_2^+ \\ V_2^- &= S_{21} V_1^+ + S_{22} V_2^+ \end{aligned}$$

- End of Chapter 2 -

Chapter 3 – Results

3.1 Device Fabrication

The first fabrication step was the CNTs deposition followed by the bottom metal electrode. The bottom metal is comprised of 2 nm of Chromium and 100 nm of Gold. The lithography was optical and the resist used was negative called AZ2020 nLOF.

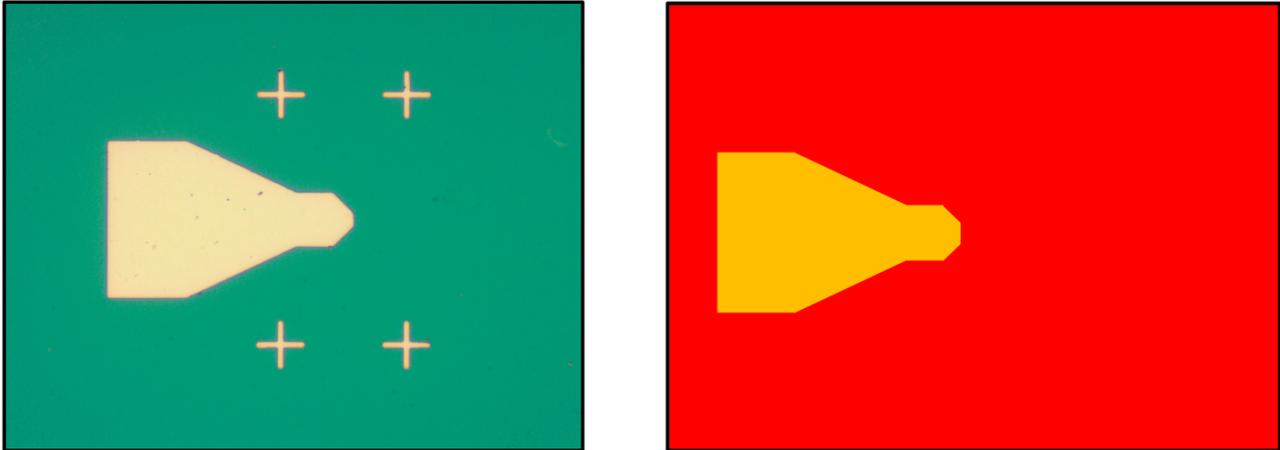


Figure 22: CNTs are deposited first and then the gold bottom electrode on top. Left picture shows the SEM image and right shows the schematic with red being CNTs and yellow being Au.

Next step is the deposition of the ring ohmic contact comprised of 30 nm of Palladium, 15 nm of Platinum and 50 nm of Gold. Platinum is used as a diffusion barrier for the high temperature oxygen plasma that follows next. The lithography was made with e-beam and a positive resist was used as a bi-layer called PMMA.

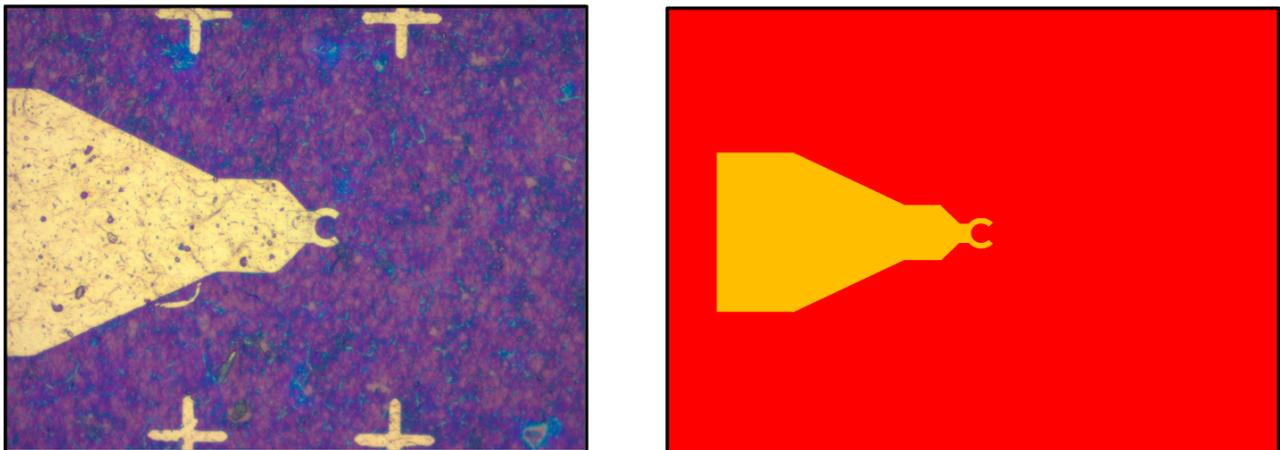


Figure 23: The ring ohmic contact made out of Pd/Pt/Au. Left picture shows the SEM image and right shows the schematic with red being CNTs and yellow being Au.

After the ring contact deposition, O₂ Plasma was used to clean the device of CNTs and then rapid thermal annealing at 300°C for 10 minutes followed to create CNT mesas leaving CNTs only in the area of the contacts.

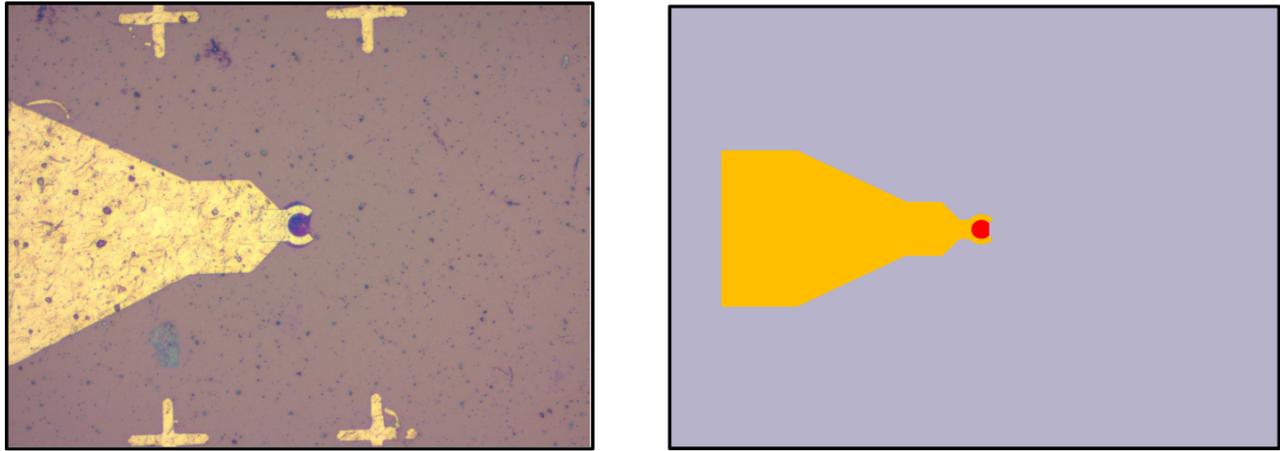


Figure 24: CNTs mesa is created leaving CNTs only on the contacts region. Left picture shows the SEM image and right shows the schematic with red being CNTs, yellow being Au and indigo being the SiO₂ substrate.

The next step includes the deposition of 20 nm of ICBA and of the top contact on top of ICBA comprised of 20 nm of Palladium and 30 nm of Gold or the other case had 20 nm of Aluminum and 30 nm of Gold. The lithography used was e-beam lithography and with a bi-layer of the positive resist PMMA mentioned earlier.

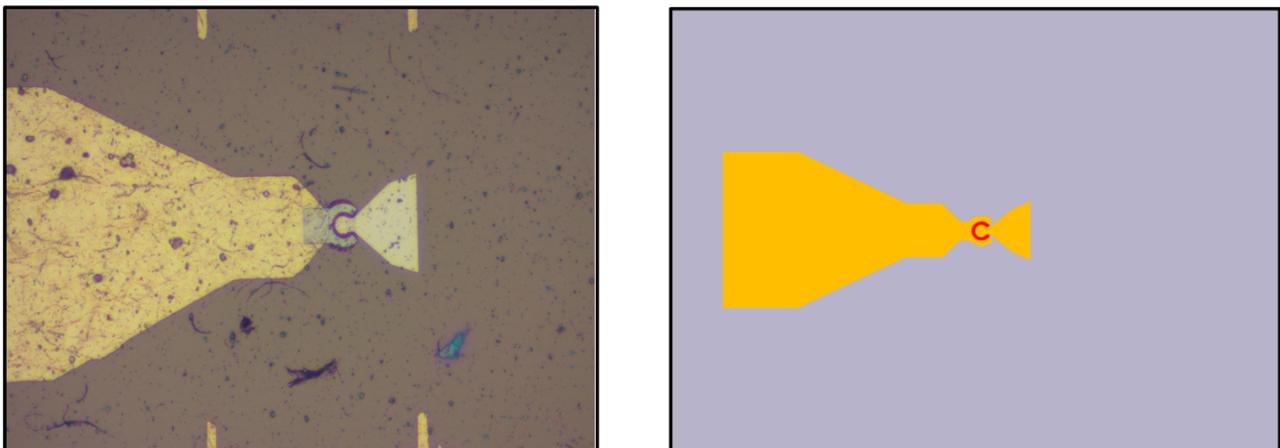


Figure 25: Top electrode deposited on top of ICBA. Left picture shows the SEM image and right shows the schematic with red being CNTs, yellow being Au and indigo being the SiO₂ substrate.

The last step is shown below where the coplanar waveguide was fabricated with 2 nm of Chromium and 500 nm of Gold along with a metal ground surrounding the device fabricated above. The lithography was optical and the same negative resist AZ2020 nLOF as in the first step was used. This piece of metal is called coplanar waveguide because in combination with the capacitance created due to the ground metal left and right of the waveguide and the inductance along the waveguide, an impedance is created; about 50 Ω in our case, making it suitable for integration. The optical image and the schematic is shown below.

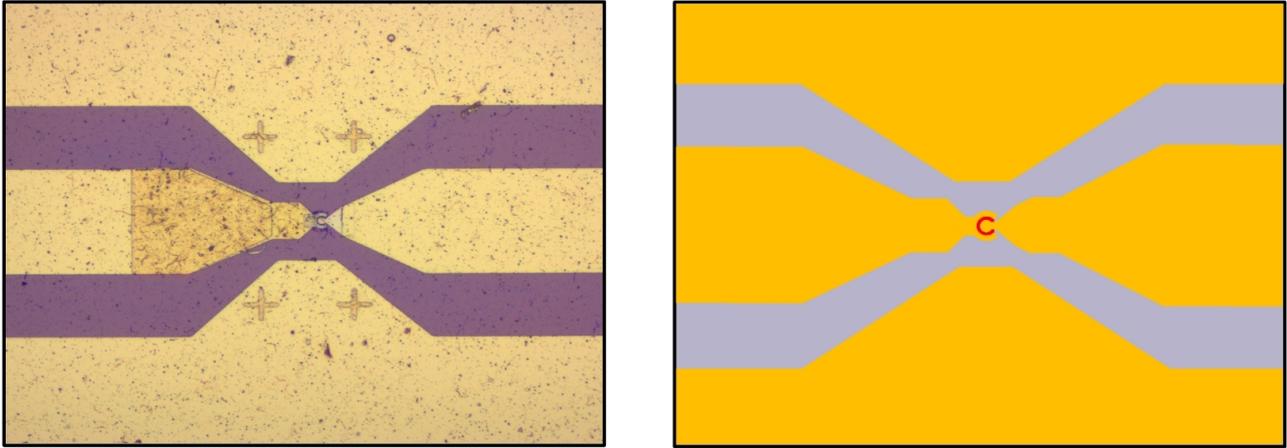


Figure 26: Coplanar waveguide deposited make the device complete. Left picture shows the SEM image and right shows the schematic with red being CNTs, yellow being Au and indigo being the SiO₂ substrate.

Last, in order to make it easier for the reader to understand the configuration of the various metals and semiconductors a three-dimensional schematic of the contact area was drawn as seen in Figure 27 below.

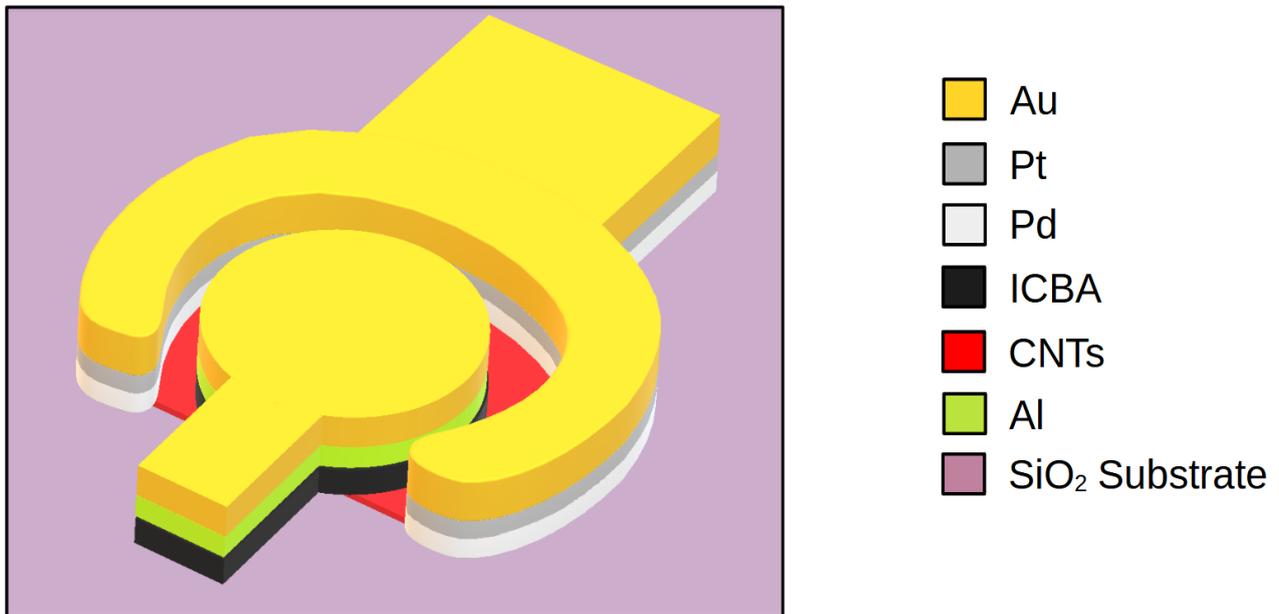


Figure 27: 3D schematic of the contact area. Each color corresponds to a material.

3.2 TLM measurements

In order to understand the role that each material plays in our experiment, a useful practice is to create separated devices in a TLM configuration. We created four types of devices all including the metal pads and the carbon nanotubes, so for the reader's convenience we name them as follows: CNTs only (Figure 28a), CNTs/ICBA (Figure 28b), CNTs/ICBA/PTCK₄ (Figure 28c) and CNTs/PTCK₄ (Figure 28d).

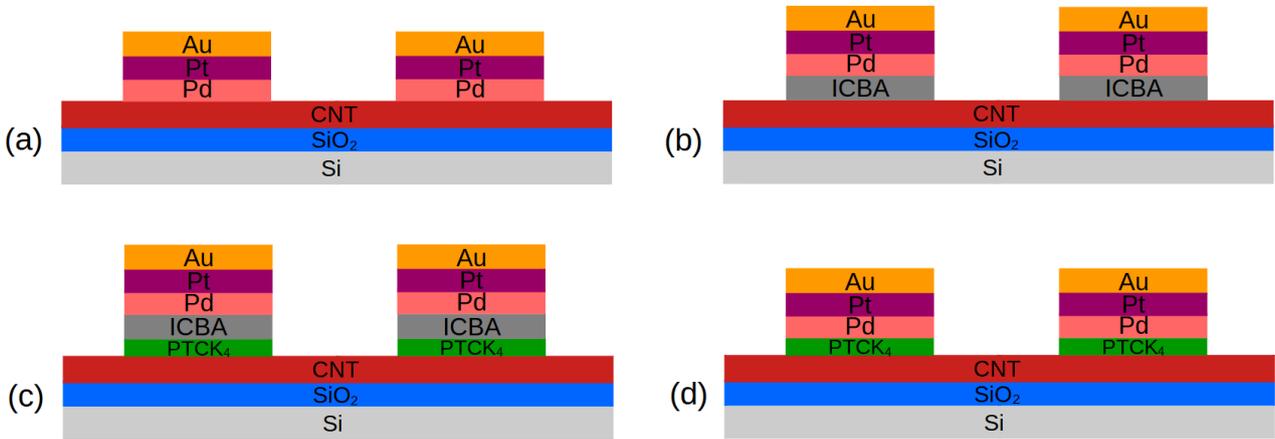


Figure 28: Schematic of the four different TLM configurations: (a) CNTs only, (b) CNTs & ICBA, (c) CNTs, ICBA & PTCK₄ and (d) CNTs & PTCK₄

The timeline in which the devices were processed was the following:

1. The fabrication was completed with all the materials, but no annealing was yet done.
2. An annealing followed at 200°C for 5 minutes.
3. The samples were doped with extra PTCK₄ regardless of whether PTCK₄ was already in the devices i.e. cases (c) and (d) above.

In the following sections we will present a series of measurements including I-V characteristics in different voltages until the breakdown point in the cases after annealing and after doping, comparative I-V's in the same devices initially before annealing, after annealing and after PTCK₄ doping and finally quantitative measurements of the contact and sheet resistances.

The purpose of the TLM measurements was to extract the contact and the sheet resistances. The contact resistance is to see how good the interface of the metals and semiconductors is, i.e. the lower the better and the sheet resistance is really helpful in indicating if the doping process was successful or not; in our case the PTCK₄ doping. PTCK₄ doping was simply achieved by depositing the material on top of the carbon nanotubes. An illustrative example is shown below in Figure 29.

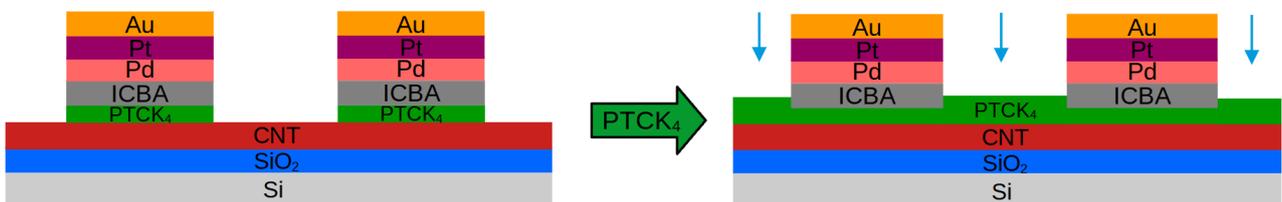


Figure 29: Schematic of the doping process with the PTCK₄.

3.2.1 First case: CNTs only

The first set of measurements are made in the devices comprised of carbon nanotubes and the metal pads as seen in Figure 22a. Initially, I-V characteristics are presented in the state after annealing in Figure 30 and after doping in Figure 31.

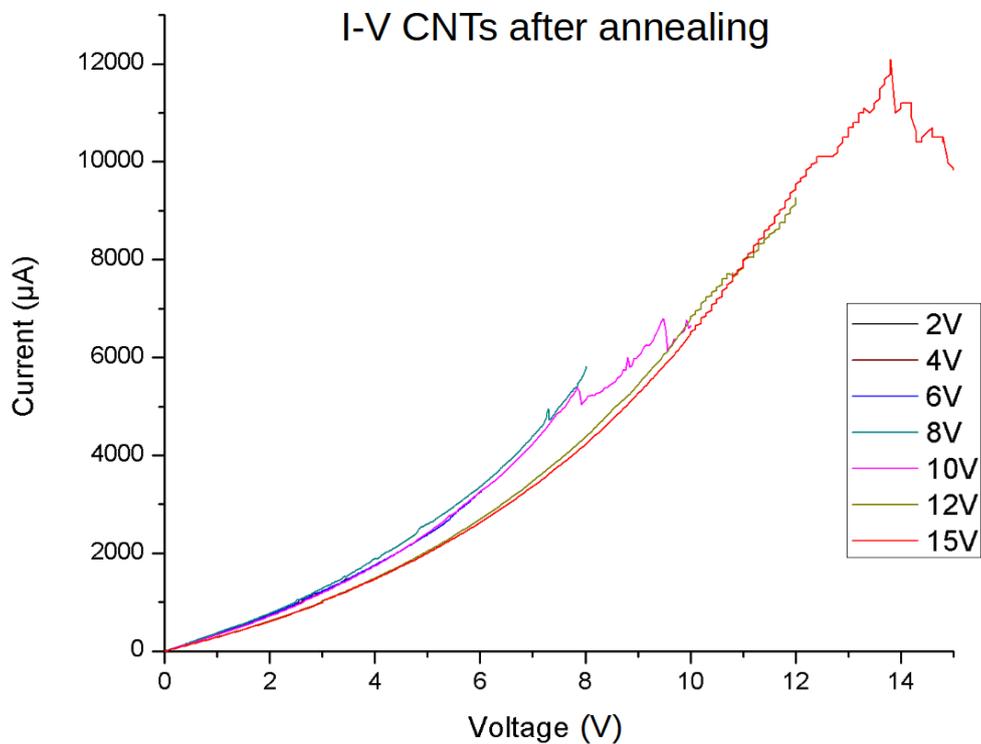


Figure 30: I-V characteristics with CNTs only after annealing.

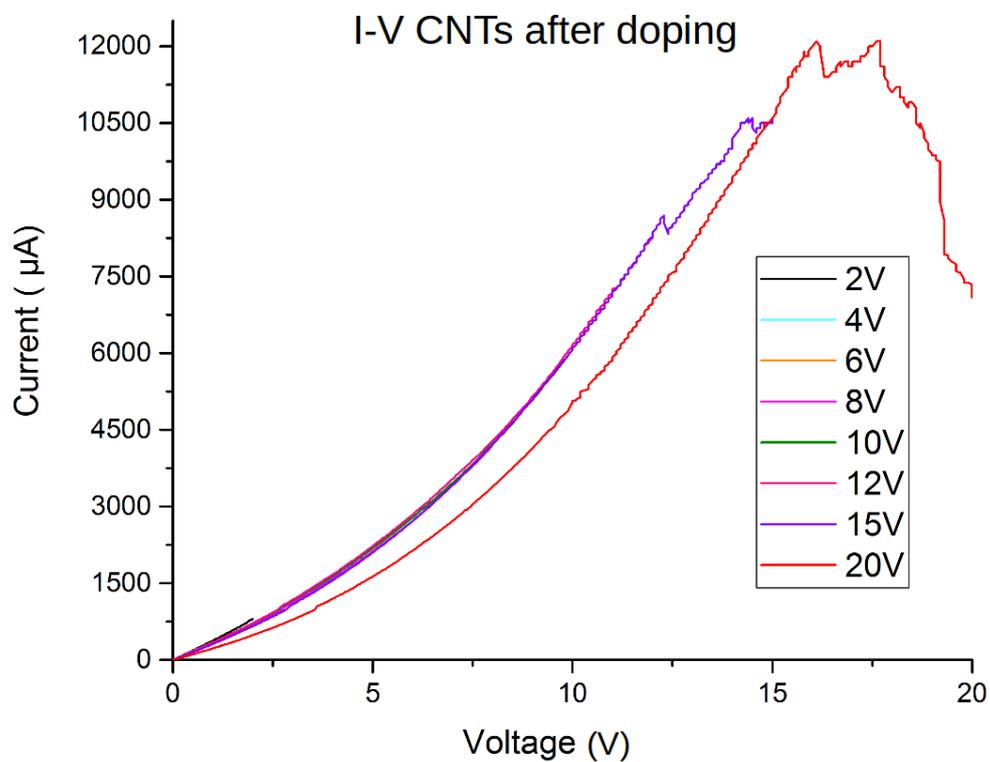


Figure 31: I-V characteristics with CNTs only after doping.

From the figures above we can observe that PTCK₄ doping has given the device an extra 5.1 Volts until it breaks down and degrade the device entirely. More specifically, the breakdown in the first case occurs at 7.2 Volts while in the second case there is an increase at around 12.3 Volts. Moreover, it is evident in both cases that after the breakdown occurs, there is a slight decrease in the currents in the next voltage sweeps, probably due to the fact that some CNTs may be degraded in high current densities.

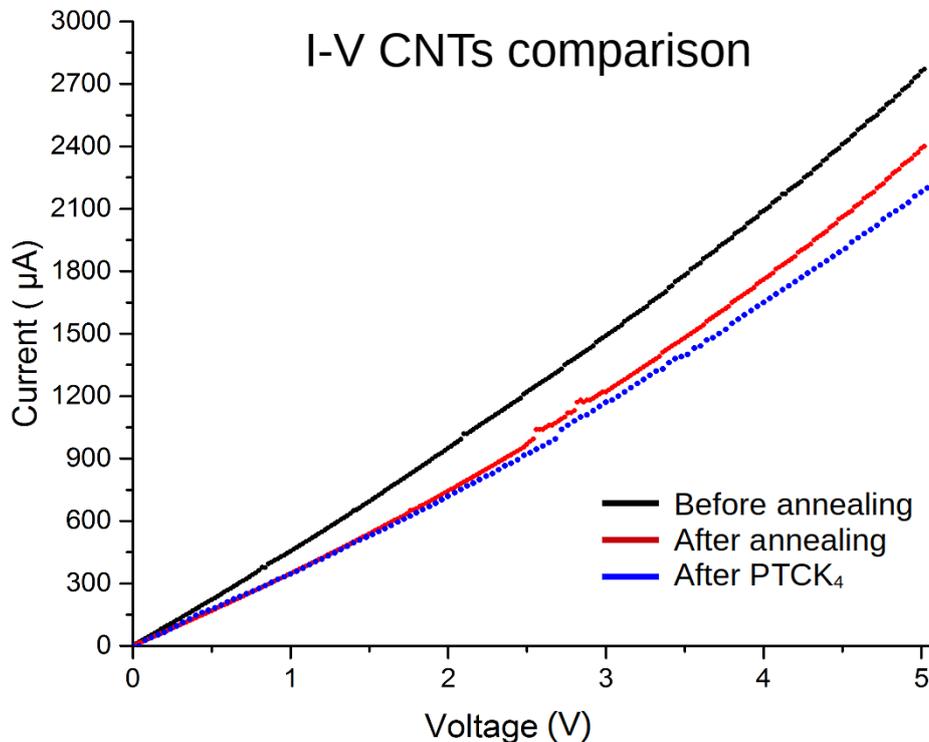


Figure 32: Comparison of I-V characteristics of CNTs devices between the three processing steps.

In Figure 32 there is a comparison of the current-voltage characteristics seeing the effect of each step. Here, both annealing and PTCK₄ doping decreased the current in the device, therefore increased the resistance. Also here and even more in the previous graphs, a non-linearity is observed indicating a diode-like behavior. Nevertheless, TLM configuration is consisted of two back-to-back diodes, therefore it is not easy to draw conclusions about the rectification capabilities of our device. This problem will be discussed later in Section 3.3 where plots of forward and reverse current will be presented.

3.2.2 Second case: CNTs/ICBA

The second set of measurements of the device include carbon nanotubes and Indene-C₆₀ Bisadduct. Below can be seen the I-V characteristics after annealing and after PTCK₄ doping in Figure 33 and Figure 34, respectively.

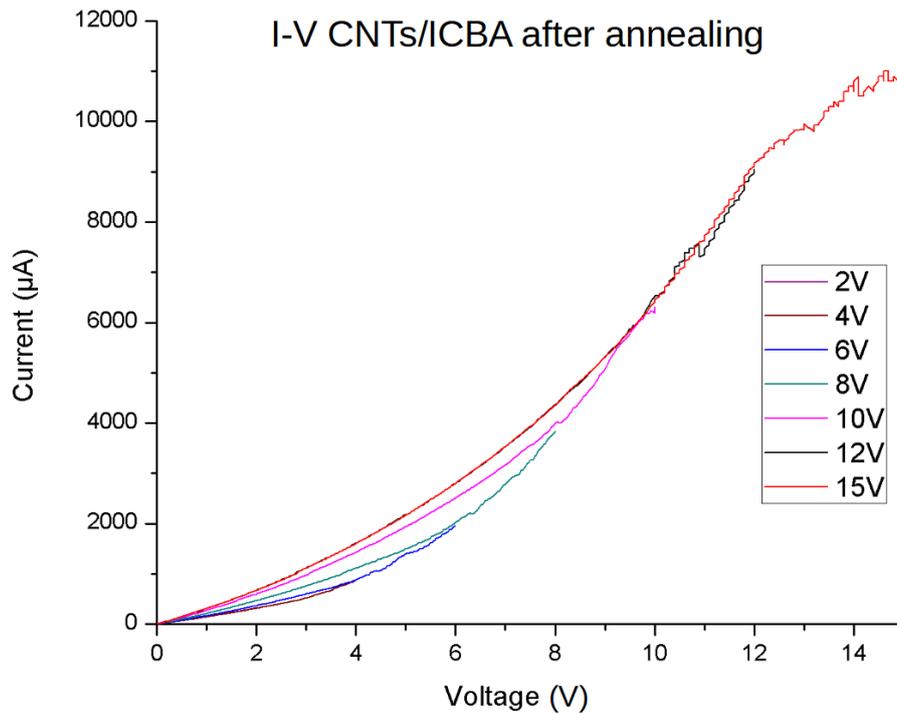


Figure 33: I-V characteristics with CNTs & ICBA after annealing.

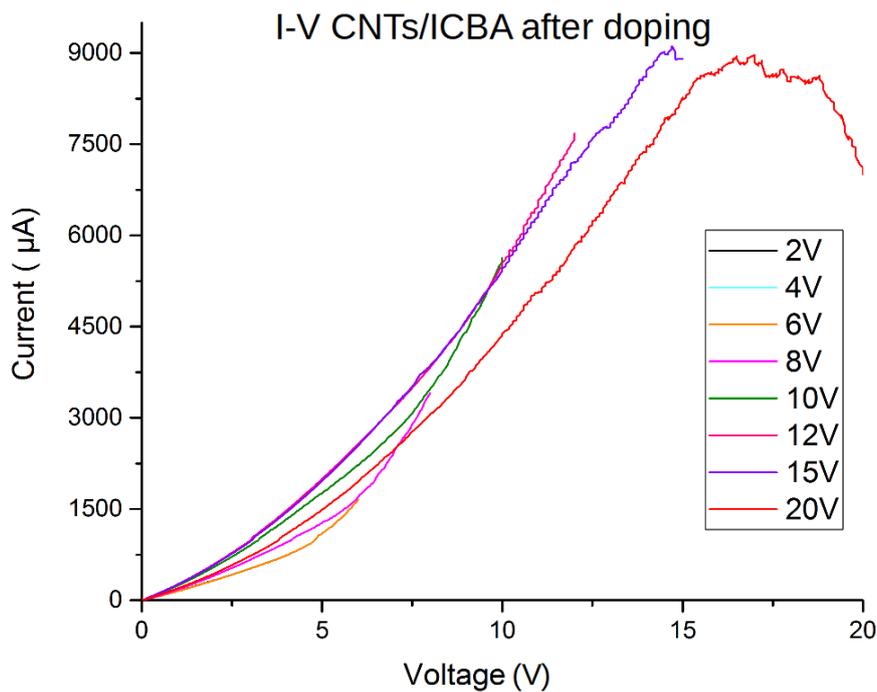


Figure 34: I-V characteristics with CNTs & ICBA after doping.

The figures above show something that we did not observe in the previous case. As the voltage maximum increases, the characteristic changes with every sweep. A similar result as before is observed in the sense of varying current, though now the breakdown has not yet happened and the current increases instead of decreasing. This phenomenon is probably explained as contact annealing where due to high current density near the contacts, the physical structure of the contact is altered, probably that of ICBA since the response was not observed in the first case. Another conclusion is that the maximum current that the device can reach, has decreased significantly after

the doping compared to the annealing case, i.e. before doping. Here, the breakdown shift is inconclusive.

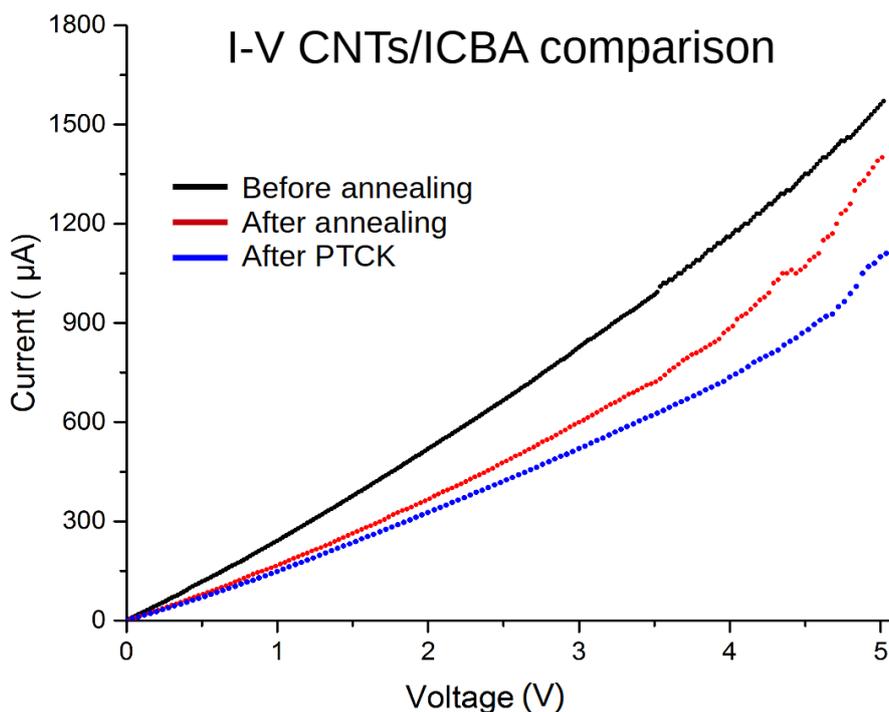


Figure 35: Comparison of I-V characteristics of CNTs & ICBA devices between the three processing steps.

In Figure 35, a comparison is again made resulting in the same picture as before. Annealing and PTCK₄ doping seem to have made the device less conductive.

3.2.3 Third case: CNTs/ICBA/PTCK₄

The third case consists of carbon nanotubes, Indene-C₆₀ Bisadduct and PTCK₄.

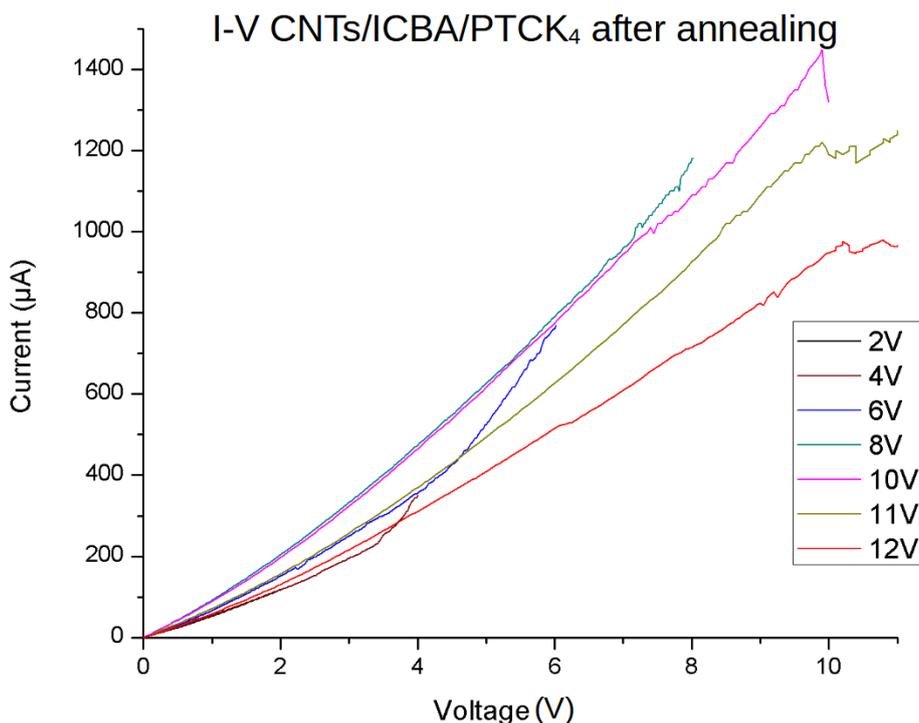


Figure 36: I-V characteristics with CNTs, ICBA & PTCK₄ after annealing.

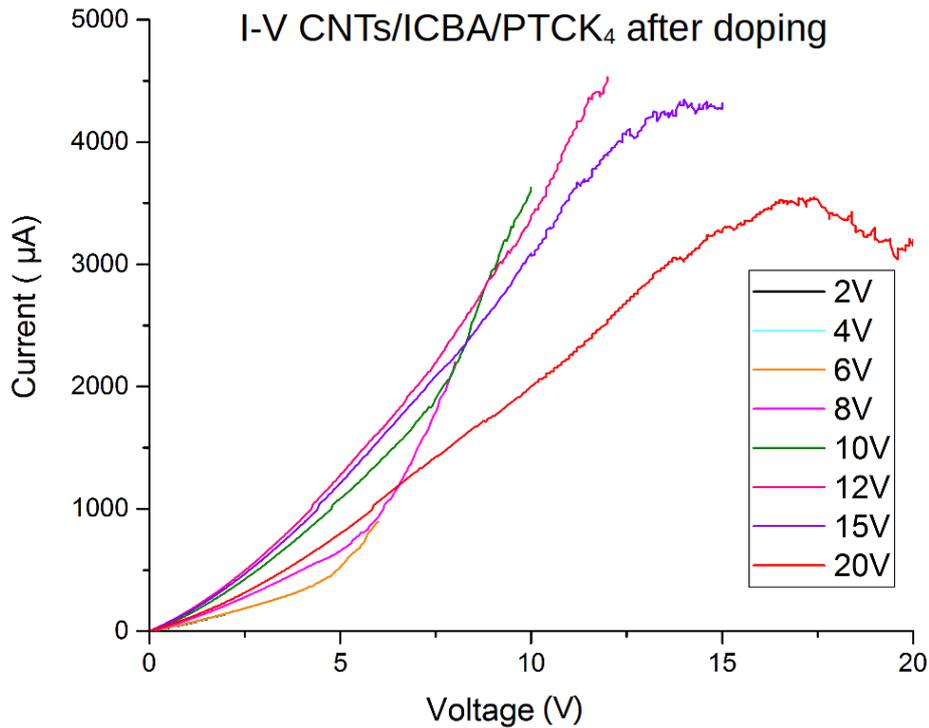


Figure 37: I-V characteristics with CNTs, ICBA & PTCK₄ after doping.

In Figure 36 and Figure 37, the same phenomenon as before is observed where the current increases as the voltage maximum increases to the point where breakdown occurs. What is interesting about this case is that after doping the current maximum almost tripled, indicating better interface and an altered Schottky barrier between CNTs, ICBA and PTCK₄. The breakdown here increased 1.9 Volts after doping compared to the annealing case, i.e. 9.9 Volts after annealing and 11.8 Volts after doping. Contact annealing is again observed.

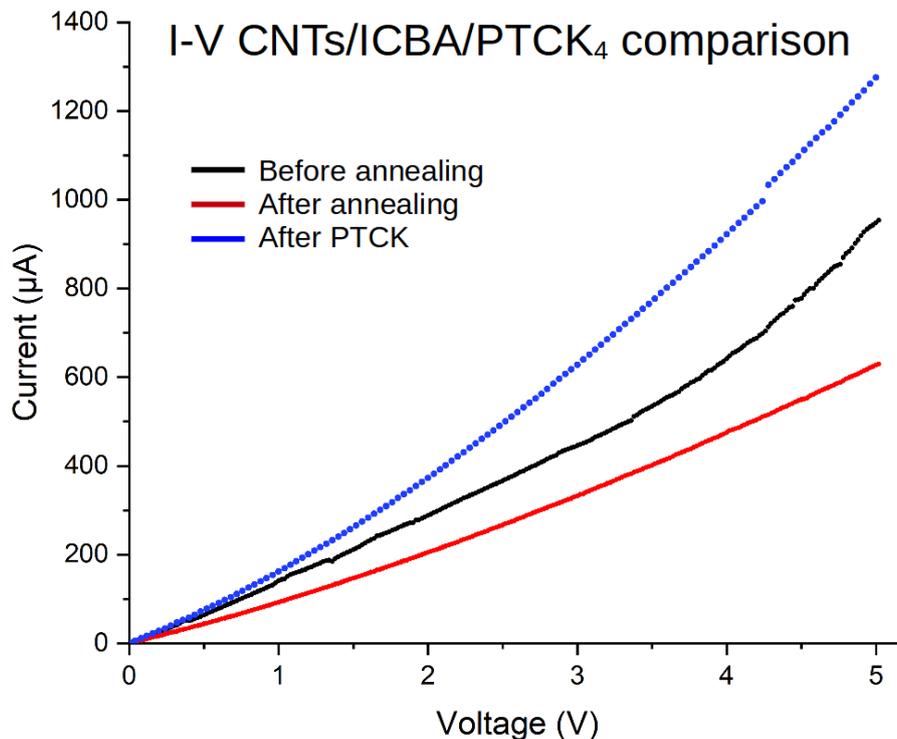


Figure 38: Comparison of I-V characteristics of CNTs, ICBA & PTCK₄ devices between the three processing steps.

This case from all four cases is the most interesting. In Figure 38 it can be seen that the characteristic after $PTCK_4$ doping surpasses both the lines from after and before annealing indicating that the doping mechanism of $PTCK_4$ between ICBA and CNTs acts in a favorable way; a conclusion that confirms the previous result of Figures 30 and 31.

3.2.4 Fourth case: CNTs/ $PTCK_4$

The fourth and last case includes samples with carbon nanotubes and $PTCK_4$.

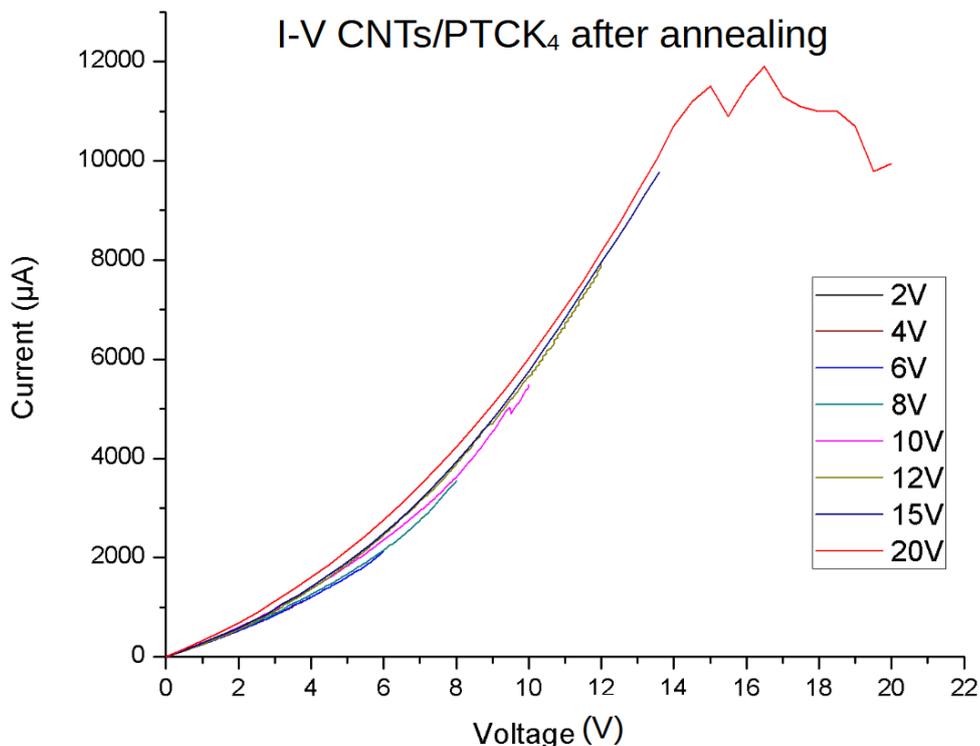


Figure 39: I-V characteristics with CNTs & $PTCK_4$ after annealing.

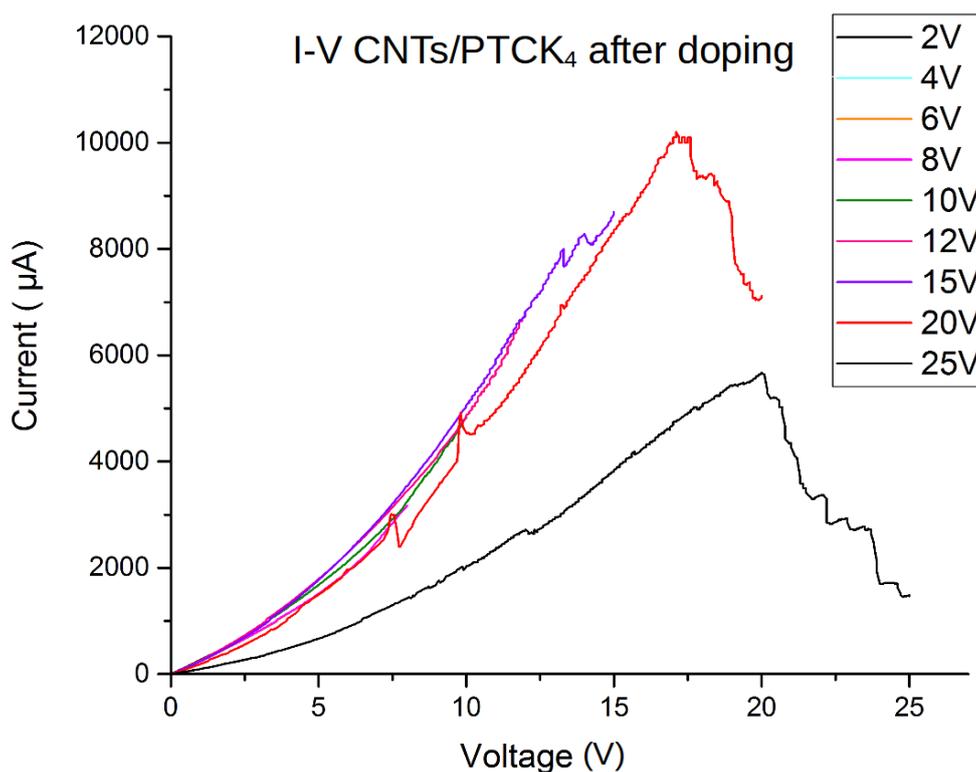


Figure 40: I-V characteristics with CNTs & $PTCK_4$ after doping.

In Figure 39 and Figure 40 a similar picture is observed as the first case where only CNTs were deposited on the device. A small contact annealing is observed again as in the cases two and three with ICBA but on a smaller scale. Furthermore, in this configuration (unlike cases one and three) a decrease in breakdown voltage was noticed of about 1.5 Volts. More specifically, after annealing the breakdown voltage was about 14.8 Volts and after doping it dropped to 13.3 Volts

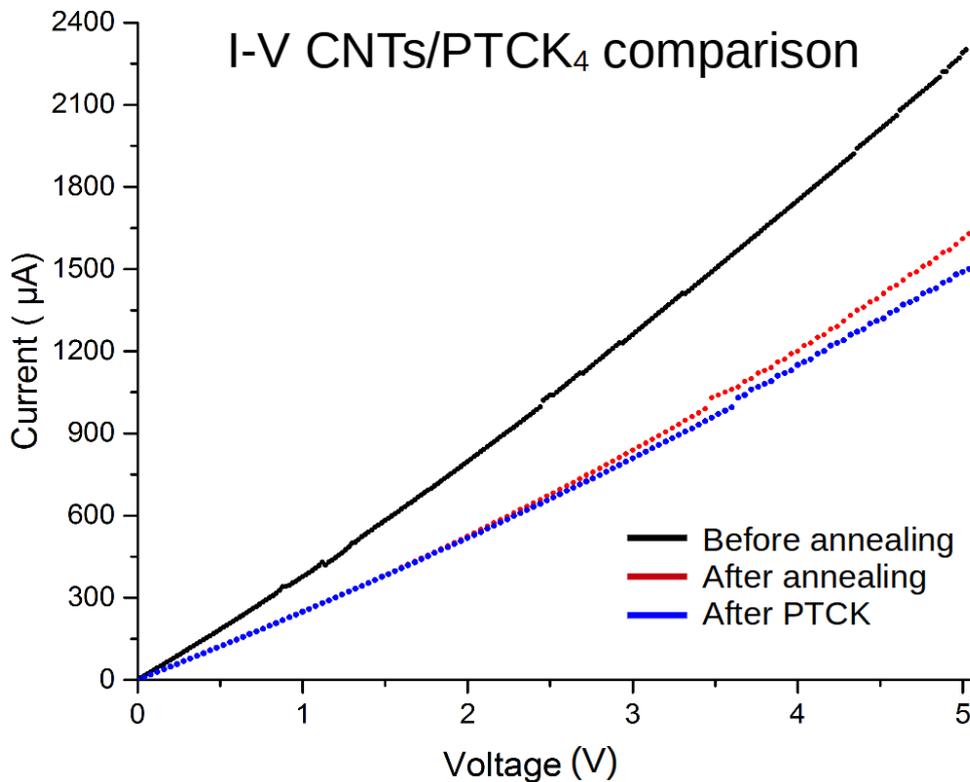


Figure 41: Comparison of I-V characteristics of CNTs & PTCK₄ devices between the three processing steps

In Figure 41, we get an almost identical image as in the first and second case except the fact that after annealing and after doping the two lines are following a similar path meaning that without the presence of ICBA there is not much of an effect on the CNTs; on the contrary the device conducts less current.

To summarize, the conclusion that can be drawn overall is that when PTCK₄ is deposited between ICBA and CNTs, there is a significant effect leading to the assumption that PTCK₄ indeed causes doping on either ICBA or CNTs. More experiments are required however to fully understand how PTCK₄ affects each material.

3.2.5 Contact & Sheet Resistances

	CNTs		CNTs/ICBA		CNTs/ICBA/PTCK ₄	CNTs/PTCK ₄
	R _C (Ω)	R _{SH} (kΩ)	R _C (Ω)	R _{SH} (kΩ)	R _C (Ω)	R _C (Ω)
Before annealing	110 ± 170	92 ± 3	560 ± 460	100 ± 2	2500 ± 500	-250 ± 290
After annealing	-5900 ± 2700	340 ± 19	4000 ± 2500	290 ± 10	3800 ± 1100	-3800 ± 3200
After doping	300 ± 600	110 ± 5	3400 ± 500	110 ± 3	4400 ± 4300	1500 ± 900

The table above contains the contacts resistances extracted from TLM for all the four cases in all three steps: before and after annealing and after PTCK₄ doping. Also, the sheet resistances for CNTs and CNTs/ICBA cases are given.

At first glance, one can see that the errors are comparable or sometimes even higher than the value of the resistance itself. This means that the conclusion, if there is any, has to be drawn after more experiments are done to verify the effect. First of all, there is a trend, almost in every case except the CNTs/ICBA/PTCK₄ case, where the contact resistance is small, then increases after annealing (at least in an absolute value) and then reduces again after doping. This response is associated with the reduction of doping due to residues on the CNTs (after annealing) and subsequent doping effect.

Since the effect of the PTCK₄ under the contacts is unclear we have not used it to fabricate rectifying diodes at this point.

3.3 Diode I-V measurements

Following fabrication of the asymmetric diodes described previously, the Current-Voltage characteristics were measured and the results are presented below along with the corresponding energy levels of the materials in Figure 42. Three different areas were measured to see the effect that each material has in the I-V characteristic.

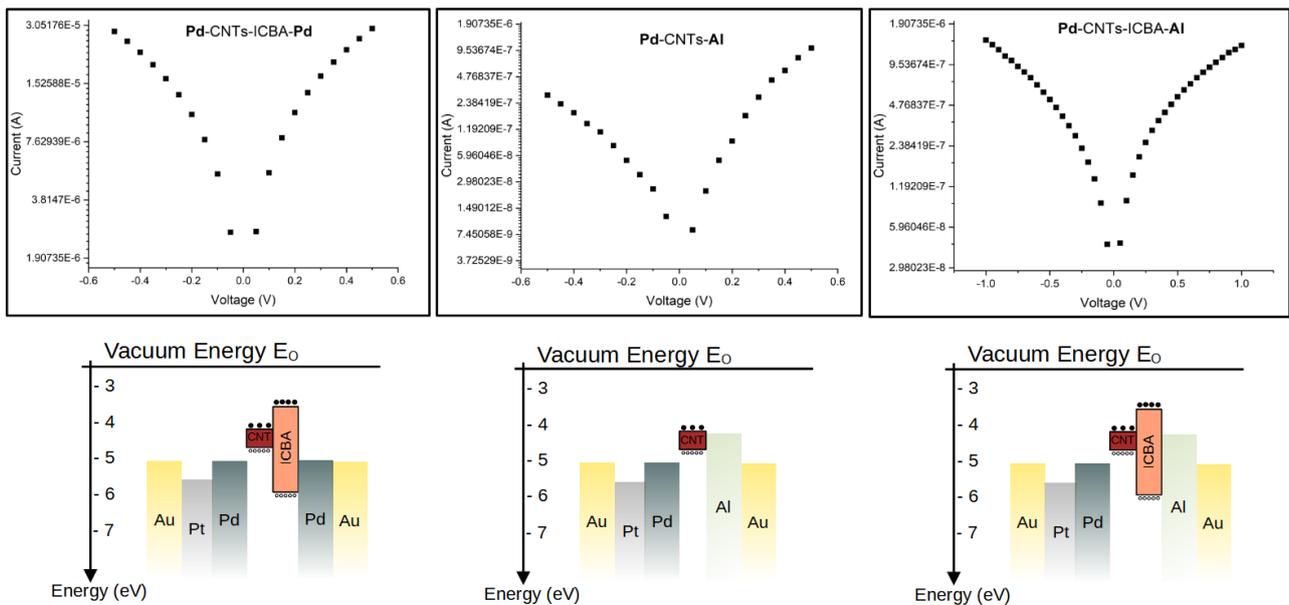


Figure 42: I-V characteristics on top with the corresponding Energy Levels: the first area is Pd-CNTs-ICBA-Pd (left), the second area is Pd-CNTs-Al (middle) and the third area is Pd-CNTs-ICBA-Al (right).

Initially, a measurement was taken with Palladium contacts symmetrically deposited around the CNTs/ICBA layers. The result is a fully symmetric Current response that is a result of the symmetric metal contacts.

Nevertheless, this was not the case for the other two device types. By replacing one of the contacts with Aluminum, two effects are noticed:

- 1) an asymmetry was observed meaning that a diode has formed
- 2) A significant reduction of the overall current is shown.

Hence the device is at least partially rectifying. In Figure 43, a comparison of the three devices is presented.

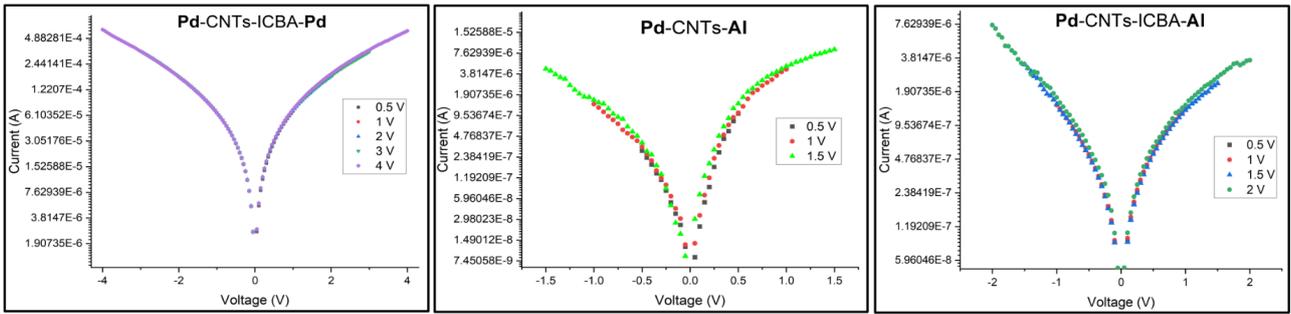


Figure 43: I-V characteristics to check the stability of each device on different sweeps.

Figure 43 above shows the stability of each device by doing different sweeps of voltage starting from 0.5 V on each case. It is evident that in the first case of Pd-CNTs-ICBA-Pd each curve retraces after every sweep meaning that there is high stability in this device. On the other hand, there is a slight mismatch in re-tracing on the other two cases.

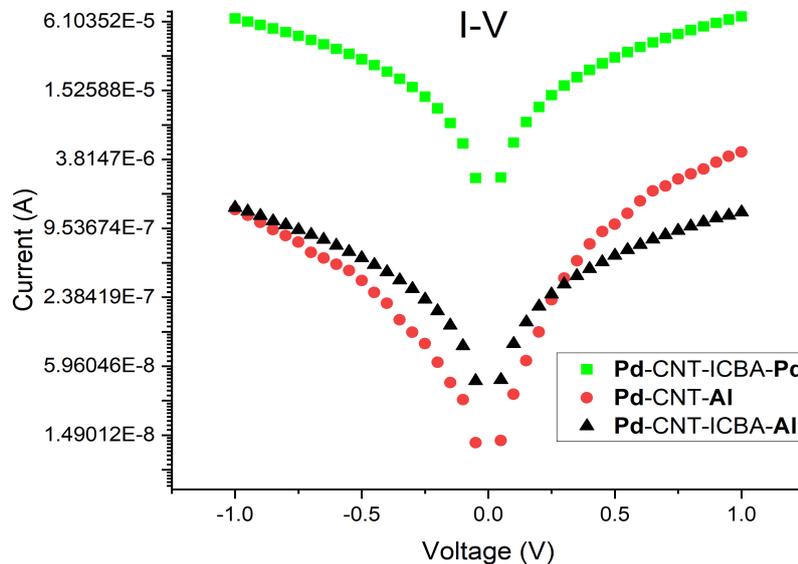


Figure 44: A comparison between the three different devices: i) Pd-CNTs-ICBA-Pd (green), ii) Pd-CNTs-Al (red) and iii) Pd-CNTs-ICBA-Al (black).

As can be seen here, one conclusion that can be drawn is that the Aluminum electrode is responsible for the large current reduction (about 10^2 times lower) we see compared to Palladium (from green to red & black).

The Aluminum case is asymmetric with higher current in the positive voltage branch whereas the ICBA / Al case exhibits higher currents in the negative current branch. Two effects can be identified here. The CNTs are natively p-type and the ICBA is natively n-type. This is consistent with the CNT/ICBA response. For the asymmetry in the pure CNT case one can only assume that Al has an opposite effect on the CNT band alignment. It is important to note that passing current through the Pd-CNT-Al rapidly changes the device response. On the contrary, multiple sweeps of the CNT/ICBA device result in no change.

3.4 High Frequency measurements

An initial attempt to measure the high frequency characteristics of the resulting diode was made. To properly de-convolve the effect of the coplanar transmission line, a device without the diode was measured. This is shown in Figure 45. The transmission line was simulated using QUCS software using the simple circuit that is shown below.

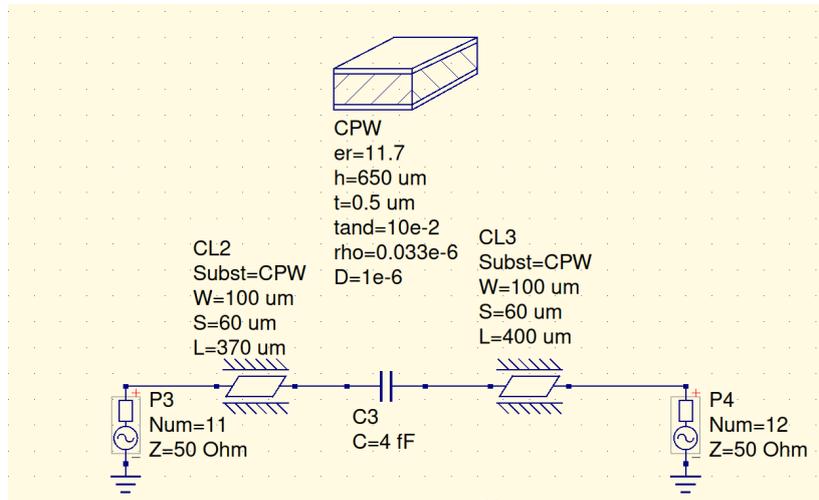


Figure 45: The QUCS circuit used to simulate the coplanar T-line system. The center capacitor is the parasitic capacitance between electrodes.

And the resulting data compared with the measured data are shown here:

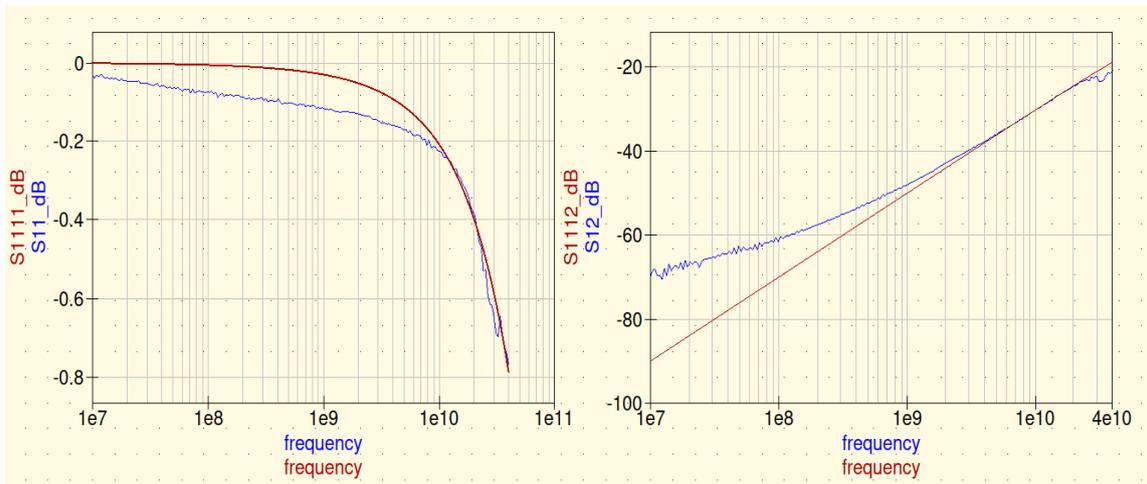


Figure 46: Reflection (left) and Transmission (right) of the reference CPW structure. The brown curve denote the simulated curves using the circuit in Figure 44.

Finally, the actual Pd/CNT/ICBA/Al device response is shown below along with the simulated data to be discussed.

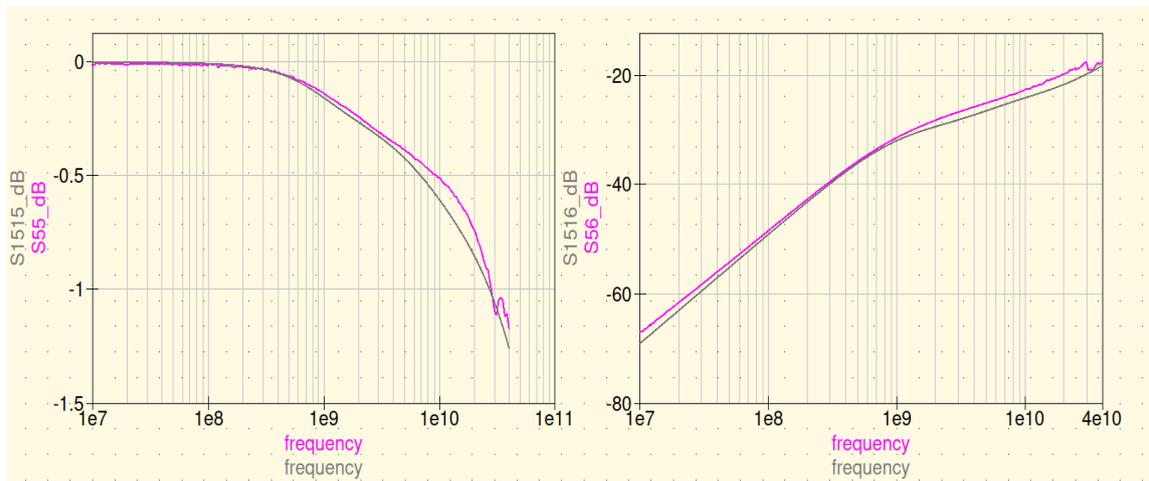


Figure 47: Reflection (left) and Transmission (right) of the Diode device. The black curve denote the simulated curves using the circuit in Figure 44.

The simulated response is calculated using the circuit shown below. The diode is simulated by 2 branches that contain a Capacitance in series with a resistance that is added to the initial circuit shown in Figure 45 previously. The exact origin of the capacitance / resistance requires better understanding of the device and more detailed simulation but we may assume that the 6 fF branch could be a parasitic capacitance originating from the top electrode in relation to the bottom electrode. Then the 45 fF branch is probably originating from the diode itself. Indeed if we assume $R = 4 \mu\text{m}$ (the design circle), $d = 20 \text{ nm}$ (The ICBA thickness) and an $\epsilon_r \sim 2.2$ [62] (The ICBA permittivity) we calculate a capacitance of 48 fF that is nearly identical to the result from the simulation.

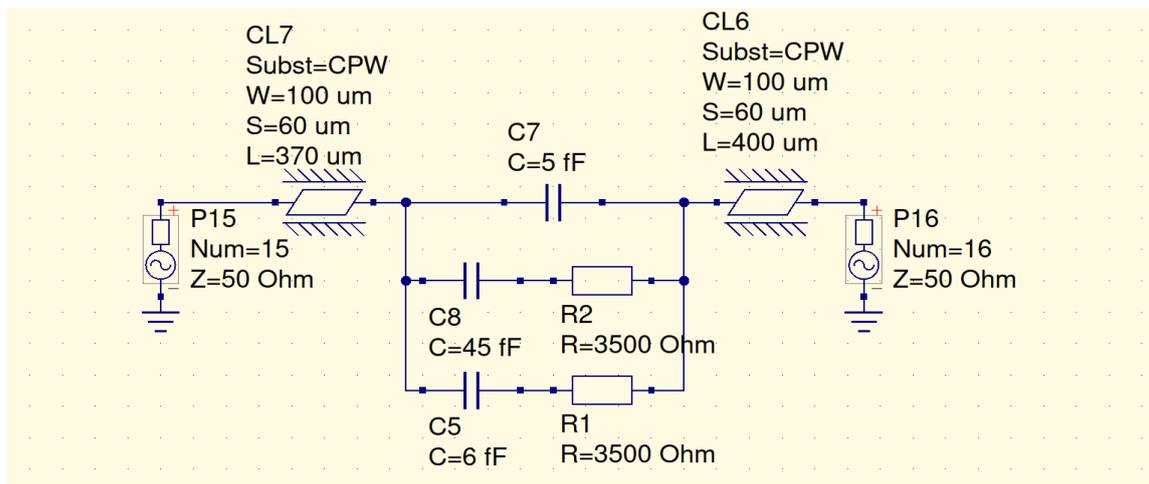


Figure 48: The QUCS circuit used to simulate the above curves of Reflection and Transmission.

3.5 Conclusions

Rectifying action has been shown using a combination of CNT and ICBA fullerenes. Several key issues still need to be carefully examined such as the effect of doping with $PTCK_4$ that we verified that has an effect on CNTs but did not incorporate into the diode structures due to time limitations. The rectifying behavior is consistent with the native doping character of both CNTs and Fullerene derivative ICBA and this is a further indication that the response originates from that system. The reference CNT/Al structure in fact exhibits opposite rectification characteristics.

It is interesting, as a future work to study the Temperature dependence of the diode characteristics that will allow us to extract useful parameters such as the Schottky barrier, the ideality factor, the series Resistance and the Richardson constant (see Section 1.4.3) and to further understand the high frequency operation of the diode including measuring the rectification as a function of frequency.

- End of Chapter 3 -

Bibliography

- [1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, Art. no. 8, 1965.
- [2] N. Baig, I. Kammakakam, and W. Falath, "Nanomaterials: a review of synthesis methods, properties, recent progress, and challenges," *Mater. Adv.*, vol. 2, no. 6, Art. no. 6, 2021, doi: 10.1039/D0MA00807A.
- [3] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 453, no. 6348, Art. no. 6348, 1991, doi: 10.1038/354056a0.
- [4] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon Nanotubes as Schottky Barrier Transistors," *Phys. Rev. Lett.*, vol. 89, no. 10, Art. no. 10, 2002, doi: 10.1103/PhysRevLett.89.106801.
- [5] M. Schroter, M. Claus, P. Sakalas, M. Haferlach, and D. Wang, "Carbon Nanotube FET Technology for Radio-Frequency Electronics: State-of-the-Art Overview," *IEEE J. Electron Devices Soc.*, vol. 1, no. 1, Art. no. 1, 2013, doi: 10.1109/JEDS.2013.2244641.
- [6] J. U. Lee, P. P. Gipp, and C. M. Heller, "Carbon nanotube *p-n* junction diodes," *Appl. Phys. Lett.*, vol. 85, no. 1, Art. no. 1, 2004, doi: 10.1063/1.1769595.
- [7] M. S. Dresselhaus, G. Dresselhaus, and P. Avouris, Eds., "Carbon Nanotubes. Synthesis, Structure and Applications," vol. 80, Springer, 2001.
- [8] C. N. R. Rao, R. Voggu, and A. Govindaraj, "Selective generation of single-walled carbon nanotubes with metallic, semiconducting and other unique electronic properties," *Nanoscale*, vol. 1, no. 1, Art. no. 1, 2009, doi: 10.1039/B9NR00104B.
- [9] X. Lu and Z. Chen, "Curved Pi-Conjugation, Aromaticity, and the Related Chemistry of Small Fullerenes (<C60) and Single-Walled Carbon Nanotubes," *Chem. Rev.*, vol. 105, no. 10, Art. no. 10, 2005, doi: 10.1021/cr030093d.
- [10] S. Hong and S. Myung, "A flexible approach to mobility," *Nat. Nanotechnol.*, vol. 2, no. 4, Art. no. 4, 2007, doi: 10.1038/nnano.2007.89.
- [11] G. Y. Guo, K. C. Chu, D. Wang, and C. Duan, "Linear and nonlinear optical properties of carbon nanotubes from first-principles calculations," *Phys. Rev. B*, vol. 69, p. 205416, 2004, doi: 10.1103/PhysRevB.69.205416.
- [12] S. Sinha, S. Barjami, G. Iannacchione, A. Schwab, and G. Muench, "Off-axis thermal properties of carbon nanotube films," *J. Of Nanoparticle Res.*, vol. 7, no. 6, Art. no. 6, 2005, doi: 10.1007/s11051-005-8382-9.
- [13] B. Peng, M. Locascio, P. Zapol, S. Li, S. L. Mielke, and H. D. Espinosa, "Measurements of near-ultimate strength for multiwalled carbon nanotubes and irradiation-induced crosslinking improvements," *Nat. Nanotechnol.*, vol. 3, no. 10, Art. no. 10, 2008, doi: 10.1038/nnano.2008.211.
- [14] C. Delacou *et al.*, "Investigation of charge interaction between fullerene derivatives and single-walled carbon nanotubes," *InfoMat*, vol. 1, no. 4, pp. 559–570, Dec. 2019, doi: 10.1002/inf2.12045.
- [15] H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl, and R. E. Smalley, "C60: Buckminsterfullerene," *Nature*, vol. 318, no. 6042, Art. no. 6042, 1985, doi: 10.1038/318162a0.
- [16] R. Nakanishi, A. Nogimura, R. Eguchi, and K. Kanai, "Electronic structure of fullerene derivatives in organic photovoltaics," *Org. Electron.*, vol. 15, no. 11, pp. 2912–2921, Nov. 2014, doi: 10.1016/j.orgel.2014.08.013.
- [17] Y. He, H.-Y. Chen, J. Hou, and Y. Li, "Indene-C₆₀ Bisadduct: A New Acceptor for High-Performance Polymer Solar Cells," *J. Am. Chem. Soc.*, vol. 132, no. 4, pp. 1377–1382, Feb. 2010, doi: 10.1021/ja908602j.

- [18] N. B. Kotadiya, A. Mondal, P. W. M. Blom, D. Andrienko, and G.-J. A. H. Wetzelaer, “A window to trap-free charge transport in organic semiconducting thin films,” *Nat. Mater.*, vol. 18, no. 11, pp. 1182–1186, Nov. 2019, doi: 10.1038/s41563-019-0473-6.
- [19] R. W. Keyes, “Fundamental limits of silicon technology,” *Proc. IEEE*, vol. 89, no. 3, pp. 227–239, Mar. 2001, doi: 10.1109/5.915372.
- [20] Y. Yu. Illarionov *et al.*, “Insulators for 2D nanoelectronics: the gap to bridge,” *Nat. Commun.*, vol. 11, no. 1, p. 3385, Dec. 2020, doi: 10.1038/s41467-020-16640-8.
- [21] O. Zhou, H. Shimoda, B. Gao, S. Oh, L. Fleming, and G. Yue, “Materials Science of Carbon Nanotubes: Fabrication, Integration, and Properties of Macroscopic Structures of Carbon Nanotubes,” *Acc. Chem. Res.*, vol. 35, no. 12, pp. 1045–1053, Dec. 2002, doi: 10.1021/ar010162f.
- [22] M. J. Bronikowski, P. A. Willis, D. T. Colbert, K. A. Smith, and R. E. Smalley, “Gas-phase production of carbon single-walled nanotubes from carbon monoxide via the HiPco process: A parametric study,” *J. Vac. Sci. Technol. Vac. Surf. Films*, vol. 19, no. 4, pp. 1800–1805, Jul. 2001, doi: 10.1116/1.1380721.
- [23] T. Tanaka *et al.*, “Simple and Scalable Gel-Based Separation of Metallic and Semiconducting Carbon Nanotubes,” *Nano Lett.*, vol. 9, no. 4, pp. 1497–1500, Apr. 2009, doi: 10.1021/nl8034866.
- [24] H.-H. Cho, C.-H. Cho, H. Kang, H. Yu, J. H. Oh, and B. J. Kim, “Molecular structure-device performance relationship in polymer solar cells based on indene-C60 bis-adduct derivatives,” *Korean J. Chem. Eng.*, vol. 32, no. 2, pp. 261–267, Feb. 2015, doi: 10.1007/s11814-014-0220-2.
- [25] C. N. Murthy and K. E. Geckeler, “SOLUBILITY CORRELATION OF [60]FULLERENE IN DIFFERENT SOLVENTS,” *Fuller. Sci. Technol.*, vol. 9, no. 4, pp. 477–486, Aug. 2001, doi: 10.1081/FST-100107150.
- [26] M. M. Boorum, Y. V. Vasil’ev, T. Drewello, and L. T. Scott, “Groundwork for a Rational Synthesis of C60: Cyclodehydrogenation of a C60H30 Polyarene,” *Science*, vol. 294, p. 5, 2001, doi: 10.1126/science.1064250.
- [27] L. T. Scott, “A Rational Chemical Synthesis of C60,” *Science*, vol. 295, p. 5, 2002, doi: 10.1126/science.1068427.
- [28] K. Björkqvist and T. Arnborg, “Short Channel Effects in MOS-Transistors,” *Phys. Scr.*, vol. 24, no. 2, 1981, doi: 10.1088/0031-8949/24/2/016.
- [29] S. Veeraraghavan, “Short-Channel Effects in SOI MOSFET’s,” *IEEE J. Electron Devices Soc.*, vol. 36, no. 3, p. 7, 1989, doi: 10.1109/16.19963.
- [30] J. Knoch and J. Appenzeller, “Modeling of High-Performance p-Type III–V Heterojunction Tunnel FETs,” *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 305–307, Apr. 2010, doi: 10.1109/LED.2010.2041180.
- [31] J. Wu, J. Min, and Y. Taur, “Short-Channel Effects in Tunnel FETs,” *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3019–3024, Sep. 2015, doi: 10.1109/TED.2015.2458977.
- [32] R. R. Troutman, “VLSI Limitations from Drain-induced Lowering,” *IEEE Electron Device Lett.*, vol. 14, no. 2, pp. 383–391, 1979.
- [33] A. Valletta, L. Mariucci, G. Fortunato, and S. D. Brotherton, “Surface-scattering effects in polycrystalline silicon thin-film transistors,” *Appl. Phys. Lett.*, vol. 82, no. 18, pp. 3119–3121, May 2003, doi: 10.1063/1.1571960.
- [34] G. W. Ludwig and R. L. Watters, “Drift and Conductivity Mobility in Silicon,” *Phys. Rev.*, vol. 101, no. 6, pp. 1699–1701, Mar. 1956, doi: 10.1103/PhysRev.101.1699.
- [35] F. Gámiz, J. B. Roldán, P. Cartujo-Cassinello, J. E. Carceller, J. A. López-Villanueva, and S. Rodriguez, “Electron mobility in extremely thin single-gate silicon-on-insulator inversion layers,” *J. Appl. Phys.*, vol. 86, no. 11, pp. 6269–6275, Dec. 1999, doi: 10.1063/1.371684.

- [36] F. Schwierz, “Flat transistors get off the ground,” *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 135–136, Mar. 2011, doi: 10.1038/nnano.2011.26.
- [37] P. Avouris, “Graphene: Electronic and Photonic Properties and Devices,” *Nano Lett.*, vol. 10, no. 11, pp. 4285–4294, Nov. 2010, doi: 10.1021/nl102824h.
- [38] F. Schwierz, “Graphene transistors,” *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, Jul. 2010, doi: 10.1038/nnano.2010.89.
- [39] T. Dürkop, S. A. Getty, E. Cobas, and M. S. Fuhrer, “Extraordinary Mobility in Semiconducting Carbon Nanotubes,” *Nano Lett.*, vol. 4, no. 1, pp. 35–39, Jan. 2004, doi: 10.1021/nl034841q.
- [40] P. Avouris, Z. Chen, and V. Perebeinos, “Carbon-based electronics,” *Nanosci. Technol.*, vol. 2, pp. 174–184, 2009, doi: 10.1142/9789814287005_0018.
- [41] E. F. Oliveira, L. C. Silva, and F. C. Lavarda, “Modifying electronic properties of ICBA through chemical substitutions for solar cell applications,” *Struct. Chem.*, vol. 28, no. 4, pp. 1133–1140, Aug. 2017, doi: 10.1007/s11224-017-0916-0.
- [42] G.-J. A. H. Wetzelaer and P. W. M. Blom, “Electron and hole transport in solution-processed fullerenes,” *J. Mater. Chem. C*, vol. 9, no. 45, pp. 16068–16077, 2021, doi: 10.1039/D1TC90228H.
- [43] E. Orgiu *et al.*, “The dramatic effect of the annealing temperature and dielectric functionalization on the electron mobility of indene-C₆₀ bis-adduct thin films,” *Chem. Commun.*, vol. 51, no. 25, pp. 5414–5417, 2015, doi: 10.1039/C5CC00151J.
- [44] M. A. Deshmukh, S.-J. Park, B.-C. Kang, and T.-J. Ha, “Carbon Nanohybrids for Advanced Electronic Applications,” *Phys. Status Solidi A*, vol. 217, no. 17, p. 2000199, Sep. 2020, doi: 10.1002/pssa.202000199.
- [45] B. Ofuonye, J. Lee, M. Yan, C. Sun, J.-M. Zuo, and I. Adesida, “Electrical and microstructural properties of thermally annealed Ni/Au and Ni/Pt/Au Schottky contacts on AlGaIn/GaN heterostructures,” *Semicond. Sci. Technol.*, vol. 29, no. 9, p. 095005, Sep. 2014, doi: 10.1088/0268-1242/29/9/095005.
- [46] W. Shockley, “The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors,” *Bell Syst. Tech. J.*, vol. 28, no. 3, pp. 435–489, 1949, doi: 10.1002/j.1538-7305.1949.tb03645.x.
- [47] C. R. Crowell, “Richardson constant and tunneling effective mass for thermionic and thermionic-field emission in Schottky barrier diodes,” *Solid-State Electron.*, vol. 12, no. 1, pp. 55–59, Jan. 1969, doi: 10.1016/0038-1101(69)90135-X.
- [48] K. M. M. R. M. Y. and Z. M., “Two methods for extracting the parameters of a non-ideal diode,” *Int. J. Phys. Sci.*, vol. 10, no. 8, pp. 270–275, Apr. 2015, doi: 10.5897/IJPS2015.4260.
- [49] S. M. Sze and K. K. Ng, “p-n Junctions,” in *Physics of Semiconductor Devices*, 3rd ed., A John Wiley & Sons, Inc., Publication, 2006, pp. 77–133.
- [50] K. Ahmed and T. Chiang, “Schottky barrier height extraction from forward current-voltage characteristics of non-ideal diodes with high series resistance,” *Appl. Phys. Lett.*, vol. 102, no. 4, p. 042110, Jan. 2013, doi: 10.1063/1.4789989.
- [51] J. Zhang, Y. Li, B. Zhang, H. Wang, Q. Xin, and A. Song, “Flexible indium–gallium–zinc–oxide Schottky diode operating beyond 2.45 GHz,” *Nat. Commun.*, vol. 6, no. 1, p. 7561, Nov. 2015, doi: 10.1038/ncomms8561.
- [52] S. K. Cheung and N. W. Cheung, “Extraction of Schottky diode parameters from forward current-voltage characteristics,” *Appl. Phys. Lett.*, vol. 49, no. 2, pp. 85–87, Jul. 1986, doi: 10.1063/1.97359.
- [53] C. Kenney, K. C. Saraswat, B. Taylor, and P. Majhi, “Thermionic Field Emission Explanation for Nonlinear Richardson Plots,” *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2423–2429, Aug. 2011, doi: 10.1109/TED.2011.2156411.

- [54] S. Aftab *et al.*, “Van der Waals Multi-Heterostructures (PN, PIN, and NPN) for Dynamic Rectification in 2D Materials,” *Adv. Mater. Interfaces*, vol. 7, no. 24, p. 2001479, Dec. 2020, doi: 10.1002/admi.202001479.
- [55] A. Pelella, A. Grillo, E. Faella, G. Luongo, M. B. Askari, and A. Di Bartolomeo, “Graphene–Silicon Device for Visible and Infrared Photodetection,” *ACS Appl. Mater. Interfaces*, vol. 13, no. 40, pp. 47895–47903, Oct. 2021, doi: 10.1021/acsaami.1c12050.
- [56] M. L. Lucia, J. L. Hernandez-Rojas, C. Leon, and I. Mártil, “Capacitance measurements of p-n junctions: depletion layer and diffusion capacitance contributions,” *Eur. J. Phys.*, vol. 14, no. 2, pp. 86–89, Mar. 1993, doi: 10.1088/0143-0807/14/2/009.
- [57] H. K. Gummel and D. L. Scharfetter, “Depletion-Layer Capacitance of $p + n$ Step Junctions,” *J. Appl. Phys.*, vol. 38, no. 5, pp. 2148–2153, Apr. 1967, doi: 10.1063/1.1709844.
- [58] A. Acharyya, S. Banerjee, and J. P. Banerjee, “Influence of skin effect on the series resistance of millimeter-wave IMPATT devices,” *J. Comput. Electron.*, vol. 12, no. 3, pp. 511–525, Sep. 2013, doi: 10.1007/s10825-013-0470-y.
- [59] M. H. Yang, K. B. K. Teo, W. I. Milne, and D. G. Hasko, “Carbon nanotube Schottky diode and directionally dependent field-effect transistor using asymmetrical contacts,” *Appl. Phys. Lett.*, vol. 87, no. 25, Art. no. 25, 2005, doi: 10.1063/1.2149991.
- [60] M. Nicolet and M. Bartur, “Diffusion barriers in layered contact structures,” *J. Vac. Sci. Technol.*, vol. 19, no. 3, pp. 786–793, Sep. 1981, doi: 10.1116/1.571149.
- [61] G. K. Reeves and H. B. Harrison, “Obtaining the Specific Contact Resistance from Transmission Line Model Measurements,” *IEEE Electron Device Lett.*, vol. 3, no. 5, pp. 111–113, 1982, doi: 10.1109/EDL.1982.25502.
- [62] S. Sami, P. A. B. Haase, R. Alessandri, R. Broer, and R. W. A. Havenith, “Can the Dielectric Constant of Fullerene Derivatives Be Enhanced by Side-Chain Manipulation? A Predictive First-Principles Computational Study,” *J. Phys. Chem. A*, vol. 122, no. 15, pp. 3919–3926, Apr. 2018, doi: 10.1021/acs.jpca.8b01348.
- [63] E. Secchi, S. Marbach, A. Niguès, D. Stein, A. Siria, and L. Bocquet, “Massive radius-dependent flow slippage in carbon nanotubes,” *Nature*, vol. 537, no. 7619, pp. 210–213, Sep. 2016, doi: 10.1038/nature19315.