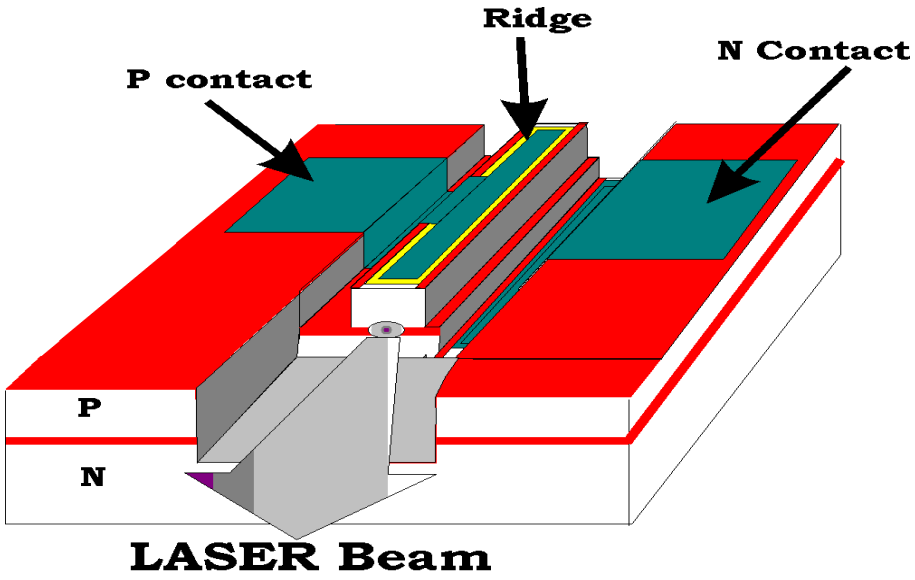
Κατασκευή Ολοκληρωμένων Οπτοηλεκτρονικών Αρσενικούχου Γαλλίου πάνω σε δισκία πυριτίου

του
Γεώργιου Δεληγεώργη



Ηράκλειο 2002

Εργασία Master

Περίληψη

Η ανάγκη για νέες λύσεις στον χώρο των ολοκληρωμένων κυκλωμάτων είναι σήμερα πιο πιεστική παρά ποτέ. Η ολοένα αυξανόμενη συχνότητα λειτουργίας των ολοκληρωμένων έχει οδηγήσει σε αδιέξοδο, που αφορά όχι το υλικό και τις ικανότητες λειτουργίας του αλλά την δυνατότητα διασύνδεσης των επιμέρους κυκλωμάτων. Η καθυστέρηση διάδοσης των σημάτων στις ηλεκτρικές γραμμές μεταφοράς που χρησιμοποιούνται στην σημερινή τεχνολογία, είναι πλέον ο βασικός παράγοντας περιορισμού της αύξησης της συχνότητας λειτουργίας. Επιπλέον, η αυξανόμενη ζήτηση για ολοκληρωμένα που μεταφέρουν μεγάλα ποσά πληροφορίας κάνει τις ηλεκτρικές διασυνδέσεις μεταξύ ολοκληρωμένων εξίσου προβληματικές.

Η παρούσα εργασία μελετά την ανάπτυξη μιας πιθανής λύσης που δεν απαιτεί υβριδικές κατασκευές, δηλαδή, την συναρμολόγηση πολλών επιμέρους ψηφίδων με ολοκληρωμένα κυκλώματα διαφορετικής τεχνολογίας το καθένα μέσα σε ένα chip. Αντίθετα, η δημιουργία μονολιθικά ολοκληρωμένων οπτοηλεκτρονικών διατάξεων που αποτελούνται από πολλά ετερογενή υλικά ολοκληρωμένα σε κλίμακα δισκίου είναι η βασική ιδέα της μεθόδου που εξετάζεται σε αυτή την εργασία.

Δεδομένου ότι η διάδοση του φωτός δεν πάσχει από προβλήματα καθυστέρησης και απωλειών λόγω χωρητικότητας, θα μπορούσε κανείς να φανταστεί ένα ολοκληρωμένο στο οποίο βασικά σήματα μεταφέρονται από/ προς ή μέσα σε αυτό με οπτικά σήματα και όχι με ηλεκτρικά.

Τα συμβατικά ολοκληρωμένα σήμερα βασίζονται στο Πυρίτιο (Si) και συγκεκριμένα στην τεχνολογία CMOS. Το πυρίτιο όμως είναι από την φύση του ανίκανο να παράγει οπτικά σήματα. Αντίθετα άλλα υλικά όπως το Αρσενικούχο Γάλλιο (GaAs) είναι ιδιαίτερα κατάλληλα για παραγωγή φωτός.

Επειδή όμως τα υλικά αυτά έχουν αρκετά διαφορετικά φυσικά χαρακτηριστικά, δεν γίνεται κανείς να ενσωματώσει το ένα στο άλλο με μεθόδους επιταξίας. Απόπειρες προς αυτή την κατεύθυνση έγιναν την προηγούμενη δεκαετία και απέδειξαν τις περιορισμένες δυνατότητες ενός τέτοιου πονήματος.

Η λύση που ερευνήθηκε στην παρούσα εργασία αφορά την ενσωμάτωση του ενός υλικού με το άλλο, όσο ακόμη τα ολοκληρωμένα βρίσκονται σε μορφή δισκίου. Συγκεκριμένα, μετά την ολοκλήρωση της κατασκευής των κυκλωμάτων στο Πυρίτιο, ένα στρώμα Αρσενικούχου Γαλλίου επικολλάται στην επιφάνεια με χρήση συγκολλητικού υλικού που λέγεται Spin On Glass (υαλώδες υλικό σε υγρή μορφή). Κατόπιν, το Αρσενικούχο Γάλλιο επεξεργάζεται δημιουργώντας οπτοηλεκτρονικές διατάξεις που διασυνδέονται με τα υποκείμενα κυκλώματα Πυριτίου και οι οποίες αναλαμβάνουν την οπτική λειτουργία.

Δισκία κατασκευασμένα με την παραπάνω τεχνική μπορούν να επεξεργαστούν χωρίς να καταστραφούν τα κυκλώματα του πυριτίου γιατί η θερμοκρασίες επεξεργασίας του Αρσενικούχου Γαλλίου - κατά την κατασκευή διατάξεων - είναι πολύ μικρότερες από αυτές του Πυριτίου. Για να δειχθεί η δυνατότητα μιας τέτοιας εφαρμογής κατασκευάστηκε ένα πρότυπο οπτικό κανάλι επικοινωνίας αποτελούμενο από ένα λέιζερ ημιαγωγού, ένα κυματοδηγό και μια φωτοδίοδο, διασυνδεδεμένα

κατάλληλα μεταξύ τους και με το υποκείμενο κύκλωμα πυριτίου.

Παρουσιάζεται στην εργασία η μέθοδος κατασκευής τόσο του ετερογενούς υλικού όσο και των διατάξεων GaAs που αποτελούν το οπτικό μέρος του καναλιού (λέιζερ, κυματοδηγός και φωτοδίοδος). Γίνεται επίσης χαρακτηρισμός της απόδοσης τους. Τέλος γίνεται μια σύντομη αναφορά στις προοπτικές και τις δυνατότητες που δίνει η προσέγγιση αυτή.

Η εργασία αυτή πραγματοποιήθηκε στο εργαστήριο Μικροηλεκτρονικής του Τμήματος Φυσικής του Πανεπιστημίου Κρήτης και του ΙΗΔΛ, ΙΤΕ υπό την επίβλεψη του αναπληρωτή καθηγητή Αλέξανδρου Γεωργακίλα. Η συγκόλληση των δισκίων GaAs και Si έγινε στο συνεργαζόμενο ινστιτούτο Max Plank, στο Halle της Γερμανίας ενώ τα ολοκληρωμένα κυκλώματα στα δισκια πυριτίου σχεδιάστηκαν και κατασκευάστηκαν απο το Ινστιτούτο Μικροηλεκτρονικής του ΕΚΕΦΕ "Δημόκριτος".

Ευχαριστίες

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Επίσης, για να πραγματοποιηθεί αυτή η μελέτη, συνέβαλαν αποφασιστικά όλοι οι συνάδελφοι της Ομάδας Μικροηλεκτρονικής του Ινστιτούτου Τεχνολογίας και Έρευνας, τους οποίους θα ήθελα να ευχαριστήσω.

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Chapter: 1 .Optoelectronic devices design

This chapter is devoted to the theoretical analysis of the concepts behind the design and implementation of optoelectronic devices. The first section presents fundamental semiconductor theory, the second waveguide design the third reviews laser theory and finally photodetectors are discussed. Since optoelectronics is a vast subject, our discussion will be constrained to GaAs based devices. Furthermore, edge emitting / detecting devices - as opposed to surface emitting devices - will be presented since this is the concept used throughout this project.

Section: 1.1 .Semiconductor fundamentals

1.1.1 .Structural properties

Semiconductors are much like insulators. When observed under very low temperature and no external excitation (i. e. light) they have no free carriers. The difference between insulators and semiconductors is not qualitative. The energy that one has to provide for a bond to break (i. e. to create a free electron) varies from a few tenths of an eVolt (eV) to a few eV in a semiconductor whereas for an insulator it is higher.

Semiconductors that are of interest are crystalline materials. By saying crystalline one means that atoms forming the crystal are located in well known spatial coordinates, therefore a clearly periodic structure appears. In fact this periodicity imposes the existence of energy "zones" in which electrons can exist, as well as energy zones that no acceptable solution is possible for an electron. That is why an **energy band gap** is formed. Theoretical analysis of the properties that a periodic structure imposes on moving carriers is possible yet extremely complicated. Solid state theory is armed with a set of models to analyze and provide theoretical understanding of the properties of such structures.

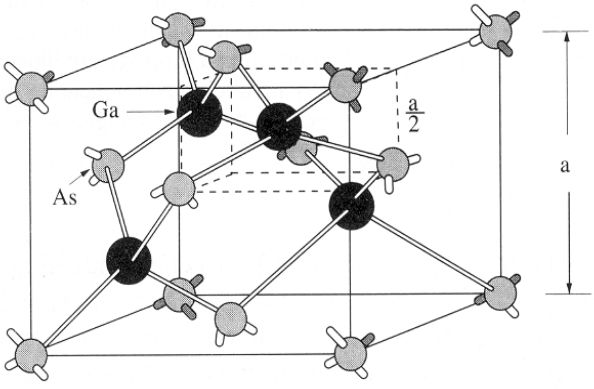

Figure 1.1: Crystal structure of GaAs. a is the lattice constant Reprinted from[1]

In order to achieve a full theoretical analysis of the band-structure of semiconductors, the band theory of solids was developed. The later is based on quantum mechanics and Pauli's exclusion principle. The theory is successfully predicting all

semiconductor properties but suffers from high level of complexity.

Another attempt to model solid state periodic structures is the *one electron model*. According to this, the periodic nature of the semiconductor is taken into account but a single, stand alone electron is considered. This simplifies the mathematics while keeping the characteristic behavior of a semiconductor medium. Quantum mechanical interaction of the electron with the periodic potential resulting from the crystal leads to basic concepts, such as the idea of a hole (a positive particle) and the effective mass of carriers.

A simplification that proved to be extremely powerful in designing semiconductor devices is the "effective mass approximation" According to this, electrons are moving in energy bands that are parabolic in shape with an effective mass different from the free electron. This simplification neglects several important phenomena but gives a good starting point for many of the real world devices.

Obviously, properties of crystals vary depending on the atom or atoms forming the building block of each crystal. One could categorize semiconductors according to whether the unit cell of their structure contains one kind of atom (Silicon, Germanium, Diamond) or more, (GaAs, InN, SiC, InAlGaAs, AlGaAsN etc) into elemental and compound semiconductors respectively. In general, a semiconductor material is formed by elements of group IV of the periodic table or combinations of symmetric groups like III-V and II-VI.

Although a piece of pure semiconductor material is of huge interest to a theoretical physicist, real world applications would not be possible unless doping was invented. By doping we mean the controlled incorporation of different kind of atoms in the crystal. The effect arising from this "dirty" crystal is astounding. One can control the conductivity of a semiconductor throughout many orders of magnitude and can even control the type of conductivity observed in a sample (more on this later). This gives a tool to manipulate electronic properties of a semiconductor and transform it to transistors, rectifiers, resistors etc. Most astounding of all is that the level of foreign atoms in a semiconductor in order to make all of this feasible is seldom more than one in a million!

Modern technology has several ways to create semiconductor material. The idea is to start with chemical purification of the material and subsequently follow thermal procedures to transform it to a single crystal of macroscopic dimensions (As large as a meter). This is the *Ingot* from which slices are cut to form the wafers.

Wafers are basically the "atomic matrix" on which the active material is grown by means of an epitaxial growth technique. This imposes limitations to the choice of materials grown on a certain substrate. Each crystal is characterized by a specific lattice constant (meaning the inter-atomic distance). In order for a crystalline material to be successfully grown on a wafer, the lattice constants of the grown material has to match that of the substrate. The parameter deciding whether a material can grow on top of a specific substrate is therefore the lattice constant and as soon as one chooses a substrate, the lattice matched semiconductors are the only choice available for use on the specific

growth sequence. Fortunately, there are several materials that are lattice matched such as GaAs and $Al_xGa_{1-x}As$ which are practically lattice matched, having only a minor lattice constant difference. Furthermore, one can bend the rule by growing thin layers of material that is not normally lattice matched. In this case elastic deformation of the crystal accommodates the difference and the crystal is still continuous up to a certain thickness. Above that, the forces developed are large enough to break the crystal and create dislocations that are detrimental to material quality.

There are several ways to "grow" a crystal. Some of them will be shortly described thereafter.

MOLECULAR BEAM EPITAXY: The sample is introduced in a high vacuum chamber and heated to a point where the mobility of surface atoms is large. A series of targets is placed opposite to the sample and heated so that evaporation takes place. Evaporated atoms reach the substrate and interact with it forming bonds therefore extending the crystal. Depending on the kind of atoms evaporated and their relative flux, the composition of the grown crystal can be controlled. This technique is considered to be slow but can provide heterostructures of superior quality.

VAPOR PHASE EPITAXY: The sample is introduced in a chamber and heated to high temperatures. Gases carefully selected are released and decompose thermally close to the substrate releasing the desired atoms that bond on the surface. This technique is known to produce very pure crystals with high quality and at higher rate compared to MBE. However it is not easy to change the composition of the crystal abruptly as this involves gas exchange. therefore thin layers of material are difficult to grow.

In general there are several techniques available but the general idea is more or less clear from the examples mentioned. Thermodynamics play a crucial role in crystal growth and a large number of parameters have to be controlled to undergo a successful growth.

The material used throughout this work was fabricated in a VG80H MBE reactor able to produce GaAs based compound semiconductors. In what follows the material characteristics for the GaAs / $Al_xGa_{1-x}As$ system will be thoroughly analyzed.

1.1.2 .Electronic properties

The main characteristic a semiconductor material has [5], is the band gap energy. Above that lies the conduction band which is actually the energy zone electrons populate in order to move in a semiconductor sample. Below that there is the valence band that corresponds to bound electrons. Similar but opposite facts hold for the hole which is bound when in the conduction band and free to move in the valence band. Doping a semiconductor is the means of controlling the number of electrons or holes available in each band and therefore controlling the conductivity of the sample.

Dopants actually provide extra states close to the valence band (acceptors) or the conduction band (donors). Since only a small amount of energy is required to ionize the dopant, typically a few meV, virtually all dopants are ionized at room temperature. This provides a deviation from the intrinsic semiconductor in the sense that there are free

carriers available (provided by the impurities).

Lets take a look at the basic equations that hold true for carrier populations. Carriers are fermions and therefore obey Fermi statistics inside a semiconductor sample. The probability that a certain state is occupied is given by the notorious Fermi-Dirac distribution: $N=\frac{1}{\exp[\frac{E-E_f}{k_b \cdot T}]+1}$ Equation 1.1

E_f is called the Fermi energy level. The Fermi energy level can be defined in several equal ways and it is basically a measure of the chemical potential the carriers have inside the semiconductor material. Although obvious, it should be noted that when no external perturbation is applied to the system, the Fermi level is constant along the sample in question. This observation allows us to simplify analysis of devices under equilibrium conditions.

Based on our discussion so far, we can calculate the probability of occupation of a quantum state as long as we know the energy that corresponds to that state as well as the Fermi level position. In order to calculate total carrier concentrations we need some information about the number of states existing in that specific energy range. therefore equally important is the density of states function which gives information about the available states.

1.1.2.1 .Three dimensional density of states

The density of states in bulk semiconductor material is derived from the fact that Pauli's exclusion principle does not allow more than one electron with the same spin in each quantum state. Thus after a simple mathematical manipulation, [5] we find that the three dimensional density of states vs. Energy is given by:

$$N_c(E)=\frac{\sqrt{2}}{\pi^2}\left(\frac{m_{eff}}{\hbar^2}\right)^{3/2}(E-E_c)^{1/2}$$ Equation 1.2

for the conduction band and: $N_v(E)=\frac{\sqrt{2}}{\pi^2}\left(\frac{m_{heff}}{\hbar^2}\right)^{3/2}(E_v-E)^{1/2}$ Equation 1.3

for the valence band.

1.1.2.2 .Two dimensional density of states - Quantum wells

In a quantum well, the three dimensional model does not apply since along one direction (usually the growth axis) there is a confining potential. Along that direction, solution of the Schrodinger equation gives discrete states (energy and wave-functions) an electron can have. The corresponding density of states is calculated taking into account the remaining two dimensions which are still not quantized[i] and have the same

i Keep in mind that we are developing this in the framework of energy bands therefore the energy can be $N(E)=\frac{m_{eff}}{\pi\hbar^2}$

parabolic E vs k relation. It is easily shown that for each sub-band we have:

$$N(E)=\frac{m_{eff}}{\pi\hbar^2} \qquad \text{Equation 1.4}$$

This results in a step like density of states for the quantum well structure.

1.1.2.3 .Carrier dispersion relation

Carriers moving in a semiconductor are characterized by their effective mass which is a property imposed by the periodic lattice potential. Effectively one takes electrons and holes to behave as if they move in free space but with a modified mass in order to take into account the lattice effect. This is called the effective mass approximation and it is valid for low kinetic energies. The total energy of each carrier is given by:

$$E_c=\frac{\hbar^2\vec{k}^2}{2\cdot m_{eff}}+E_g \qquad \text{Equation 1.5}$$

for the conduction band.

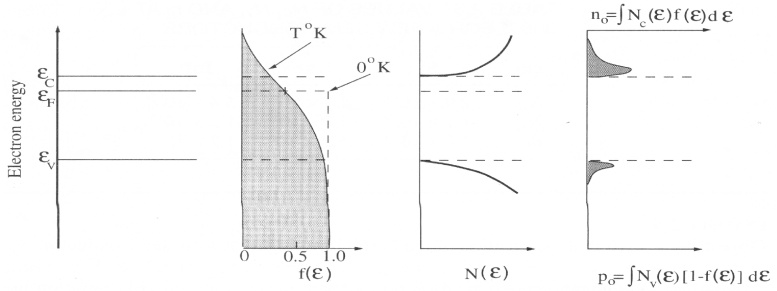

Figure 1.2: Carrier density profile vs energy for both bands. One can see that most carriers reside close to the band edges. Reprinted from [1]

1.1.2.4 .Energy gap parameters

The energy gap E_g is characteristic of each semiconductor and is temperature dependent. There is an empirical relation proposed by Varshni [6] that accurately describes this dependence.

$$E_g(T)=E_g(0)-\frac{A\cdot T^2}{T+B} \qquad \text{Equation 1.6}$$

where A and B are two material dependent parameters. The following Table provides a sample of parameters for the Varshni equation for various materials.

Material	*$E_g(0)$*	*A (eV/K^2)*	*B (°K)*
GaAs	1.519	$5.405\text{x}10^{-4}$	204
InP	1.421	$4.906\text{x}10^{-4}$	327

regarded as continuous

aterial	$E_g(0)$	$A\ (eV/K^2)$	$B\ (°K)$
$Al_{0.27}Ga_{0.73}As$	1.932	$6.580x10^{-4}$	248

Table 1.1: Varshni equation parameters

There is another interesting point to be noted: One can grow $Al_xGa_{1-x}As$ with varying mole fraction (x). This necessitates the prediction of the energy gap of alloys, depending on the mole fraction of each element. To first approximation, one could take the weighted average of the to extremes but this is not accurate. Usually there is a nonlinear term called **bowing** factor. The following table gives a few interesting examples of band gap dependence of several alloys at 300 Kelvin.

Compound	*Direct energy gap (eV)*
$Al_xGa_{1-x}As$	$1.425 + 1.247x + 1.147(x-0.45)^2$
$Ga_xIn_{1-x}As$	$0.36 + 1.064x$
$Al_xIn_{1-x}As$	$0.36 + 2.012x + 0.698x^2$
GaP_xAs_{1-x}	$1.424 + 1.150x + 0.176x^2$

Table 1.2: Compositional dependence of the energy band gap for some compound semiconductors. (from P.Battacharya Prentice Hall 1993)

1.1.2.5 .Heterojunction formation

When two different semiconductor materials are grown one on top of the other, a heterojunction is formed. Normally the two materials will have different band gaps. The question is, how will the conduction and valence band of the materials behave near the heterointerface? There have been many attempts to predict theoretically the band lineup in a heterojunction but so far none seems to have universal success.

One of the simplest approaches was the **electron affinity rule**. (Also named Anderson model) According to this, the conduction band discontinuity is such that it accommodates the difference in electron affinity[i] between the two materials. In this model a perfect, defect free interface is assumed. Although gross estimates of some discontinuities are obtained by this method, it appears unable to predict the accurate band lineup for several cases. This is why a different model was proposed.

i Electron affinity is the energy difference between the conduction band of a semiconductor and the vacuum level

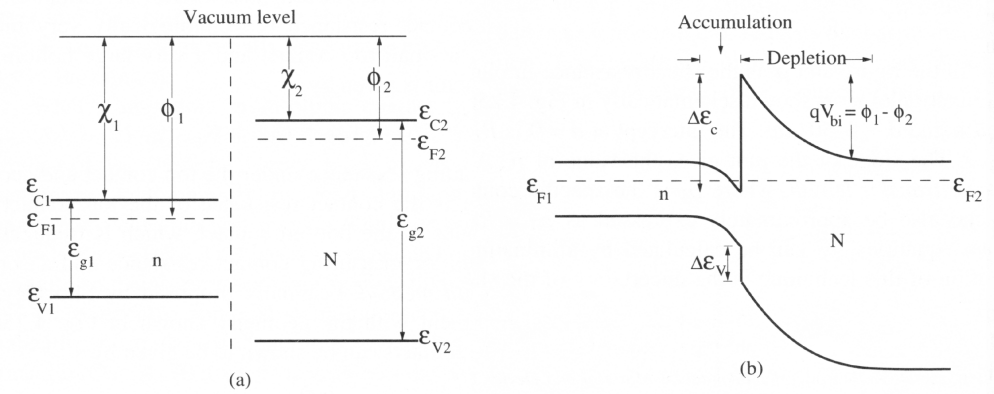

Figure 1.3: Band lineup in a heterostructure according to the Anderson model. Reprinted from[1]

The **common anion rule.** Since the top of the valence band is formed by the anion of a compound semiconductor, materials sharing the same anions are expected to have very small valence band discontinuities. Although the trend of experimental results is matching this model, good numerical agreement was not observed.

Experimental data have been collected and usually theoretical work is based on the former to ensure good agreement between device analysis and experiment.

1.1.2.6 .Free carriers - conduction

Free carriers move in their respective bands. To start with, they have a thermal energy which is manifested by a mean velocity u_{th}. Besides that, they will respond to an electric field by drifting. Finally if for any reason the concentration of free carriers is not uniform throughout a sample, there will be diffusion toward lower concentrations.

Obviously, once a carrier starts moving it will not go on forever. There are several reasons to hinder this ever lasting movement. Carriers scatter at impurities, dopants and any kind of anomalies. All these processes slow carriers down and when no electric field or concentration gradient exists carriers eventually move only because of their thermal energy.

If one assumes parabolic bands (the effective mass is independent of energy) then the electron and hole current densities are given by the following equations:

$$J_e = qnm_e E + qD_e \frac{dn}{dx} \qquad \text{Equation 1.7}$$

$$J_h = qnm_h E - qD_h \frac{dp}{dx} \qquad \text{Equation 1.8}$$

D_e and D_h are the diffusion constants of electrons and holes respectively and they are proportional to the mobility with a constant of proportionality equal to k_bT/q.

Obviously eq. 1.7 And 1.8 hold for small electric fields. If this is not true, then the constant mobility assumption is no longer accurate and different models are needed to explain carrier conduction processes in that regime.

1.1.2.7 .Recombination – Generation processes

At a given temperature, there is a small but finite possibility that some free carriers exist in a semiconductor sample. Those carriers come from the finite possibility that a carrier is thermally exited. Of course for typical semiconductor band gaps, the energy needed for such a process is huge compared to the mean thermal energy k_bT. Thus only few carriers will be present.

When a semiconductor is doped, the situation is much different. The energy needed to ionize the dopants is rather small compared to the mean thermal energy. This results in almost complete ionization of the dopants at room temperatures. However, as soon as one type of carriers is increased by means of doping the opposite kind will decrease so that the product is a constant. This is called the mass product law and holds true for semiconductors under equilibrium. We will come back to this shortly.

Obviously electrons and holes interact with each other. If for example we create some electron hole pairs by means of illumination in a semiconductor, as soon as the excitation is turned off, the excess carriers will recombine and the steady state populations will be reinstated.

This annihilation process can happen either through direct band to band transition of a carrier, or through defects in the band gap. Back in 1952, Shockley, Read and Hall [7] [8] presented a theory of recombination that explained recombination through defects in the band gap. According to this, the recombination rate is given by:

$$R = s_r u_{th} N_T \frac{np - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_T - E_f}{k_B T}\right)} \qquad \text{Equation 1.9}$$

Where n_i is the intrinsic carrier concentration, E_T is the energy of the defect center, N_T is the density of the defects and s_r is the capture cross section of each defect.

According to the last equation there can be both positive as well as negative recombination. This merely represents the fact that there can be either creation or annihilation of carriers so that carriers tend to resume their equilibrium concentrations. If the np product is larger than n_i^2 then annihilation takes place whereas if it is smaller, carriers are thermally created. In the following section we shall see an example of both cases.

1.1.2.8 .The PN structure

If we assume that a semiconductor is grown by some means and the composition as well as the type of doping is varied across the growth axis, resulting in an area that is p-type doped (holes are majority carriers) and an adjacent area which is n-type doped (electrons are majority carriers) due to the difference in concentrations, there will be diffusion of carriers toward small concentration areas. Accordingly, this will result in an electric field near the junction which will hinder the diffusion process. Overall, a dynamic equilibrium will be reached and macroscopically no current will flow. The region where the electric field is developed, is called the depletion region. When no

external bias is applied to this system the Fermi potential is flat and the np product is equal to the n_i^2 throughout the structure. If however a Voltage is applied, the situation changes drastically. The applied bias will affect the depletion region, changing its width and the corresponding carrier distributions. For a reverse applied bias, the np product will be smaller than n_i^2 which means that generation of carriers will take place. This is why we see a small reverse current dependence on applied bias. If on the contrary the applied voltage is positive (forward bias) the depletion region becomes smaller and more carriers are injected into this area. This means that the np product becomes larger than n_i^2 and therefore we have recombination effects inside the depletion region.

In order to reach a solution for the PN junction behavior we will make a series of approximations. Namely, we will assume an abrupt junction with constant doping density within each side. Furthermore, we assume that close to the junction where the depletion region is formed, there is a well defined area that no free carriers exist because of the electric field. The later is called **depletion approximation.** Using Poisson's equation for the density of carriers and the current density equations that are described earlier, we find that there is a built in potential across the depletion region

that is equal to: $$V_{bi}=\frac{K_B T}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$ Equation 1.10

And a depletion width equal to: $$W=\sqrt{\frac{2\varepsilon_o \varepsilon}{q N_B}\left(V_{bi}-\frac{2k_B T}{q}\right)}$$ Equation 1.11

Under forward bias the diffusion and drift current components for each kind of carrier do no longer balance each other. The potential barrier across the depletion region is lowered by the externally applied voltage. As a result, current flows through the device. We again use the same equations but add a deviation from equilibrium minority carrier densities δp and δn. Following the necessary mathematical manipulation we get that the current density flowing across the device is an exponential function of the externally applied bias:

$$J=q\left(\frac{D_h p_{NO}}{L_h}+\frac{D_e n_{PO}}{L_e}\right)\cdot\left(e^{\frac{qV_f}{k_B T}}-1\right)$$ Equation 1.12

Under reverse bias, the scenery is much the same. Only that know the potential barrier across the depletion region is magnified by the external voltage. Using the same reasoning we can neglect the exponential term in eq. 1.12. therefore the current assumes a simpler form independent on applied voltage (only the first bracket survives).

It is important to note that carrier density inside the depletion region changes with the applied bias. When in reverse bias, the carrier density drops below the equilibrium. Therefore, as we have seen in section 1.1.2 there will actually be a regeneration process evolving inside the depletion region. On the contrary, under forward bias the situation is reversed. The concentration of both kinds of carriers is increased compared to the

equilibrium values, this results in a recombination process inside the depletion region.

One of the approximations done in order to obtain the I-V characteristics of the PN diode was that a small deviation of minority carriers, δp and δn, is imposed by the applied bias. If we increase the forward bias this approximation is no longer valid as the excess minority carriers on each side of the depletion region become comparable to the majority carrier densities. At this regime, both drift and diffusion components become important and the current density becomes more complicated. This issue will be addressed later in more detail.

1.1.3 .Optical properties

Traditionally, semiconductors are divided in two main categories depending on their band formation, those that have the conduction band minimum at the same k that the valence band maximum appears and those that do not.

The later case is designated by the name "indirect" which comes from the fact that carriers traversing the band gap have to undergo an indirect transition i.e. a photon and one or more phonons have to participate in order not to violate the rules of energy and momentum conservation. This category is of little interest to us since multi particle transitions are known to happen with very low probability. Practically this means that these materials do NOT produce light efficiently simply because carriers recombine

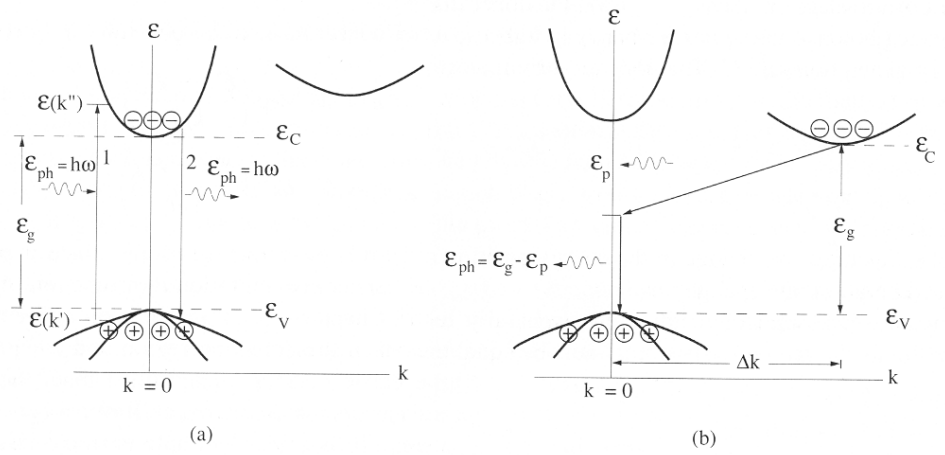

Figure 1.4: Direct (a) and indirect (b) semiconductor band structure. One can see the carrier interaction process. Reprinted from[1]

through processes that are equally probable and do not radiate. Typical semiconductors in this category are Germanium, Silicon and several others.

On the other hand, direct band gap semiconductors as one may foresee do not need multi particle processes to interact with photons. Simply because a photon carries significant energy but practically no momentum, energy momentum is easily satisfied from the majority of carriers that get involved in a band to band process since both holes and electrons thermalize to k = 0. Obviously this process is much easier, and will therefore be more probable. Such materials are good candidates for optoelectronic applications since they interact strongly with light.

To support the later conclusion one may take a look at radiative efficiency of Silicon (indirect) which is less than 1% and GaAs (direct) which can easily exceed 99%.

1.1.3.1 .Absorption

The main interaction of light propagating in a direct semiconductor originates from carriers traversing the band gap. That is why semiconductors are nearly transparent to radiation that does not provide enough energy per photon to match the energy band gap. Above that energy however, direct semiconductors become strongly absorbing. Quantum mechanical perturbation theory provides the theoretical tool to model the probability of a transition caused from a light beam in a semiconductor media.

If one photon is absorbed, and an electron and a hole are created, the general rules of momentum and energy conservation are valid. In this context, the energy of the photon is passed to the generated carriers and the momentum that they obtain has to be equal to that of the photon. If one looks at the momentum a photon is carrying, it turns up that it is negligible compared to typical momentum of a free carrier, on the other hand, the energy that the photon releases during absorption is rather big (in the order of 1 eV. therefore the transition of the carrier that absorbed the photon will be aproximately vertical (In an E vs k diagram) .This is commonly referred to as the **vertical transition rule**. In order for a carrier to absorb a photon, there have to be an empty state directly above the initial state and furthermore it has to be exactly E_{photon} above in terms of energy. Thus, the probability of an absorption taking place depends on the available carriers, the empty states and the transition probability.[1] This is all summed up in the following equation:

$$\alpha(\hbar\omega)=\frac{q^2 m_o^{1/2}}{4\pi\hbar^2\varepsilon_o c} n_r^{-1}\left(\frac{2m_r^*}{m_o}\right)^{3/2}\frac{f_{CV}}{\hbar\omega}(\hbar\omega-E_g)^{1/2} \qquad \text{Equation 1.13}$$

Where f_{CV} is the oscillator strength and it is a measure of the quantum mechanical probability of the transition. It is worth noting that the final bracket originates from the density of states in bulk material.

For an indirect semiconductor,momentum conservation cannot be satisfied in a photon – electron interaction alone. This case is more complicated and involves one or more phonons that contribute their momentum (phonons typically have large momentum and small energy). As one may understand, indirect transitions, being multi-particle processes, happen with a much smaller probability.

Another phenomenon that puzzled scientists in the early days of semiconductor research was the exciton. It appears that there is a sharp peak of absorption a few meV below the absorption edge of the material. This peak originated from the fact that interaction of electrons and holes can form states much like a hydrogenic orbital but instead of free space, the surrounding material was the semiconductor lattice. The result is that those hydrogenic orbitals provide states inside the forbidden gap of the semiconductor (namely a few meV below the edge of the conduction band). Since the energy state is so close to the energy of the free electron inside the crystal, this

interaction is very sensitive to temperature. This is why excitons are observed at low temperatures in typical semiconductor materials.

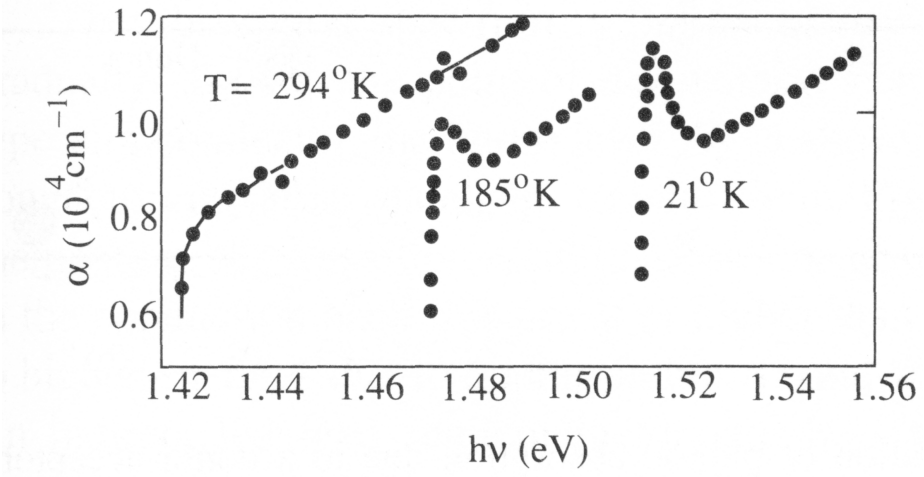

Figure 1.5: Absorption vs Temperature. The excitonic peak is evident at low temperatures. Undoped GaAs grown by MBE. Reprinted from [1]

A word of caution here concerns new, wide bandgap semiconductors which have exciton binding energy that can be as high as 50meV. This is twice the average thermal energy at room temperature so maybe a change of scenery is approaching.

Besides band to band and exciton absorption, there are several other - less profound but equally significant - processes one has to take into account to explain absorption spectra. These processes have to do with extra states created by impurities (like donor-Acceptor transitions) or with multi-particle processes (like free carrier absorption). These effects become important when one operates a device under very high light intensity and/or high carrier concentrations (such as those in a laser device!).

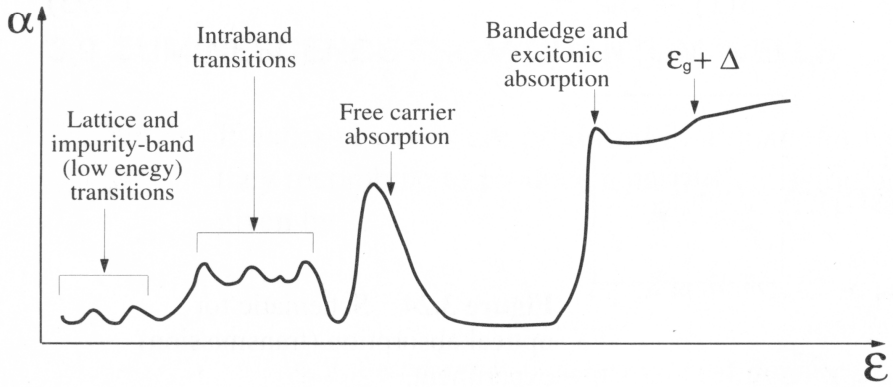

Figure 1.6: Absorption vs photon energy diagram taking into account different effects at various energies. Δ is the energy difference between the valence band minima. Reprinted from [1]

1.1.3.2 .Recombination – Light Emission

The exact opposite of absorption is emission of photons from a semiconductor. The radiation spectra is however a completely different story. Carriers inside a band interact

so fast that usually they assume a fermi distribution profile before any recombination takes place. therefore by the time an electron recombines with a hole to produce a photon, it will be part of a Fermi gas no matter what its initial state was. This is why radiation from a semiconductor is mainly observed at energies that match the band gap and not far above. Obviously, there are no states inside the band gap so there is no recombination possibility for lower energies as well.

As we have already explained, carriers in a band always obtain a Fermi distribution. Photon emission is the result of carrier recombination inside a semiconductor. When a semiconductor is at rest, both carrier distributions are described by a single Fermi level. For such a case, we have already discussed that the carrier populations are constant. Such a semiconductor obviously will not emit light. This is the concept that van Roosbroeck and Shockley used to calculate the spontaneous photon emission probability. For each photon energy, there has to be an equilibrium so that whatever is emitted, is re-absorbed by the material.

The final result is obtained taking into account Plank's law and the absorption spectra which is easily measured.

$$R_{sp}(\nu)d\nu = \frac{32\pi^2 k_a(\nu) n_r^2 \nu^4}{c^2[\exp(\frac{h\nu}{k_b T})-1]} d\nu \qquad \text{Equation 1.14}$$

Where k(ν) is the absorption vs frequency. In order to get the radiation spectra from a semiconductor sample one needs the emission probability (Eq. 1.14) as well as the occupation probability for both carriers involved.

Besides recombination that results in photon generation (radiative recombination) there are other recombination processes that compete in carrier destruction. Depending on the time scale of each process the relative intensity can be deduced. If for example radiative recombination takes place with a carrier life time of nsec and there is another, non radiative process that provides a carrier life time of psec, then only a small amount of photons will be produced as most carriers will recombine through the fast, non radiative process. This is why, material for optoelectronic application have to be high quality, a material with low quality would provide many, fast recombination centers, stealing carriers from radiative recombination.

So far we have neglected the fact that for intense radiation and high carrier concentration, there is a non negligible probability that stimulated emission may take place. This will be covered when gain in a laser is addressed.

1.1.4 .Material armory

The idea of optoelectronic devices is based on the concept that one can have a material that efficiently handles both carriers (i.e. electrons and holes) as well as photons. In order for this to happen radiative efficiency alone is not enough. There is a need to confine light. This translates to refractive index variations that can be tailored according to our needs. There is also need to confine carriers to parts of the structure

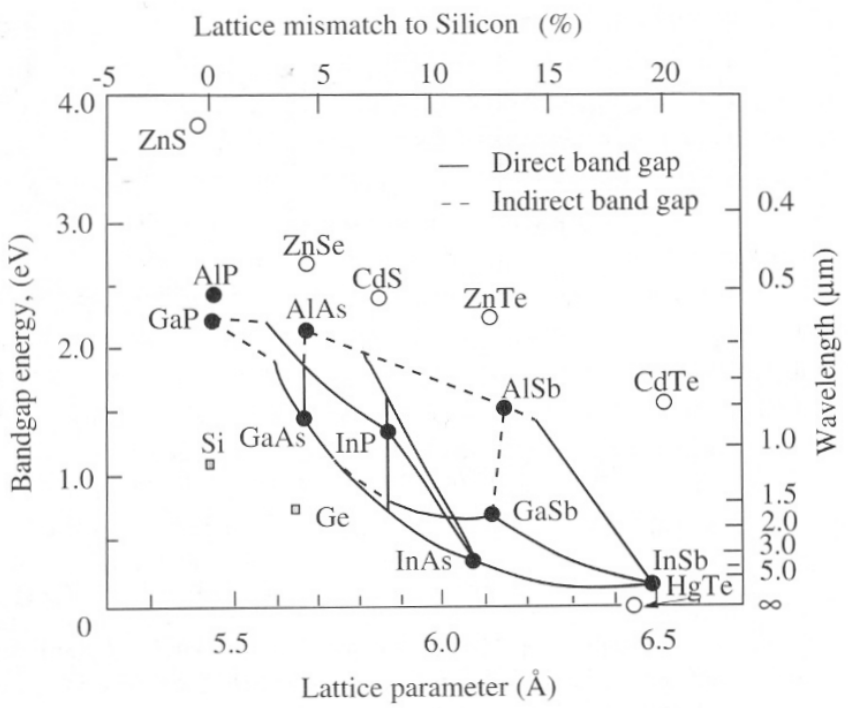

Figure 1.7: Bandgap vs Lattice constant. for different materials. Dotted lines represent indirect bandgap alloys. Reprinted from [1]

where you expect them to recombine (giving photons). The latter translates to band tailoring. Luckily, both may be satisfied simultaneously using semiconductor materials. There is a general tendency that the higher the band gap, the lower the refractive index of a given material and it is "god's gift" that this tendency exists! [9]

In search for an optoelectronic circuit one needs a pool of materials to use in order to manipulate basic characteristics of the structure.

One of these choices is the $Al_xGa_{1-x}As/GaAs$ system. As we have already mentioned, both the band gap of this material as well as the refractive index change with the mole fraction x. Furthermore the fact that $Al_xGa_{1-x}As$ is lattice matched to GaAs alleviates all problems that one may encounter in heterostructure growth. To add to this, $In_xGa_{1-x}As$ with low Indium mole fraction can be successfully incorporated into GaAs based structures although it is not lattice matched.

Section: 1.2 .Waveguide design

The word **waveguide** is describing fairly accurately the purpose of such a design. A waveguide is a "device" that can guide electromagnetic radiation, in other words light. The first waveguides were more or less like pluming and they were designed to guide microwaves. A metallic tube that would bend around leading the electromagnetic radiation inside, toward its other end. For light however a metallic tube will not do the trick. That is because metal itself is absorbing light since it has a high concentration of free carriers (electrons) which steal energy from the wave dumping it into oscillatory motion. There is however a much more clever way to guide light.

Dielectric materials have no free carriers but they do have a property relative to light

propagating inside them, refractive index. Let us assume that we have a slab of glass much like a piece of a broken window and we shine light across one edge. If one looks across the opposite edge of the glass the light will shine out, even if the original track of the light ray was such that it should normally come of the polished flat side. Whats going on? The answer lies in total internal reflection or, to be formal, in Maxwell's set of equations that are going to be presented in the next section.

A simplistic yet very powerful approximation lies in Snell's law:

$$\frac{\sin\theta_1}{\sin\theta_2}=\frac{n_2}{n_1}$$ Equation 1.15

According to this if we have an interface of two materials with different refractive indices, and a ray of light impinges onto the interface originating from the high index material, there is an angle above which no light will emerge into the low refractive index material but total internal reflection will happen, meaning that 100% of the intensity will be reflected back into the high index material. This concept is used in telecommunications to create optical fibers which guide light and therefore carry information.

1.2.1 .Theoretical background

As stated earlier, light is actually electromagnetic radiation. The correct tool to analyze the behavior of light is to use equations coming from electromagnetic theory. The following relations are called Maxwell's equations after lord Maxwell who invented them and they form the basis of such a formalism.

$$\nabla\cdot E=[\frac{1}{4\pi\varepsilon_o}]4\pi\rho$$ Equation 1.16

$$\nabla\times E=-[c]\frac{1}{c}\frac{\partial B}{\partial t}$$ Equation 1.17

$$\nabla\times B=[\frac{\mu_o}{4\pi}c]\frac{4\pi}{c}J$$ Equation 1.18

$$\nabla\cdot B=0$$ Equation 1.19

Departing from these equations and using some mathematical manipulation we can reach the following set of equations which are called the wave equations and give us the tool to find out if an electrical or magnetic perturbation is actually a wave or not.

$$\nabla^2 E+\omega^2\mu\varepsilon_o\varepsilon_r E=0$$ Equation 1.20

and $$\nabla^2 H+\omega^2\mu\varepsilon_o\varepsilon_r H=0$$ Equation 1.21

were μ is the magnetic permeability of the material and ε are the dielectric constant of the vacuum and the relative dielectric coefficient of the material. The quantity ω is

actually the frequency of the light and it is directly related to the energy a photon of this radiation carries through Plank's formula.

If we try to solve this set of equations for a non uniform system like the glass example described in the introduction, we will see that although light can travel parallel to the glass bulk, there is no solution allowing waves to propagate outside. In other words, light is trapped into the high refractive index material exactly like Snell's law predicted.

In a typical semiconductor laser, the waveguide is usually rectangular in shape as opposed to optical fibers which are circular. Furthermore, the thickness of a typical waveguide is in the order of a micron whereas the width is seldom less than 10μm. This allows us to simplify the above equations into a much simpler form:

$$\frac{\partial^2}{\partial x^2}E(x,y)+(k_o^2 n_{ri}^2-\beta^2)E(x,y)=0 \qquad \text{Equation 1.22}$$

And an identical one for the magnetic component. As one can see, there are two simple solutions to these equations, one when no electric field is present along the axis of propagation (This is called Transverse Electric or TE mode) and another where no magnetic field is present along the propagation axis (TM mode). [2]Of course there are modes which are neither one or the other and these are called TEM modes.

Now let us return to the semiconductor system applying the knowledge gained so far. If we can sandwich a layer of a high refractive index material between two layers of low refractive index materials we may have the same situation. This is actually the case. After careful modeling and taking into account the pool of refractive indices we can get, varying the Al mole fraction in an AlGaAs alloy, it turns out that it is easy to create a waveguide using these materials.

1.2.2 .Waveguide design issues

In a waveguide, light is supposed to travel inside the high refractive index material. Outside this region, there is an exponential like decay of radiation. However even if the cladding layers of the waveguide are large, there is a small part of the propagating light that reaches the area outside the waveguide. Usually this part reaches other semiconductor material that may absorb or even sustain a different waveguided mode. In order for a waveguide to be efficient, the refractive index difference between the core of the waveguide and the cladding layers needs to be as high as possible (this corresponds to small penetration depth into the cladding or in other words better confinement) thus the thickness of the cladding layers have to be calculated so that they are thick enough to provide a sufficient barrier for the radiation.

Furthermore, doping a layer so that it is conductive results in absorption from free carrier effects as well as scattering from the dopant species. Both mechanisms result in loss of radiation and this is to be avoided in a well designed waveguide. As we will see in the following section there are reasons not to make a very thick, undoped cladding layer. One can understand that there is an optimum that has to be pinpointed in order to

design an efficient waveguide structure.

1.2.2.1 .Modeling of waveguides

There are several ways to model the optical behavior of a waveguide structure and to calculate important features such as the numerical aperture, the losses and the modes that can be sustained. The initial parameters are the refractive index profile as well as the wavelength of the propagating radiation.

Finite element analysis: The brute force method to analyze a waveguide that posses practically no limit as far as the refractive index profile, is to use a large grid of points in space and discretize the equations into this area, using differences and divisions. This method requires that large arrays are solved in order to calculate the eigenvalues and eigenvectors. The first will give the propagation constants and the latter will provide the radiation profile along the structure. The drawback of such a technique is that it usually involves large computing times as matrices as large as 10^5 by 10^5 are used to achieve an accurate solution.

Transfer matrix method: A more subtle approach that takes into consideration each layer alone before combining the entire structure to calculate modes. The structure is analyzed on a known basis of solutions i.e. A "rectangular well" set of eigenvectors. The drawback of this method is that it performs poorly if the structure is actually not close to the structure on which the basis of eigenvectors is chosen.

Analytical solutions: This method is actually the most accurate yet very restrictive. If the profile of the refractive index is very simple, a purely mathematical treatment can provide analytical solutions for all of the structure's properties. This method is usually found in textbooks about waveguides but is of small use to real world structures that contain asymmetric or graded regions.

The method that was used to calculate the properties of the waveguide used in this project was the transfer matrix method. Although this method is fairly accurate and provides fast results, it is not very efficient in solving graded index profiles. The graded index regions were actually simulated with a large number of thin layers. The finite element method is more versatile and should be used instead but the computational work involved is much more and was out of scope for this work.

Section: 1.3 .Laser diode design

A semiconductor laser diode is actually three devices in one. First there have to be a waveguide that will keep light on the right track in so that only certain modes are sustained. Then there have to be a gain medium that will provide new photons inside the modes. Finally there have to be an optical cavity that will give the necessary feedback to the optical mode so that the modes are amplified by the gain material.

Waveguides have been already presented in the previous section. Here we will focus on optical gain and a way to introduce carriers in the active part of the structure as well as optical feedback mechanisms.

Optical gain in a semiconductor is achieved by introducing both kind of carriers

(electron and holes) in the same region. Carriers recombine emitting photons that have energy matching that of the energy released by the recombination. This is how light emitting diodes (LEDs) are realised. Normally some of the light that is emitted will be reabsorbed by the material. If however the carrier concentration is high enough, the probability of absorption becomes equal to the probability of emission. This is the point where the material reaches "transparency", in the sense that the material is behaving as if it is transparent. If the carrier concentration is increased even more, a photon is likely to be amplified. What one would have in this case is a semiconductor optical amplifier. This is the area of operation for a semiconductor laser, the only difference being the **optical cavity** that makes sure that some part of the radiation is re-entering the structure. This ping pong track of the photons results in amplification of a mode by a few orders of magnitude. That is when lasing occurs.

1.3.1 .Theoretical background

1.3.1.1 .Semiconductor Diode – PIN structure

The semiconductor laser diode is actually a PIN diode meaning that there is an intrinsic area sandwiched between a p type and an n type layer. The conductive layers are there to provide carriers of the respective type, and the intrinsic area is actually the heart of the device. There is a gain medium that is usually some quantum wells and there is also the core of the waveguiding scheme which is supposed to contain light and guide it toward the mirrors. Besides the modes that can be sustained due to the waveguide design, there is also a question of influence as far as lateral confinement is concerned. There has to be some way to guide light so it does not escape parallel to the substrate. This is done by forming a waveguide in this dimension as well. The easiest way to do this is to etch the surrounding area of the device and remove part of the cladding layers and the core. Thus air surrounds the active material. Since air has a refractive index of 1 a strong waveguiding effect is created. There are other more complicated ways to perform the same task such as buried waveguides e.t.c. The drawback of having air around the device is relevant to surface states that exist on the material. Surface states clamp the Fermi level and provides a fast non radiative recombination path. Both effects result in poor performance of such an exposed laser compared to one that uses a buried waveguide.

The next thing one needs in the intrinsic area is some means of carrier trapping. Carriers that are injected from each side need to stay in the active region until they recombine. This is usually done by the very same layers that provide the optical cladding.

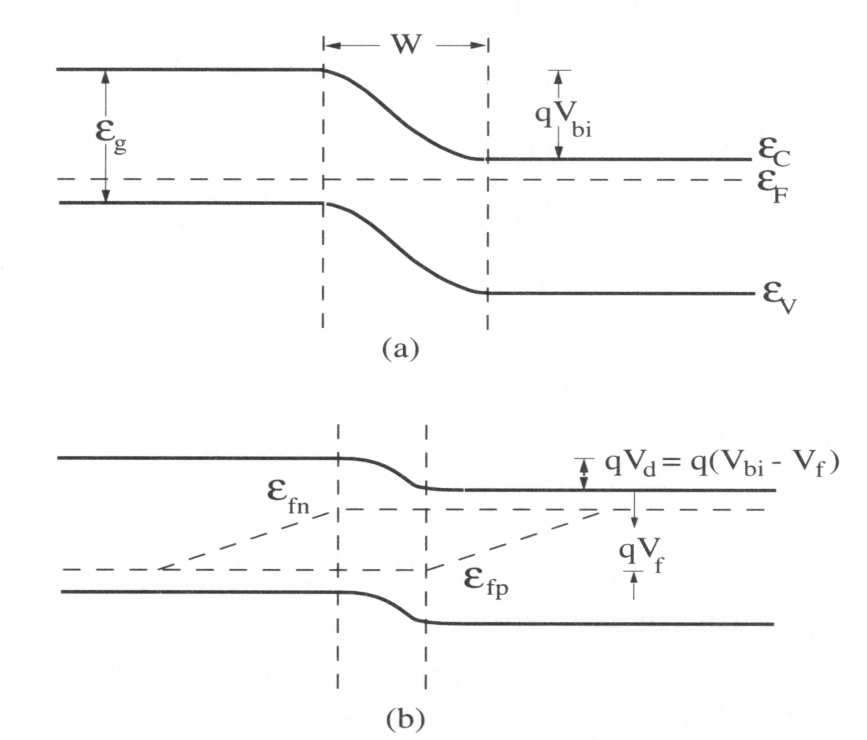

Figure 1.8: PIN structure Band diagram. One can see the quasi fermi levels in forward bias (b). Reprinted from [1]

1.3.1.2 .Cavity analysis

Our discussion is only limited to edge emitting lasers. For this category, light travels parallel to the active region. The transverse waveguide is designed and fabricated during growth. The lateral waveguiding is achieved by creating a ridge surrounded either by air or some regrown semiconductor. Finally, the mirrors to define the cavity are normal to the surface of the wafer and can be realised either by cleaving (stand alone devices) or by etching (integrated lasers).

To begin cavity analysis one has modeled the waveguide created by the material heterostructure. This gives information about radiation leak towards the substrate or overlaying semiconductor layers that absorb. Furthermore, information about the radiation intensity profile and the modes that are supported are deduced. Once the lateral refractive index profile is created by ridge formation, the same procedure is followed to obtain the lateral modes. These modes define the far field behavior of the device and the maximum intensity that may be emitted by the structure. Finally the information gained about the propagation constant that depends on the lateral and transverse modes, are used to obtain the effective refractive index for each mode that may lase and the corresponding far field characteristics.

Since light is reflected from the mirrors at each end of the cavity, a new relation has to be satisfied by the traveling wave in order to be amplified. After one round trip into the cavity, the reflected radiation is back at the beginning of its path. In order for such a beam to survive the reflected wave has to be in phase with the initial one. This is called the **"round trip phase rule".** If a wave does not satisfy this rule, the reflected part is

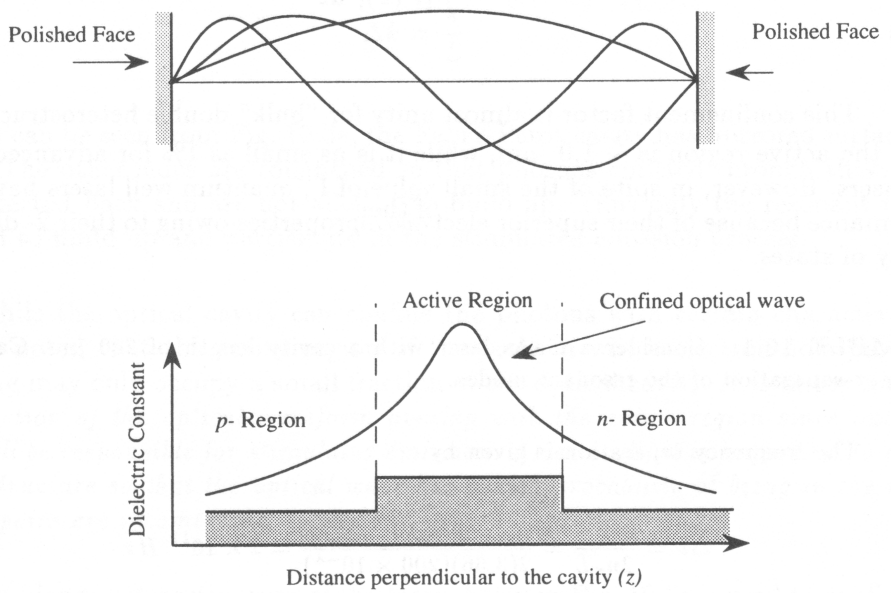

Figure 1.9: Longitudinal modes and transverse profile of the optical beam in a cavity. Reprinted from [2]

out of phase and the total intensity is reduced. On the contrary if a mode satisfies the above rule, the reflected part is in phase with the initial wave and the intensity adds-up. If there is a cavity of length l and a mode is traveling inside it with effective refractive index n_{eff}, then the modes that can be sustained will be given by the simple relation:

$$l = \frac{m\lambda}{2n_{eff}} \qquad \text{Equation 1.23}$$

m is an integer that is usually a large number and is called the **mode index**. Within each longitudinal mode there can be several lateral or transverse modes.

As in conventional lasers, light has to travel many times through the structure to be amplified. The mean distance a photon travels inside the laser device before it escapes, is usually larger than the actual length of the device. This actually depends on the escape probability per round trip or, in other words, the survival factor of the cavity.

In gas lasers, the reflectivity of the mirrors is close to 99%. This results in a mean photon lifetime which is very large compared to the round trip time inside the cavity. In order to obtain amplification, the photon losses per round trip have to be balanced by the gain process inside the active region. This means that for a gas laser, only a small amplification of the photons inside the cavity is enough to sustain laser oscillation. The situation in a semiconductor laser is quite different.

Typical reflectivities of a semiconductor laser are in the order of 30% which means that only a small fraction of the photons survive through a round trip inside the cavity. This in turn means that the gain needed to sustain lasing has to be equally large. In the following section we shall gain some insight into the optical amplification mechanism in a Laser diode.

1.3.1.3 .Gain characteristics

So far we have neglected the fact that for intense radiation and high carrier concentration, there is a non negligible probability that stimulated emission may take place. A powerful approach to deal with this situation is Einstein's two level medium.

According to this, there can be:

a) Absorption with rate B_{12}

b) Spontaneous emission with rate A_{21}

c) Stimulated emission with rate B_{21}

and two populations, one being the number of excited carriers (N_2) and one being the number of non excited ones (N_1). Exactly like the van Roosbroeck concept, under thermal equilibrium, the upward transition must exactly match the downward ones. Taking into account the Black body radiation pattern, we finally conclude that:

$$B_{12}=(\frac{g_{D2}}{g_{D1}})B_{21} \text{ and } \frac{A_{21}}{B_{21}}=\frac{8\pi v^3 n_r^3}{c^3} \qquad \text{Equation 1.24}$$

where $g_{D1,2}$ are the degeneracy numbers for the valence and conduction bands respectively, which are the same in a semiconductor so we can neglect them. If we assume a light beam with N_p photons traveling through a semiconductor sample, we can relate N_p, N_1 and N_2 through the following equation.

$$-hv\frac{dN_p}{dt}=(N_1-N_2)N_p hv B_{21} \qquad \text{Equation 1.25}$$

In order to obtain this equation, we have assumed that no spontaneous emission takes place. The reason for that is twofold. A spontaneously emitted photon is NOT in phase nor does it have the same heading as the light beam. In a non-perturbed semiconductor, N_p becomes smaller with distance since photons are absorbed. This is predicted by eq 1.25 since N_1 is larger than N_2 (Boltzmann equation predicts this). If we could get a semiconductor to have $N_2 > N_1$ then the opposite would happen. Light traveling inside the sample would gain photons instead of losing. This is exactly the situation one needs in order to get gain and therefore lasing in a material. In a semiconductor specifically there is no discrete excited state but a continuum called conduction band. If we write down the equations that give us absorption and stimulated emission rates we get:

$$r_{abs}=P[1-f_n(E_2)]f_p(E_1)N_p(E) \qquad \text{Equation 1.26}$$

$$r_{st}=P f_n(E_2)[1-f_p(E_1)]N_p(E) \qquad \text{Equation 1.27}$$

Where P is the probability of the given transition and f are the respective fermi occupation probabilities, for electrons (f_n) and holes (f_p). E_1 and E_2 are the energies related to the states in question.

Obviously, we must have $r_{abs}<r_{st}$ in order to get net amplification of the light beam. It is easily proven that this is satisfied if we have $E_{fn} - E_{fp} > E$ where E_{fn} and E_{fp} are the

Imrefs of the conduction and valence bands respectively.

If we see what happens for $r_{abs} = r_{st}$ we will see that the net change of photons will be zero, which means that the material is behaving like a transparent medium. This is called transparency level and at this point $E_{fn} - E_{fp} = E_p$.

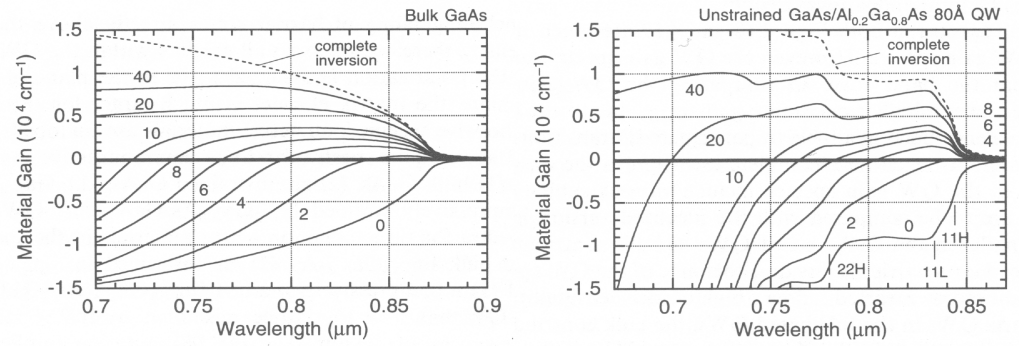

Figure 1.10: Gain in bulk (a) and Quantum well (b) for different carrier concentrations Reprinted from [2]

In a laser device, each time a photon passes through the cavity, there is a finite probability that it will escape through the mirrors at the end. In order to get a constant number of photons inside the cavity, there is a need to exceed the limit of transparency. We also need to compensate for photons that are scattered out of the light path by some imperfections. If we assume that the cavity introduces losses γ per unit length and that the reflectivites of the mirrors at the end of the cavity are R_1 and R_2 then we can right down the intensity of the light after it completes one round trip inside the cavity. This will be: $I = I_o R_1 R_2 e^{2(g-\gamma)l}$ Equation 1.28

At the point where laser oscillation is barely surviving (at the threshold) we should have $I = I_o$ which results in gain g_{th} per unit length equal to:

$$g_{th} = \gamma + \frac{1}{2l}\ln\left(\frac{1}{R_1 R_2}\right) \quad \text{Equation 1.30}$$

Equation 1.30 provides a useful tool to estimate the gain needed by a device to reach threshold.

So far we have assumed that the gain area, and the core of the waveguide where the optical mode travels, coincide. This holds true for bulk lasers. However, quantum well lasers have a different layout. The quantum well is quite narrow and the core of the waveguide is made up of a non absorbing material. In that case, the interaction of the propagating mode with the active region is not complete. In a sense, the part of the mode that is traveling in the core but outside the quantum well can not interact with carriers. To correct eq. 1.30 for this case, we need to multiply the left side with the percentage of the light that travels inside the active area, namely the quantum well. This fraction is usually depicted by the symbol Γ and the product Γg_{th} is called the **modal gain**.

1.3.2 .Outlook of a device

Given the above, a simple laser diode should look much like the following image.

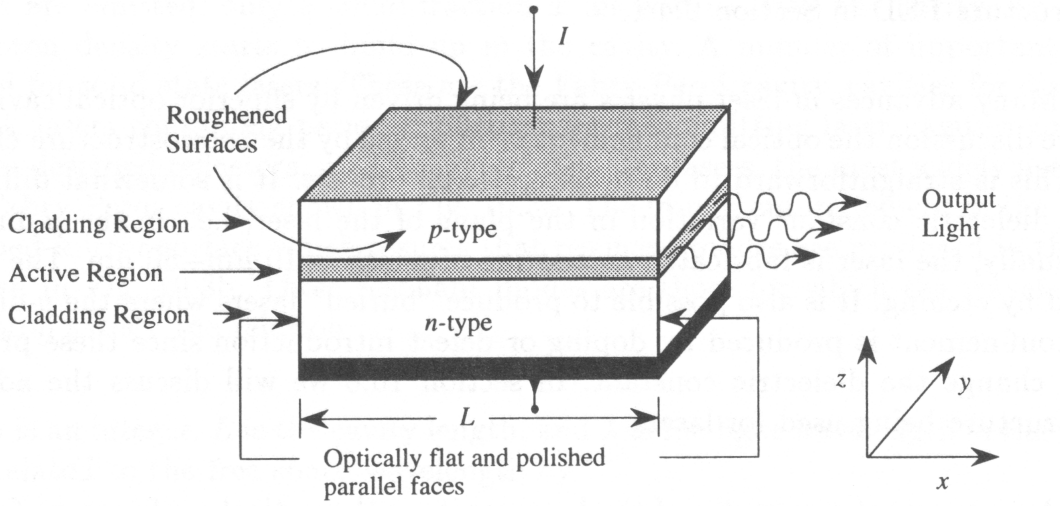

Figure 1.11: Cleaved LD. The emission occurs from the side facets. Reprinted from [3]

As one can see the current is flowing through the top – bottom contacts and the regeneration – gain process occurs in the active region. The optical cavity is formed by the parallel surfaces.

Section: 1.4 .Photodiode design

1.4.1 .Theoretical background

As previously described, if a light beam travels inside a semiconductor, absorption will occur provided the photon energy is large enough to match the bandgap of the material. All semiconductor photodetectors are based on this phenomenon. The idea is to convert light into carriers and then collect and measure them. There are however many concepts concerning the way photo generated carriers are collected and measured.

The simplest idea is to have an intrinsic piece of semiconductor, put two electrodes on opposite sides and apply a voltage. As soon as carriers are created, they drift towards the electrodes depending on their charge and are collected. This creates a current which we can measure. This realization is called a photoconductor. It is important to point out that a photoconductor needs bias to function. If there were no bias there would be no electric field to set carriers into movement and they would soon recombine. One understands from the last sentence that the time of travel inside the material for each carrier has to be far smaller than the recombination lifetime. If it were not so, carriers would be lost due to recombination. The efficiency of such a detector can be quite large. In order to have a quantitative measure of the efficiency of a detector we use the **quantum efficiency** which is given in eq. 1.31.

$$n=\frac{I_{ph}/q}{P_i/h\nu}=\frac{I_{ph}}{q}\frac{h\nu}{P_i}$$ Equation 1.31

Where I_{ph} is the current induced by the light and P_i is the optical power incident on the device. Actually this is the number of carriers produced divided by the number of photons incident on the device. This is also termed **external quantum efficiency** in contrast to the internal quantum efficiency which is the number of carrier pairs created divided by the number of photons absorbed. Typically the second one is very high whereas the first one may vary, depending on the absorption and other parameters.

Another figure of merit for photodetectors is the Responsivity (R) which is given by the following equation.

$$R=\frac{I_{ph}}{P_i}=\frac{n\lambda(\mu m)}{1.24}\left(\frac{Amper}{Watt}\right)$$ Equation 1.32

The second equality merely present a useful form of the original equation. Eq. 1.32 is one of the most characteristic values of a photo detecting device, the larger it is the better the photodetector.

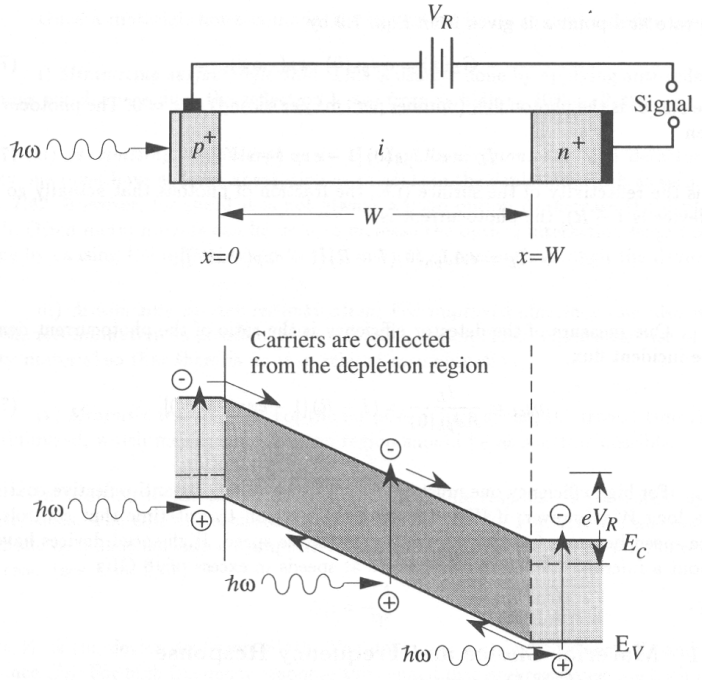

Figure 1.12: Concept of a photodiode. Actually one uses a reverse biased PIN diode (a). The carrier flow diagram explains the idea (b). Reprinted from [3]

Developing further the idea of a photoconductor one can replace the ohmic contacts with Shottky ones. In that case the detector is called MSM after the Metal Semiconductor Metal photodetector. The advantage of such a scheme is easier fabrication and faster response.

The next idea is to have a pin diode (Fig.1.12). As we have already seen, in a PN diode, there is a built-in voltage V_{bi}. If we introduce an intrinsic area between the P and N sides, the depletion region expands to include the entire I area. In such a device, light

will produce extra carriers in the depletion region and they will drift towards the respectively doped regions depending on their charge. Theoretically, one needs no external bias for such a device to work. Practically, a small reverse bias is applied to enhance the built in electric field, thus improving carrier collection.

Normally there are two current components in a PN diode, J_{drift} and J_{diff}. They add up to form the net current flowing through the device. If we consider thermal generation of carriers to be negligible, then the drift component can only originate from carriers that are generated by incident photons. Using the continuity equation and Poisson's law, much like we did for the PN diode analysis, we can find the diffusion component. Adding both we get:

$$J = -q\frac{P_i}{h\nu}\left(1-\frac{e^{-\alpha w}}{1+\alpha L_h}\right)-qp_n\frac{D_h}{L_h} \qquad \text{Equation 1.33}$$

Where p_n is the minority carrier density -and therefore very small. Given eq. 1.33 we can see that the current is proportional to the intensity of the light impinging on the device. A word of caution here concerns the fact that light coming from outside the semiconductor will reflect on the surface, thus only a fraction of it will reach the intrinsic absorbing area. This is not accounted for in the equation given above.

Finally it should be mentioned that other type of photodetectors also exist but are out of scope in this brief introduction.

1.4.2 .Photodiode design issues

For the purpose of our work, there exist a number of prerequisites concerning photodetector design. The light that we need to detect travels parallel to the substrate and has a wavelength which is very close to the bandgap energy of the active material used for the laser devices. Actually if heating and band renormalization effects are taken into account the wavelength emitted from the laser diodes could be marginally below the band gap of the active quantum well material. Furthermore, we might need to detect small intensities as the beam produced by a laser travels through a long waveguide and is then delivered to the photodiode.

The easiest concept to realize without adding extra layers to the already complicated structure is to use the same PIN structure that is used for lasers as a PIN photodiode. This concept is easy to implement since the structure already exists as well as the fabrication steps required to create the p and n contacts. The only drawback of such an implementation is the fact that our structure, being designed for a laser device, has small absorption coefficient. This translates into a large photodetector, if we want a significant electrical signal originating from the detection devices. One thing that is granted naturally with this approach is the fact that we can create a photodetector that works as a waveguide. Once the light beam is directed into the device it is waveguided and this allows us to build up interaction between the weak absorption and the traveling beam. Finally, biasing the structure results in a favorable phenomenon. As the electric field builds up in the depletion region, the quantum well that constitutes the absorbing

material obtains a stark – shift. This red shifts the absorption edge. The consequence of this effect is that even if the laser operates below the absorption edge of the quantum well, the photodetector absorbs strongly and thus provides a large signal.

Section: 1.5 .Combining everything in a single structure

Although low temperature GaAs/Si wafer bonding provided us with a solution to implement optical devices attached on a material such as Silicon which by nature is a lost cause as far as high end optoelectronics are concerned, there are several limitations posed by this technological innovation.

First of many is the fact that one has to take into account the heterogeneous nature of the wafer (GaAs/SOG/Silicon) and avoid elevated temperatures that would stress the system mechanically.

Secondly, one has to process GaAs into devices, respecting circuits present on the Silicon wafer. In other words, prolonged exposure to elevated temperatures is out of the question since that would lead to diffusion in the Silicon and therefore render devices such as transistors useless.

To conclude, special care must be taken during processing of GaAs into devices (this issue will be discussed later) and no potential for regrowth of GaAs material exists. The later is a solution often used in order to provide different material structures for laser diode and photodetector on the same wafer. The remaining solution being to implement all devices from a single structure, one has to take into account all together laser diodes, photodetectors and waveguides.

Combining the ideas of a laser diode and a photodetector device in a single structure are somewhat conflicting. To add to the complexity of such a design, a waveguide has to be implemented from the very same structure as well.

In the next two chapters one may find the reasoning behind our choice of structure, as well as the processing details that were resolved for such an implementation to work.

Chapter: 2 .Material preparation

In this chapter, issues regarding material will be discussed. After a short description of the available equipment, the structure that was used will be described along with explanation of the choices made. Finally, special considerations regarding bonded material processing will be presented and necessary modifications made to the structure will be described.

All samples discussed in this work were grown using a VG80H Molecular beam epitaxy (MBE) reactor, equipped with a series of sources in order to be able to grow $Al_xGa_{1-x}As$ as well as $In_xAl_yGa_{1-x-y}As$ compounds. MBE is nowadays considered a mature growing technique, able to provide structures with accurately engineered quantum wells as well as samples with very low defect density. The later is pointed out, since it plays a crucial role to the successful outcome of material bonding as described elsewhere.

Section: 2.1 .GaAs structure

Following the discussion of section 1.3, it is clear that the structure should contain some gain media (namely quantum well's) and some sort of waveguiding effect in order to create the optical resonator. Combining $Al_xGa_{1-x}As$ with different mole fractions of Aluminum – therefore different refractive indices - with GaAs quantum wells one can readily create a structure with the desired properties. Such a structure is tabulated below.

Material	*Mole fraction*	*Thickness(μm)*	*Doping*	*Utility*
GaAs	0.00	3	$> 2\ 10^{18}$	N+ contact
AlGaAs	0.45	1.4	$1\ 10^{18}$	N+ cladding
AlGaAs	0.45 – 0.26	0.1	$1\ 10^{17}$	N cladding
AlGaAs	0.26	0.19	Undoped	N clad. conf.
AlGaAs	0.26-0.2	0.10	Undoped	N graded conf.
AlGaAs	0.2	0.005	Undoped	Spacer
GaAs	0	0.008	Undoped	OW 1
AlGaAs	0.2	0.005	Undoped	Barrier
GaAs	0	0.008	Undoped	OW2
AlGaAs	0.2	0.005	Undoped	Barrier
GaAs	0	0.008	Undoped	OW3
AlGaAs	0.2	0.005	Undoped	Barrier
GaAs	0	0.008	Undoped	OW4
AlGaAs	0.2	0.005	Undoped	spacer
AlGaAs	0.2 - 0.26	0.10	Undoped	P graded conf.
AlGaAs	0.26	0.19	Undoped	P confinement
AlGaAs	0.45	0.6	$1\ 10^{17}$	P cladding
AlGaAs	0.45	0.10	$1\ 10^{18}$	P+ cladding
GaAs	0	0.25	$>2\ 10^{18}$	P+ contact
AlAs	1	0.1	Undoped	Etch stop
GaAs	0	400	$>2\ 10^{18}$	Substrate

Table 2.1: Typical structure for this project. Observe the graded layers as well as the AlAs layer to be used as etch stop. This is an inversed structure to be bonded on Si. Structures for comparison

are grown inversed and without the AlAs layer.

Section: 2.2 .Silicon processing

In order to demonstrate the concept of optical interconnects, a set of circuits was designed and fabricated on the Silicon wafers before bonding. This task was performed by the team of Dr. G. Halkias at IMEL, Demokritos. The simplest approach would be to include a laser driver and a current amplifier in order to drive the laser diodes and extract the signal from the photodetectors respectively.

Silicon circuit characteristics will be shortly reviewed hereafter.

2.2.1 . Silicon laser driver

Laser diode driver can be described as a current source able to switch on and off fast enough in order to modulate the output power of a laser. The device implemented on the demonstration wafers were designed [10] to provide maximum current of 40mA with switching times less than 1nsec.

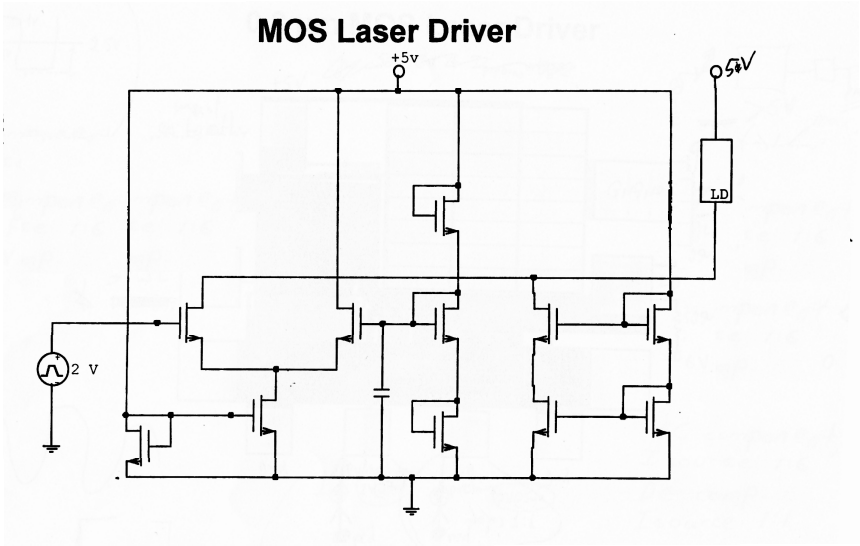

Figure 2.1: Laser driver schematic based on CMOS technology. This is implemented on Silicon using AMS foundry. Reprinted from [4]

2.2.2 . Silicon photodiode amplifier

A photodiode alone is best described as a current source. Typically Silicon circuits operate using voltages and not currents. It is clear that an interface circuit is necessary to convert the photodiode signal into usable voltage signal for the silicon circuit. [11] This is the task performed by the receiver circuit fabricated on silicon. This circuit is classified as a trans-impedance amplifier (TIA) meaning that input impedance is as low as possible (remember it's a current input not voltage) and the output impedance is high (voltage output). [12] Typical current signals coming from the photodiode are in the order of μA and output voltages should be in the order of Volts thus the gain required

by this circuit is approximately 10^5Volts/Amp.

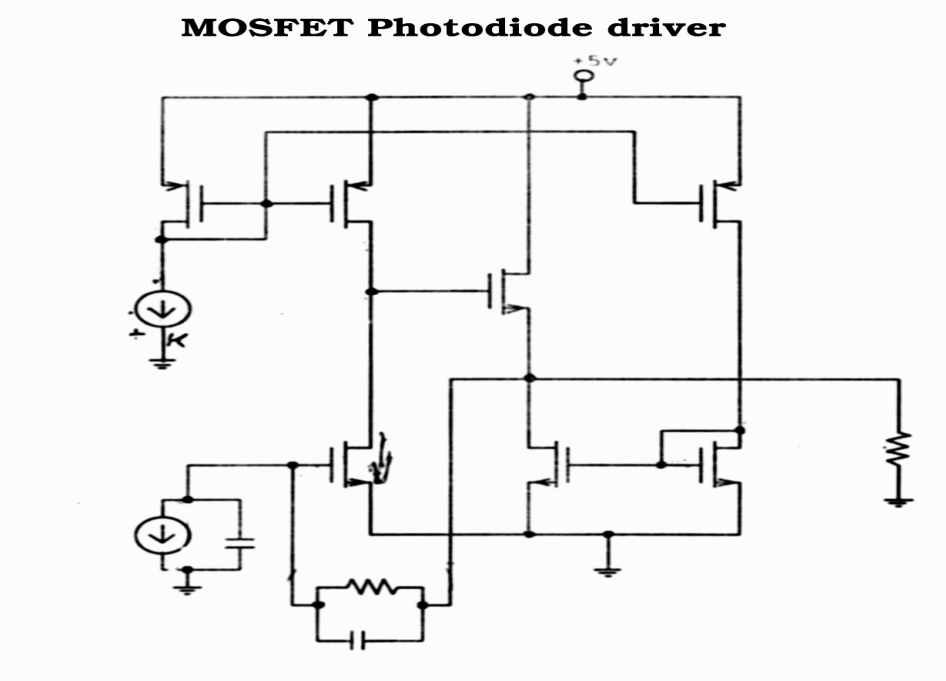

Figure 2.2: Photodiode driver based on MOS Silicon technology. The current source (bottom left) is the photodiode equivalent. The resistance (right edge) is the load equivalent. Reprinted from[4]

Section: 2.3 .Low Temperature Bonding

The core of the entire project is bonding of two different wafers face to face. First a silicon wafer, processed with potentially complex circuits and secondly a GaAs wafer that provides the direct band gap semiconductor material to process into optical devices.

Early attempts were made to grow epitaxially GaAs on Silicon. [13] Although lattice mismatch between the two materials is beyond the point that can be accommodated through elastic deformation, GaAs layers were successfully grown on silicon. That method suffered from several drawbacks. To start with, silicon should not be processed before GaAs overgrowth since elevated temperatures are needed to grow good quality crystal. Furthermore, processing silicon requires high temperatures (1000ºC) for diffusion which is non compatible with GaAs as the later decomposes in temperatures above 400ºC. Last and most important is the fact that GaAs grown epitaxially on silicon suffers from high dislocation density as well as large residual stress. Dislocations and stress are considered a major problem as far as optoelectronics are concerned since even one dislocation in a device can render it useless (leak currents, non radiative recombination e.t.c.).

The concept of wafer bonding gives an alternative approach to these issues. One may process silicon in a typical fashion having low cost production, grow the GaAs structure on a completely separate wafer homo-epitaxially – growing high quality layers- and

then "stick" the two wafers together face to face.

In order for this idea to work a low temperature "gluing" agent is necessary. This material should be easy to apply, have mechanical properties that match those of the two wafers and be able to withstand thermal processing up to the point were GaAs contact annealing traditionally takes place.

2.3.1 .Gluing agent

The material of choice was spin on glass (SOG). SOG is a polymer named **methylsyloxane** dissolved in volatile material. Initially one can spin the material onto the surface and then bake it at moderate temperatures in order for the solvents to evaporate. The first step in the LT bonding sequence, is to cover one or both wafers with SOG. Then the two wafers are brought face to face and a pressure is applied to remove any air bubbles trapped between the two wafers. This is actually done under an IR microscope. Infra red, is below the band gap of both GaAs as well as Silicon. This means that the wafers appear transparent at this wavelength. This allows for real time inspection of the bonding process. Any air bubbles trapped between the surface, refract the radiation. This is viewed as a bright spot and pressure is applied in order to drive the bubble towards the edge of the substrate. After this process is completed, the two wafers are baked at 200 °C for several hours. This drives the solvents out of the SOG and turns it into a solid film. The next step is necessary to convert methylsyloxane into an inert substance.

The resulting film is solid in room temperature but liquefies at 200ºC. This is because there is not enough energy at 200ºC to decompose the chemical compound and thus convert it into an inert substance. This is accomplished by annealing at temperatures as high as 350ºC , structural changes turn the material into a glass like substance that is inert and has mechanical properties very close to that of Silicon dioxide. In the process, certain chemical substances are evaporated from the film.

After bonding is achieved, the GaAs wafer is no longer needed. Silicon is now the mechanical carrier of the active GaAs layers. Subsequently the GaAs substrate is removed using a combination of wet and dry etching techniques. As described earlier an AlAs layer is added below the active structure when growing the GaAs structure . This very layer is used in conjunction with a selective dry etch process to remove entirely the GaAs wafer without damaging the active layers.

Finally what is left, is a fully processed silicon wafer, covered with SiO_2 and carrying on top a thin film (3-6μm) of GaAs. The GaAs material is then processed starting from what used to be the back side of the GaAs wafer. A thorough description of the bonding – thinning process will be presented when processing of bonded material is presented. (see chapter 4 p.51)

Chapter: 3 .Processing of GaAs devices

In this chapter, implementation of optoelectronic devices on GaAs is presented. The optical interconnection scheme was initially fabricated on plain GaAs wafers. This was done in order to pinpoint possible design flaws as well as to evaluate the concept without being troubled by problems that could rise due to increased complexity when processing bonded material. Chapter 4 will present the final implementation on bonded material.

Another reason for following this step by step fabrication is to provide ourselves with reference devices. This way one may compare device performance, both to theoretical models as well as to final devices, thus gaining some insight into what actually affects the behavior of the fabricated devices.

Section: 3.1 .Processing of Semiconductors

By processing we mean the entire procedure that transforms a crystalline material like a GaAs wafer into operating devices. By definition processing is sequential in the sense that everything is performed on the entire wafer, layer by layer. Each layer is a building block of the final topography and can be one of many possible procedures that are described thereafter. Each time a layer is to be completed, some means to define the planar geometry is needed. Depending on the technology used, either the beginning or the end of a step is pattern definition.

Let us presume that we need to remove material from a specific location on the surface of the wafer. Since patterns are really small and the shape of the area to be etched is possibly complex, the easiest way to define this is to protect everything with an inert material and expose only the areas to be etched. Then immerse the sample in a chemical solution that attacks the semiconductor, wait for a well determined period of time and then rinse everything away to stop the process. What about the pre- shaped inert material? Well the easiest way to achieve this is to “copy” the pattern from a prototype.

3.1.1 .Lithography

In order to etch, deposit metal or insulator onto a wafer one needs a way to define the shape each of the above will eventually have. Technology has provided us with chemicals that react to light or electrons much like a photographic emulsion. These are called resins. There are photo-activated resins (Photoresist) as well as electron activated resins (E-beam resist).

It has long been established that if one tries to focus a light beam to a very small area the best one can do is create a spot with dimensions similar to the wavelength of the light. This is why when small patterns are to be created small wavelengths are needed. Contemporary photo-lithography operates in the UV region (e.g. 350nm or 240nm) Thus the smallest feature we can copy is approximately that big. Light is manipulated with optics so that a large aperture, parallel and uniform intensity beam is created. The prototype of the pattern is engraved on a thin metallic film supported by some

transparent material (Quartz or Borosilicate) defining transparent and opaque areas. This plate is placed facing down on the sample to be processed and a specific dose (intensity x time) of light passes through. This causes chemical reaction on the emulsion that is subsequently immersed in a developer that selectively removes the exposed (positive resist) or unexposed (negative resist) areas. Thus the pattern is transferred onto the sample.

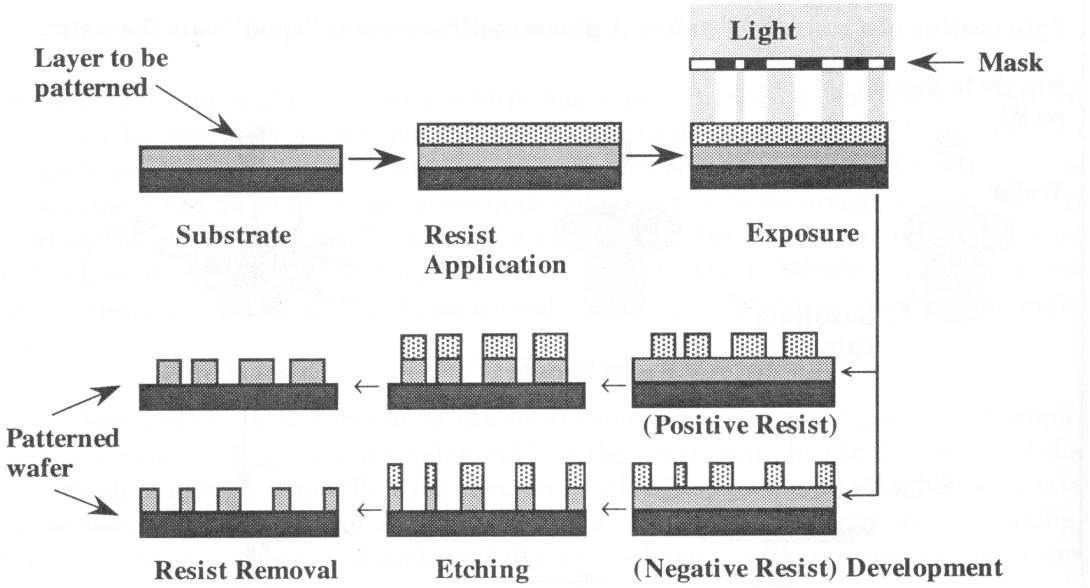

Figure 3.1: Lithography concept, applied in an etching step. Reprinted from [3]

For patterns much smaller than typical wavelengths, the focused electron beam is used. Since there is no way to create a prototype plate that is transparent to electrons, special tools are used (e-beam writer) to expose the emulsion to certain doses of energetic electrons. The effective de Broglie wavelength of an electron accelerated to a few KeV is so small that it is easy to focus the e-beam to spots as small as a few nanometers. Thus very small geometries are defined.

In conclusion it should be noted that photolithography is orders of magnitude cheaper than e-beam lithography and much faster since an exposure of a few seconds can pattern a 6" substrate whereas e-beam (direct writing) is slow. This is why photolithography is very popular and e-beam is used only when absolutely necessary.

3.1.2 .Metal evaporation

A device needs ohmic or/and Shottky contacts in order to work. Additionally metal interconnects are materialized on a semiconductor circuit to connect several devices together forming a complex circuit. Metal is evaporated or sputtered on a patterned substrate by means of thermal evaporation or e-gun evaporation in a vacuum chamber. After the metal coats everything, the photoresist is removed leaving metal only in the initially exposed areas. This technique is called lift-off and is widely used in III-V semiconductor processing.

Alternatively, the uncoated substrate is sputtered with metal and then photoresist is

applied and patterned and the unwanted metal is removed.

In our lab we use the lift-off technique to deposit metals in conjunction with a Temescal e-gun evaporator. The strong point of this process is that many different metals can be evaporated and the sample is not exposed to strong chemicals that could potentially damage it.

3.1.3 .Semiconductor Etching

Semiconductor material is removed by two ways.

Wet etching is frequently used to isolate devices or whenever the etching profile and depth is not critical. Many solutions attack GaAs based material and they provide different etch rate and uniformity results. The choice of one chemistry over the other has to do with the desired depth of etching, the other exposed materials and the desired profile.

Dry etching is considered to be high end, it is much more complex, expensive and time consuming but can achieve high quality results both in terms of uniformity as well as control over the etched areas and etch profiles. In the following section a short description of the concept of dry etching is developed. This is necessary to explain the decisions made regarding mirror etching.

3.1.4 .Dry etching basics

Dry etching utilizes a plasma to etch the surface of a material. Unlike wet etching where the ions in a solution react with the etched material and thermal kinetics apply, the dry etching technique is based on a low pressure gas (10 – 200mTorr) that is dissociated into particles by means of an alternating electric field. [14]

The chamber in which the process takes place is initially pumped by a vacuum system to low pressure (typically 10^{-6} bar). This is done to remove the air surrounding the sample. After a controlled flow of special gas is introduced (usually gases containing Cl or F and/or inert gases like Ar or N). The chamber is made up of two parts, one is the surrounding wall which is grounded and the other is a flat electrode on which the sample is put. An RF[i] generator creates alternating Voltage which is applied on the electrode. The electric field is strong enough to break up some of the molecules in the gas. The electrons that are created, accelerate from the alternating field and execute an oscillation. It is quite possible that during this oscillatory motion the electrons collide with some other molecule/atom. Then a number of processes can occur:

1. Excitation

The electron excites one or more bound electrons from the molecule or atom into a higher state. The energy is absorbed from the collision. The excited atom will finally emit a photon when returning to the ground state. This is the reason why we see a glow coming out from the plasma. The emitted photons are characteristic of the atoms existing in the chamber and this provides a tool to monitor the spieces that exist in the

i Radio Frequency

chamber.

2. Dissociation

If the energy of the accelerated atom is enough to break a bond in a molecule, dissociation occurs. This usually provides atoms from a complex molecule. This process is very important since the free atoms are chemically active and react with the sample to be etched. The resulting atoms are called radicals.

3. Ionisation

It is also possible to have ionization. This process emits one electron leaving the ionized molecule or atom positively charged. These positively charged atoms or molecules are also chemically active and the fact that they carry a charge means that they are also accelerated by the alternating potential. This provides an additional interaction with the sample. The physical etching.

As soon as the RF field is initiated, an avalanche effect takes place. The dissociation process provided large number of electrons that increase the rate at which all these effects happen. Keeping in mind that electrons are very light when compared to charged particles (more than 1:1000) their oscillatory motion is much larger. Close to the electrode, the electrons will hit the surface if they are close enough and get trapped there, charging the electrode negatively. The same effect happens on the surrounding walls. However the walls are grounded so these charges do not accumulate.

Back at the surface of the electrode, the charging effect can build up since the electrode is not connected to the ground. As soon as the voltage of the electrode changes, the electrons close to the electrode are repelled further away whereas the positively charged particles are attracted. Finally, a steady state is reached when the rate at which electrons hit the surface of the electrode, matches the rate of the positively charged ions. The potential difference on the electrode is called the DC bias. The area above the electrode where no electrons reside (because they are repelled from the negative potential) is called the seath and is visible by eye since collisions that excite the spieces are different in that area. Seath thickness ranges from a few mm to tenths of mm depending on the process parameters. In this area, the positively charged ions see the potential difference and are accelerated towards the electrode. There is nothing to stop this motion (apart from collisions) and this results in a bombardment of the electrode's surface with positive ions. This creates a physical etching mechanism on the surface of the sample.

The combination of all the above processes leads to a very complicated behavior of the plasma etching. Usually semiconductor engineers work on a trial and error bases to find the necessary parameters for a specific etching

3.1.4.1 .Physical etching

As explained, the charged ions are accelerated by the seath's potential and hit the surface of the electrode and the sample with a high kinetic energy component. This may remove atoms from the surface of the sample. This process is called sputtering. Since

this is a mechanical interaction, it etches the surface downwards without etching

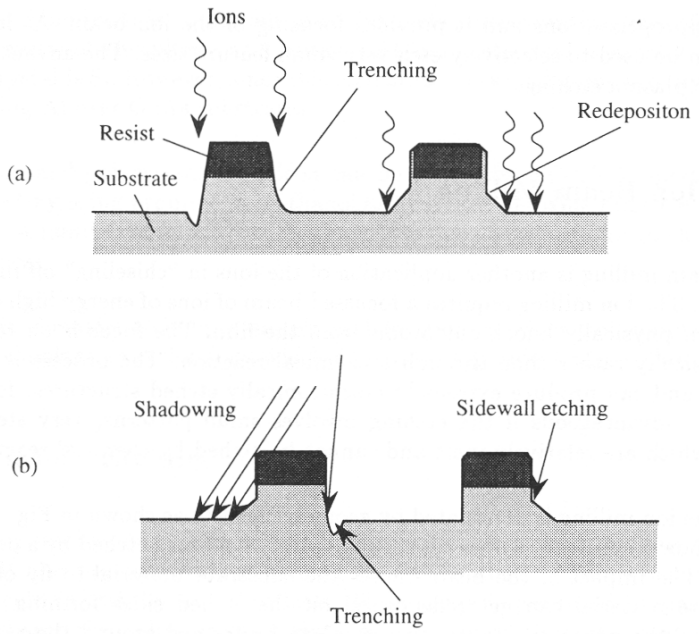

Figure 3.2: Some of the typical features of Dry etching procedure. Reprinted from [3]

sideways. This is expected as acceleration takes place normal to the surface.

The energy that is needed for such a process to occur is relatively high. This is why when the DC bias is low, physical etching may not take place at all. As one may understand, depending on the material that is etched, a different threshold of kinetic energy is needed. This process is not selective between semiconductor materials since their bond strength is not very different. Finally, since the charged ions are rare ($1:10^6$) this process is relatively slow compared to the chemical etching described below.

3.1.4.2 .Chemical etching

A different mechanism to etch is chemical reaction. As stated earlier, radicals and ions may be chemically active. This means that if they come in contact with the semiconductor surface they may react chemically and form some product. If this product is volatile it will diffuse out of the surface and the process may go on using reactant spieces that will diffuse in. This process depends on the materials chemical structure as well as the reactant spieces that are created in the plasma. Since this is a chemical reaction it is essentially independent from the kinetic energy of the reactant spieces and this is why it is happening even at low DC bias. The energy needed for the reaction is actually provided at the time the gas molecule is dissociated inside the plasma. Most active spieces are usually neutral and they simply diffuse towards the surface of the sample.

Volatility of the chemical products is an important issue. If the products of the chemical reaction are not volatile, they form a barrier at the surface of the sample which inhibits both chemical and physical reaction. Since the concentration of chemically

active spieces may be high, chemical etching may provide high etch rates.

3.1.4.3 .Ion enhanced etching

The actual picture of etching in a gas chamber, is actually more complicated. The sputtering mechanism may not only expunge atoms from the lattice of the semiconductor but it may destroy the lattice. In other words energetic ions may destroy the structure creating dangling bonds and or non volatile compounds that stay on the surface of the sample. However these compound products having a different structure may be prompt to chemical reaction that would otherwise not happen. This increases the etch rate and maintains the directionality of the sputtering since damaging occurs mainly on the horizontal surfaces of the sample. This process is faster than sputtering as chemical reactions speed up etching of the sample. The only drawback of such a process is a thin sacrificial layer that is composed of damaged semiconductor material and may pose operational problems to devices that are sensitive to surface damage (Shottky contacts, photodiodes e.t.c.). The damage level usually is a function of kinetic energy (i.e. DC bias), density (i.e. pressure) and ion mass (i.e. gas type). In the following paragraph we will shortly describe the parameters that one may tune in a dry etching chamber.

3.1.4.4 .Dry etching parameters

The result of a dry etching process can be controlled via a number of parameters like gas flow, gas type, RF power and chamber pressure.

3.1.4.4.1 . Chamber Pressure

The mean free path between collisions in a plasma chamber is controlled by changing the pressure of the gas introduced inside the chamber. Higher mean free path results in higher kinetic energy, more dissociation collisions and higher probability that an ion reaches the surface. Conversely, high pressure leads to less energetic ions, higher density of atoms and less dissociation collisions. From the above it is obvious that at low pressures it is likely to get chemical dominant etching (i.e. High etch rate, isotropic etching) whereas for low pressures physical dominant etching occurs.

3.1.4.4.2 .RF power

The RF power is controlled be means of changing the amplitude of the electric field. The frequency of the generator is not tunable and is usually fixed at 1.256MHz (This frequency is dedicated to RF power applications so that no interference is created to radio equipment). Higher electric field means that the oscillatory motion of the charged particles is stronger and therefore higher kinetic energy is obtained. This in turn leads to higher probability for dissociation and therefore more ions are present in the chamber when the RF power is increased. Furthermore, the velocity of the ions that hit the semiconductor is higher and this leads to enhancement of the mechanical etching. The drawback of using high RF power is twofold. First, damage is more on the sample and secondly, there is a need for harder material to protect the areas not to be etched.

3.1.4.4.3 . Gas flow

As etching takes place, the gas components that react with the sample are consumed. This means that their concentration drops inside the chamber. Therefore there is a need to replenish the gas with fresh one. The rate at which new gas is coming in is controlled be the flow measured in standard cubic centimeters per minute (sccm)[i]. A very small flow would result in reactant spieces depletion leaving only inert particles to perform sputtering. A very high flow may result in decrease of dissociated particles inside the chamber, therefore less chemically active spieces for the process to proceed. The controlling parameter is called residence time and is actually a measure of how long a particle will stay inside the chamber before being sucked out by the pump.

3.1.4.4.4 .DC Bias

Although the DC bias is not controlled directly, it depends on power and pressure. Since the dc bias is directly proportional to the energy that the ions attain inside the seath, it is also directly proportional to the mechanical component of the etching process. Usually, depending on the process that we want to have, the DC bias is tuned to high or low values (typically between -10 to -200 Volts).

3.1.4.5 .Selective dry etching

It is possible to achieve dry etching processes that are selective. Usually this is done by controlling the gas type as well as the parameters of the process. Only one example is known to the writer and it will be explained here.

Fluorine containing gases selectively etch non Al containing materials like GaAs and InGaAs. Fluorine reacts with Ga and In to form InF and GaF wich are volatile and diffuse out of the surface. This provides a fast chemical etching component. On the contrary, AlF is non volatile. Therefore as soon as an AlGaAs layer is exposed to the etching environment, Al reacts with Fluorine to form AlF which remains on the surface. This has two consequences. First, chemically active spieces are not able to reach the material because a film of AlF exists on the surface. This stops any chemical reaction. Secondly, the AlF film acts as a mask to energetic ions that hit the surface. This results in inhibition of mechanical etching as well. It is important to note that if the RF power is set to high, the AlF is sputtered away and the selectivity is destroyed. This process needs small DC bias (therefore small mechanical etching component to work efficiently). This selectivity is used in our project to remove the GaAs wafer while leaving the active layers unaffected.

3.1.4.6 . Our dry etching chamber

The dry etching equipment available for this project was a reactive ion etching fabricated by Vacutec. It is equipped with 4 pumps joined in two pairs, one pair for base pressure pumping (Turbo and mechanical backing pump) and one pair for process (Roots and mechanical backing pump). The base pressure that it can achieve is 10^{-6} Barr

i sccm flow = 1 cubic centimeter of gas measured at 1bar pressure, at 0 °C, in 1 minute

and it is equipped with several gases (Cl_2, BCl_3, CCl_2F_2, CF_4, SF_6, Ar and Oxygen). Gases that contain Chlorine and/or Fluorine are typically used in semiconductor processing because both atoms are chemically active.

The electrode is 22cm in diameter and is made of Aluminum. The RF power is driven to the sample electrode while the surrounding chamber acts as the grounded electrode.

Nowadays new systems have appeared that give more flexibility and have better performance. One of these is ICP[i] [15] which uses two RF generators, one to dissociate the gas and one to produce the seath. This decouples DC bias from the dissociation efficiency and can provide plasma with large number of radicals without increasing the damage on the sample. Such systems have been used intensively to produce high etch rate maintaining high directionality and low damage on semiconductor samples. Finally, new equipment are able to process samples at even lower pressures than 10mTorr, thus enabling very good etching of deep and small features.

3.1.5 .Insulator deposition

Insulating materials are required to isolate electrically crossing wires or conducting layers. There are two categories of insulating materials.

Spun on insulators: Polyimide and several other polymers are frequently used to create insulating layers. Initially the material is liquid and is spun on the wafer. A medium temperature annealing evaporates the solvent leaving a solid film that is patterned and finally, a high temperature process cross-links the polymer to make it inert to chemicals.

Deposited insulators: In case very thin, high quality insulating layers are needed chemical vapor deposition is used to deposit Si_xN_y or SiO_2. Although this process is much more complicated, the resulting layers are of very high quality and are used for capacitor dielectrics or MOS oxides. One very favorable characteristic of these processes is the fact that the sample is coated uniformly no matter the topography existing (i.e. side wall coverage).

3.1.6 .Annealing

Often there is a need to diffuse elements into a semiconductor. For example ohmic contacts are usually created by controlled diffusion of a predetermined metal on the surface of the semiconductor. This is done in a rapid thermal annealing chamber. Therein, the temperature can be varied with accuracy and speed so that small or no damage is done to the semiconductor but the necessary diffusion takes place. Keep in mind that a slow thermal cycle would mean more time at elevated temperature which in turn results in problems like evaporation of spieces (As in GaAs) or quantum well inter-diffusion

i Inductively coupled plasma

Section: 3.2 .General processing of a Laser - Waveguide - Photodiode system.

The final system that we want to fabricate for this project is illustrated in fig.3.1. One can see there is a need to fabricate laser diodes, photodetectors and waveguides on the surface of a wafer that in principle could be of any material. Wafer bonding has provided the material suitable for optoelectronic applications.

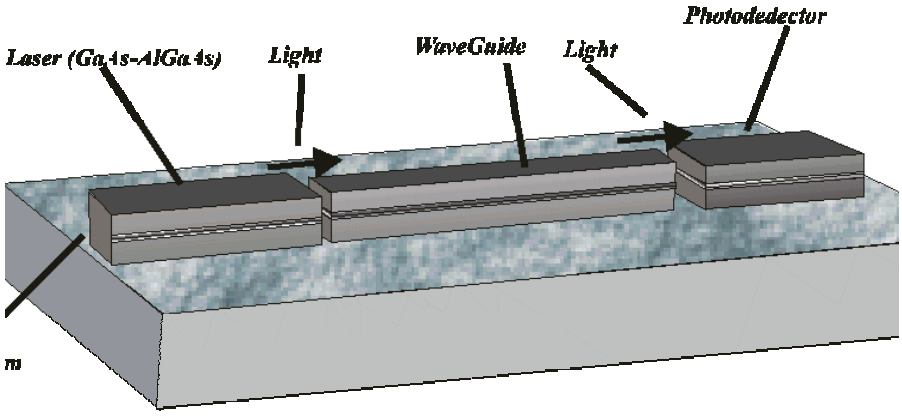

Figure 3.3: Illustration of the concept of an Optoelectronic IC.

The process flow is defined by basic steps as lithography, etching, deposition and annealing. A short description follows:

Ridge
Lithography AZ 5214
0.8um etch using $H_3PO_4/H_20_2/H_20$
P-contact
Lithography AZ 5214
Use Chlorobenzine x 10min before development
Typical p contact for GaAs,
anneal with recipee #8 in RTA
N-etch
Etch using $H_3PO_4/H_20_2/H_20$ down to n+ region
N-contact
Lithography AZ 5214
Use Chlobenzine x 10min before dev.
Typical n contact for GaAs
Anneal using rec #9 in RTA
Isolation
Lithography AZ5214
Etch 10sccm $BC1_3$, 2sccm CI_2 @ 50W,50mTorr
Polyimide
Spin poly, 5Krpm x 20sec

Spin 5214, normal, expose
Develop AZ4O0 1:4, (approximately 2min)
Oven Bake 200x60min (curing)
Vias opening
Lithography 4562
Wet etch HF 10% until first vias open
Dry etch to complete the process: 100sccm CF_4 + 20sccm O_2 100W, 200mTorr
Interconnect
Lithography AZ5214
Use Chlorobenzine x 10min before development
Evaporate 200A Cr/ 200A Pt/ 4000A Au
Mirror etch
Lithography AZ5214
Etch 10sccm $BC1_3$, 0.5sccm CI_2 @ 50W,50mTorr

Regarding Silicon circuits the design was done so that the GaAs device would be aligned as shown in the following figure.

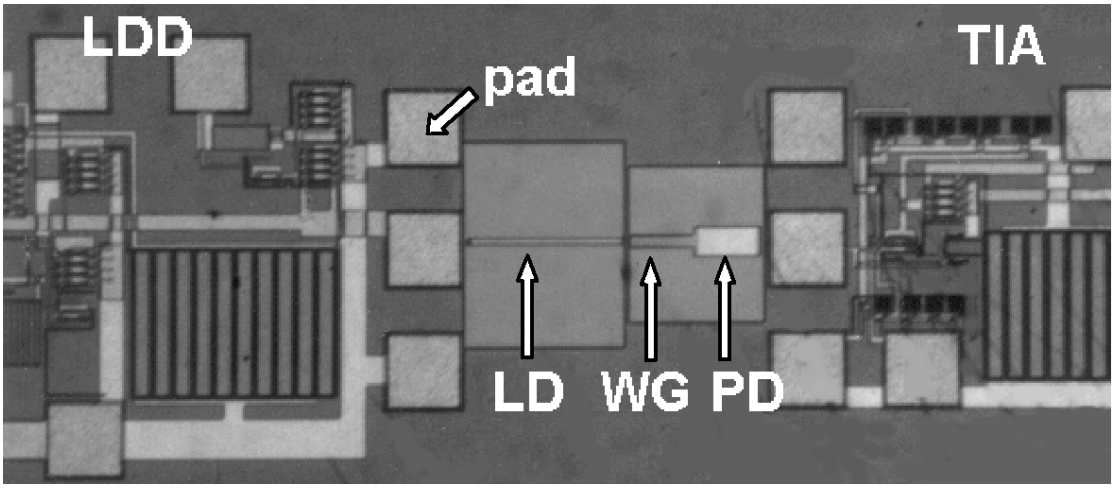

Figure 3.4: SEM picture of the GaAs devices bonded on the Silicon wafer. Extra GaAs is already removed.

Section: 3.3 .Mirrors

One of the key steps in fabricating laser diodes is fabricating the cavity mirrors that provide the electromagnetic wave feedback necessary for such a device to operate. Traditionally, mirrors are created on GaAs using cleaving. However when integration is one of the targets, the wafer can not be diced into pieces. Furthermore creating an optical interconnect using cleaved laser diodes would mean realignment of the resulting devices. It is easily understood that this has little -if any- practical meaning.

The second option is to create mirrors using some kind of micro-fabrication technique. In this work, reactive ion etching (RIE) was used. In this section, mirror

etching using RIE is presented. All experimentation and fine tuning to attain an acceptable mirror quality will be presented. Furthermore physical aspects of the RIE etching process will be presented so that a rule of thumb for future recipe development is attained.

3.3.1 .Mirror etching

During a mirror etch, one has to etch starting from the top of the device all the way through the cladding layers, the core of the waveguide and reach the bottom cladding layers. This means that both GaAs as well as AlGaAs have to be etched. [16] Since Fluorine containing gases are not able to etch Al containing material, the only available solution is to use Chlorine containing gases. But this is not the only requirement.

In order to create mirrors, dry etching needs to meet certain criteria.

- Vertical – completely anisotropic etching

  Light is propagating parallel to the surface. If one needs a mirror to reflect it back from its original course, this mirror has to be vertical. Furthermore a mirror has to be planar so that it does not change the spatial distribution of the electromagnetic radiation that gets reflected. This means that etching has to create a planar, vertical surface that will act as a mirror for the laser to operate efficiently
- Smooth morphology of the etched areas

  The difference between a mirror and a white board is scattering. The first one is smooth to a point where roughness is less than the wavelength of the radiation that gets reflected. According to the Hyugens principle in optics, a perfectly planar surface will reflect a wave front without distorting it. On the contrary roughness gives arbitrary direction to the reflected light thus distorting the wave front and sending the light towards all directions.
- Minimum damage in the etched surface

  Surface damage of a semiconductor material gives extra states which are responsible for surface conduction. In a semiconductor laser, surface conduction gives a path for carriers to recombine non radiatively. This means that close to the surface of the mirror, the radiative efficiency drops. This is to be avoided for two reasons, small radiative recombination means less gain, therefore increased absorption which leads to increased temperature and secondly, bad radiative efficiency leads to higher operating currents for a given output power.

The above should be convincing that what one needs to create etched mirrors, is a completely anisotropic process that is not aggressive enough to create extended damage. Sputtering for example (which is purely mechanical) creates damage to the etched surface and this is obviously a problem for our case. Careful tuning of mechanical and chemical etching components of the dry etching can provide smooth, vertical walls with minimum structural damage.

BCl_3 is a gas that is widely used in semiconductor processing. Once dissociated in an RF – plasma environment it produces atomic Chlorine and Boron. The first one is chemically active whereas the later is relatively inert but acts as an ion milling component. Experiments performed with BCl_3 alone at low pressures, provided vertical smooth walls of the etched patterns as desired. However the etch rate of the process was extremely slow since photoresist (the masking material) was strongly sputtered. This leads to formation of a protective thin layer over the surface of the sample that has to be mechanically removed before etching can take place.

In order to increase etch rate, Cl_2 was added to the gas discharge. Theoretically one expects to provide more atomic chlorine this way that will increase etch rate. At the same time, photoresist sputtering should protect the side walls of the etched surface that is not bombarded by the kinetic ions. Several experiments where performed for varying Cl_2 percentage and different etching conditions. Once the chlorine percentage was high, rough isotropic surfaces appeared giving indications of strong chemical etching that was not desirable. Etch rates were higher with Cl_2 percentage which is according to our analysis. Finally a 5% Chlorine gave acceptable etch rate while the etch profile remained practically intact.

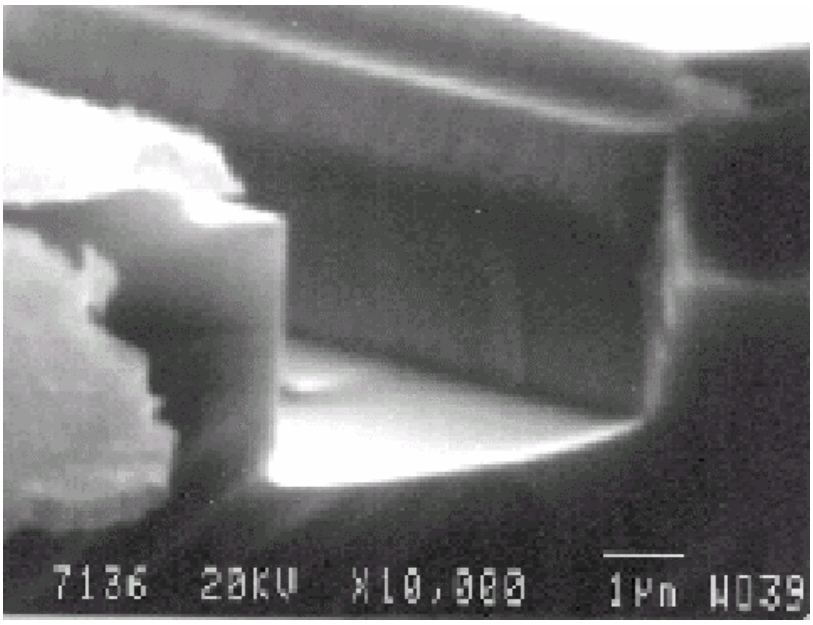

Figure 3.5SEM picture of etched mirror vertical smooth wall is seen. The detail is from a laser device (right) facing a photodiode (left)

3.3.2 .Evaluating mirror quality

The best mirror quality one can obtain, is to have an atomically flat, vertical mirror. In other words if one could cut the crystal along a crystal plane, without deviations the best mirror would result. In fact this is how most of the semiconductor lasers are created. [1] Cleaving is a process during which you stress the crystal mechanically to the point where it breaks. Since the bonds in the crystal break, the minimum energy

orientation is preferable. GaAs (100) cleaves at the {011} and {110} planes and engineers have taken advantage of this to create atomically smooth mirrors.

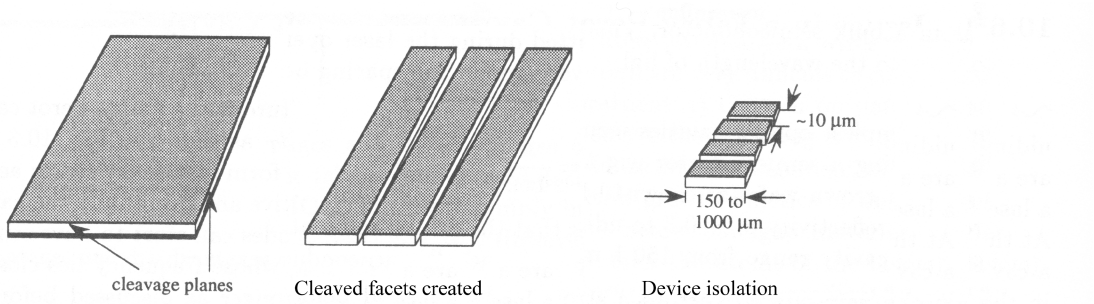

Figure 3.6: Cleaving process schematically illustrated

In order to evaluate the mirror quality created by any other technique (including dry etching) the standard should be cleaved mirror performance. That is true as long as no reflective coating are added to increase the reflectivity of the mirror.

In this work, cleaved mirror samples were prepared in parallel to the etched mirror devices. Comparison of the threshold current density needed for a device to lase, taking into account device length can give a good approximation of the mirror reflectivity. This method was used and the results will be discussed in chapter 5.

Chapter: 4 .Processing of GaAs bonded on Silicon

Section: 4.1 .Thinning of bonded material

One of the basic processes that were developed was backside thinning of the GaAs bonded material. As explained already, the GaAs substrates that were used to grow the active layer structures, are bonded facing down on the Silicon wafers. When the bonding is completed, the GaAs wafer is no longer needed and has to be removed. This is described as backside thinning. [17][18] It is important to realise that although the necessary structure is only a few microns thick, the GaAs wafers are typicaly 400μm. The thickness is such that the wafers can normally be handled without risk of breaking them (GaAs is actually a fragile material). In the following paragraphs, the thinning process is described in detail.

Several GaAs wafers were grown, some with structure necessary to fabricate LD and optoelectronic circuits and some with structures used for testing. The GaAs wafers were bonded either on plain Silicon wafers or fully processed CMOS wafers

The following table is a summary of structures bonded and thinned.

GaAs Wafer ID	*Structure*	*Silicon wafer / CMOS*
125	Laser Diode Structure	CMOS
126	Laser Diode Structure	CMOS
127	Laser Diode Structure	Plain Silicon
130	Laser Diode Structure	Plain Silicon
131	Optical characterization Str.	Plain Silicon
133	MESFET structure	Plain Silicon
163	MESFET structure	Plain Silicon
162	Test GaAs structure	Plain Silicon

Table 4.1: Bonded wafers processed at MRG-IESL-FORTH

The reason to bond different kind of structures is simple. Besides proper evaluation of laser processing on bonded material, the effects of structure complexity vs bonding quality have to be investigated. Furthermore, it is necessary to evaluate the bonded material to see if the bonding process introduces electrical or mechanical defects.

4.1.1 .Backside thinning technology

In order to develop a successful wafer thinning process, two different approaches were investigated. Each one will be described and evaluation of the results obtained will be presented.

A) Process starting by CMP[i] thinning

CMP was performed by MPI, Halle. The purpose was to remove 90% of the total thickness of the GaAs wafer. In this case, the GaAs material was thinned to approximately 40μm using this technique. The uniformity of this process is rather good. It is possible to etch 300 microns of material in the entire 3" GaAs wafer with a 10-20%

i Chemical mechanical polishing

variations of final thickness. CMP is based on a combined action of chemical etching and grinding of the surface. The fact that grinding is heavier for areas that are protruding, creates a self compensating action of the nonuniform etch rate across the wafer. Some of the parameters that one can tune in CMP, is applied pressure of the grinder to the semiconductor surface as well as rotation/translation speed of the wafer. As one may understand this process is stressing the substrate mechanically and this may pose problems for thin substrates. In some cases large areas of the GaAs wafer could be de-bonded by the process as shown in fig.4.1

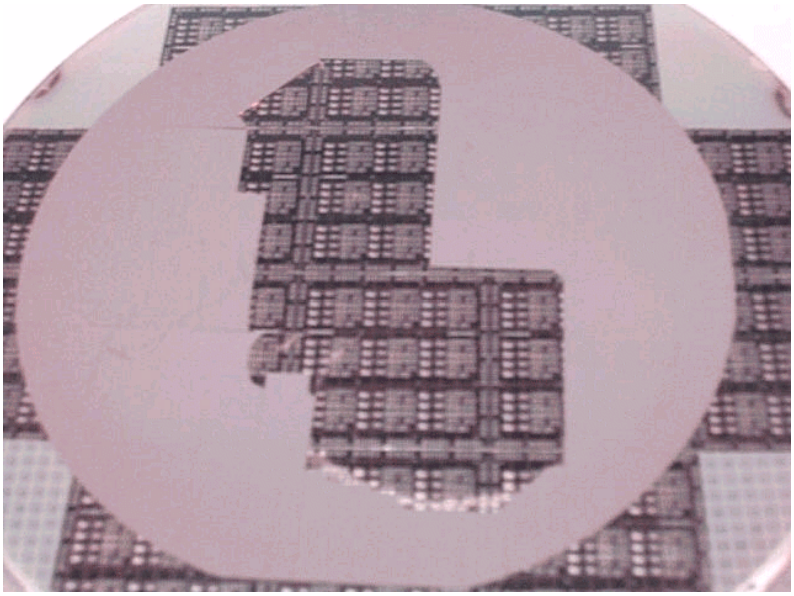

Figure 4.1: CMOS wafer after CMP etching and annealing at 350C. Central area was not properly bonded and broke off.

Since the substrate is likely to break if one tries to thin it down more and since the non uniformity that is associated to the CMP process could cause some parts of the substrate to be removed completely while others still have unwanted material left, there is a need for a more subtle technique to complete the GaAs wafer removal.

Luckily, it is possible to obtain a selective etch process. By selective one means that although the etch rate of one material (i.e. GaAs) is fast, the etch rate of a different material (i.e. $Al_xGa_{1-x}As$) is very low. This alows for a "trick". If during growth of the structure a thin layer of $Al_xGa_{1-x}As$ is incorporated directly below the wanted structure, and since we need to remove the GaAs wafer, we can use that layer to stop exactly at that point. This is easily accomplished with GaAs/AlAs materials. When we etch the GaAs substrate, as soon as the AlAs layer is exposed, the etch rate at that location drops. Evidently that area is left intact allowing at the same time for other areas to etch down to the "etch-stop" layer.

There are two categories of selective etching available. The first one is to use aqueous solution to etch the desired material. If the etching solution is carefully fabricated, it can attack only one kind of material and leave a different material intact.

This has to do with the chemical behavior of each semiconductor that differs slightly from other materials. An example that has been utilized in the past is Citric acid / Hydrogen peroxide solution. If the PH of the solution is carefully tuned, then this solution will attack GaAs but not AlGaAs with Al mole fraction more than 0.2. [19] The selectivity of this solution can be quite high (as much as 1:1500). The problem with this solution is that if the PH is not tuned correctly or the etching modifies the solutions concentrations, the selectivity drops rapidly. This is obviously a problem when one tries to etch large surfaces of material in a simple experimental set-up as in our case.

The second option is to use dry etching in a plasma. Although the equipment necessary for such a process is expensive and the process itself is time consuming, the results can be superior to the wet etchant. The gases that are used to obtain selectivity are Fluorine containing. Fluorine when reacting with Al it forms a non volatile product that operates as a micro-mask on the surface of the etched substrate. This inhibit etching selectively for layers that contain Al with mole fraction more than 0.5. This is the process that was used to complete the thinning of GaAs substrates.

The RIE process was performed at:

- 75mTorr chamber-pressure
- 7sccm CCl_2F_2 flow and
- 70Wattt of RF power.

Selectivity of AlAs etch-stop layer over GaAs material is more than 1:1000, thus allowing a non-critical thinning process. GaAs material was removed at an average etch rate of about 1μm/min. End point monitoring was performed by reflectivity measurement of the GaAs surface. [16]

This way the entire GaAs material is removed and a relatively smooth surface of AlAs material is exposed. Below that is the layers that will later be processed into III-V optoelectronic devices.

In order to expose the active layers, the etch stop AlAs layer has to be removed. This is accomplished by a selective wet etching that will attack only AlAs material. An aqueous solution of Hydrofluoric acid (HF) 10% is etching AlAs at very high rates while it does not attack GaAs or AlGaAs with mole fraction below 0.5. This way, a short, wet etching step in HF is enough to remove the AlAs etch stop layer. This has two advantages: First of all, it is certain that the active layers will not be affected by the solution since they do not contain high Al concentration layers. Secondly, the fact that this step is selective as well, will remove any roughness remaining from the dry etch process. This is good since the surface quality (i.e. roughness) of the remaining material is comparable to the surface quality of epitaxially grown III-V layers.

After this step what is left is a 5-10μm thick III-V heterostructure bonded on the surface of a Si wafer that may or may not have Silicon circuits. This is the material that will finally be used to fabricate the proof of concept of the entire project, namely Optoelectonic circuits.

B) Process starting by wet etch thinning

Some of the bonded GaAs wafers were not thinned using CMP. This was done in order to compare and evaluate the damage induced by this process. These wafers were delivered at full thickness (500μm) and were thinned using a fast wet etching process (H_3PO_4,H_2O_2,H_2O) to an average thickness of 80μm. Using wet etching, mechanical stress of the material was avoided.

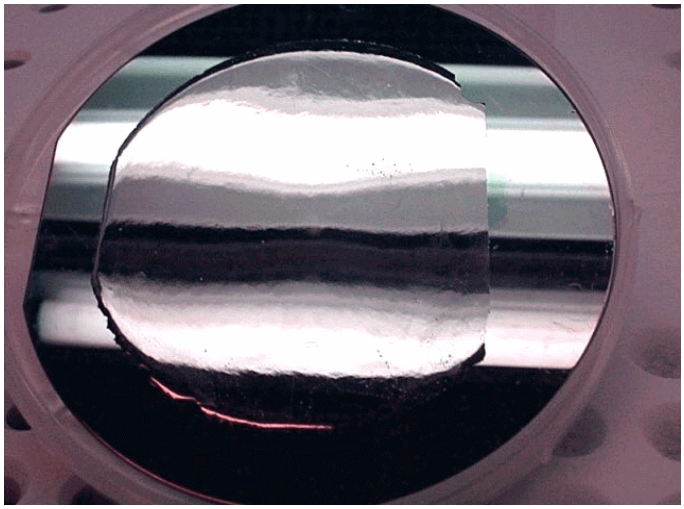

Figure 4.2: Test wafer after wet etching, before final thinning by RIE. No cracks appear. The side that broke off revealed SOG material that was not in touch with GaAs wafer

Unlike CMP, wet etching introduces no additional damage to the GaAs material. This is true since no mechanical contact to the substrate is done. The material is removed via a chemical reaction between the solution and the semiconductor material. For this reason, however, an issue of uniformity could rise. Even the slightest difference in etch rate between two locations can build up a difference in etched material thickness. Since the goal is to etch most of the substrate (i.e. 400μm) it is important to have uniform etch rate. This is why special caution was taken and agitation of the etching solution was performed using magnetic steering. This ensures that the solution is not depleted from active spieces on top of the etched surface. Furthermore, fresh solution coming is effectively increasing the etch rate. The thickness of the substrate was measured every few minutes and the corresponding etch rate was in the order of 20μm/min. Once the thickness was less than 80μm, the etch process was stopped to avoid over etching in some areas of the wafer.

Following that step the rest of the process (selective dry etching and HF) were the same as for CMP thinned samples.

From optical inspection of the samples, it was evident that samples thinned with the second method had less cracks. In essence, it appears that CMP is introducing some defects to the fragile GaAs layers.

4.1.2 .Evaluation of the thinning results

A parameter for evaluation of the thinning process is damage induced in terms of cracking, yield of bonded material and surface characteristics of the remaining active material.

In order to estimate the surface quality of the thinned material, AFM measurements were performed. Roughness was found to be similar to that of as-grown wafers, thus indicating that thinning produces no significant surface degradation of the material's quality.

An additional issue was electrical properties of the resulting surface. In order to evaluate potential damage, MESFET transistor Schottky and ohmic contacts were fabricated and measured, exhibiting similar characteristics to that of MESFET devices fabricated on GaAs wafers (See task 2.3). It is therefore clear that material bonded and thinned exhibits no significant degradation when compared to grown GaAs wafers.

An important issue is yield, in terms of material remaining as well as cracking that renders areas of material useless.

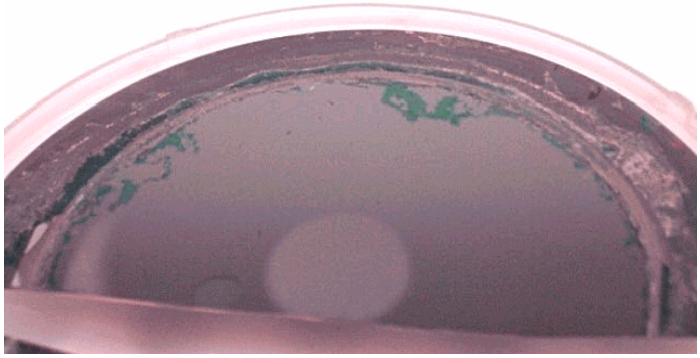

Figure 4.3: Part of MESFET structure after RIE thinning. Crack free material and almost 100% yield. The dark spot in the middle of the wafer is GaAs that was removed by complementary RIE process

Although the potential of SOG low temperature bonding appears promising since entire wafers of GaAs material have survived the thinning process, being completely crack-free and no areas of the GaAs material peeled off, this did not hold true for all the processed wafers.

Few wafers exhibited inadequate bonding quality that resulted in low material yield. The most common situation encountered was large areas of GaAs material that were not bonded adequately to underlying Silicon material and would peel off, as soon as the thickness of the GaAs wafer was not enough to keep them in place. Although these areas were not visible before thinning (using infrared transmission photographs), SOG that was uncovered exhibited wavy patterns that lead to the assumption that bonding in those areas was not achieved. On the contrary, areas with good quality bonding would exhibit a smooth uniform SOG area if GaAs material were removed.

Section: 4.2 .Special processing considerations

4.2.1 .Structure related issues

Comparing different growth structures there has been a significant difference in bonding quality between wafers with Laser structure and samples containing less AlGaAs layers. Namely, MESFET structures and test structures having a small percentage of AlGaAs over GaAs thickness would exhibit better bonding quality and higher material yield through the thinning process. The best result consist of a practically 100% yield, with complete absence of GaAs cracks which was achieved for a MESFET structure (epitaxial film of about 2μm thickness with only 5 AlGaAs layers) On the contrary, some Laser structures, would exhibit low bonding yield and large cracking density.

This could be partially attributed to internal stresses created by the lattice mismatch between GaAs and AlGaAs material. This holds especially true for a Laser diode structure in which $Al_xGa_{1-x}As$ layers are thick compared to the total thickness of the GaAs film and Al mole fraction (x) was as much as 45%.

4.2.2 .SOG thermal processing issues

Another important parameter of the bonding and thinning process is the 350C annealing step of the bonded GaAs/SOG/Si material. Although better bonding strength and therefore better yield was expected for samples that were bonded and annealed after CMP thinning to 40μm, before the final thinning process, it was found that non annealed samples, would exhibit better behavior during the wet/dry etching thinning process.

Bonding strength was not an issue as long as there are no voids between GaAs and Si and good low temperature (<150C) bonding is achieved. During processing, annealing of GaAs contacts can complete the imidization process of SOG giving much easier escape route to gases that are released around GaAs devices and not through the edges of the wafer. [4]

The best results, as far as the thinning process was concerned, were obtained for a sample that was soft annealed before thinning and then processed into GaAs devices.

4.2.3 .SOG thickness

SOG films that reached MRG/FORTH varied in thickness. For CMOS wafers, total thicknesses measured after processing were in the order of 5μm (including CMOS processing SiO_2). For structures bonded on plain silicon, the SOG film thickness was in the order of 1um. There is not enough evidence to support a conclusion about bonding quality vs. SOG thickness. However, it is certain that a thick SOG film is not desirable, considering the cooling efficiency of Laser devices.

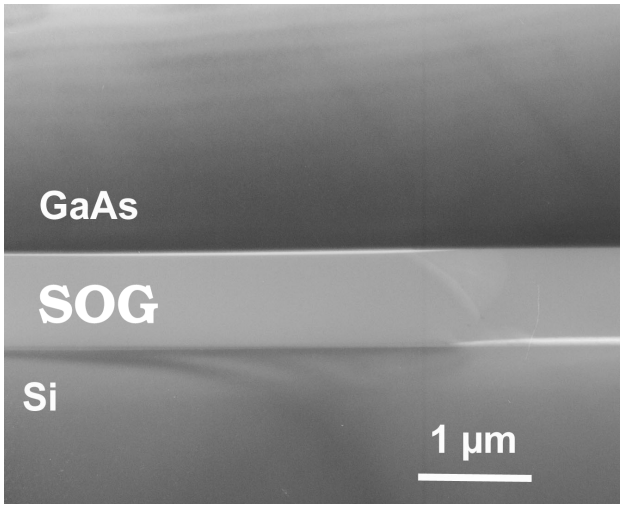

Figure 4.4: TEM cross section image of the bonding interface

4.2.4 .Conclusions on thinning

Backside thinning of the GaAs bonded wafers was successfully developed in this project at MRG/FORTH, thus showing that SOG low temperature bonding is a viable solution for wafer scale integration of GaAs and Silicon circuitry

Even though planarity problems on CMOS processed silicon wafers were evident, SOG L.T. bonding was able to provide adequately bonded material for the investigation of O/I's on GaAs.

Almost 100% yield was obtained for MESFET structures bonded on plain Silicon wafers, providing crack free, excellent quality, thin film GaAs material.

Section: 4.3 .Silicon - GaAs interconnection

Another important step that needs to be completed in bonded substrates is the electrical interconnection of GaAs based devices with circuits implemented on Si. In between the two materials, lies a film of SOG that has to be etched away in order to deposit metal that will come in contact with the Si circuits.

In order to make the alignment of the devices easy and non critical it was chosen to create big pads (150x150μm) on the Si chips. This would also facilitate device probing without problems so that Si circuits can be checked. The SOG film is etched either using wet etching (HF 10%) or dry etching (CF_4/O_2). The window that is opened is 2μm smaller than the Al pad existing on the Si circuit. This will ensure that no damage is done to the circuit by etching and that no short circuit is possible. Finally a thick metal is deposited (Au 500nm) starting from this pad to the pad created on the GaAs device.

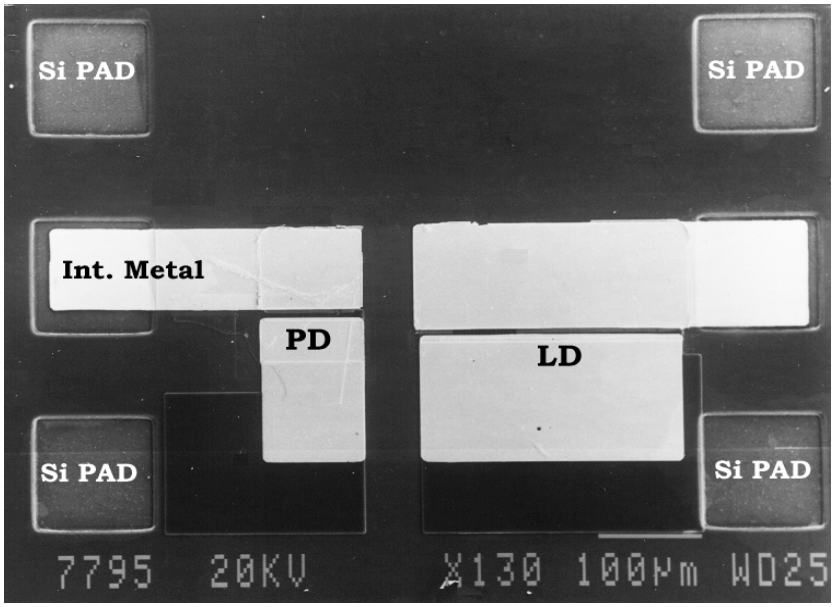

Figure 4.5: Top view of an interconnected OEIC, the Si pads are visible under the SOG layer (black area). SEM imaging cannot penetrate insulating materials.

Section: 4.4 .Thermal stability of the bonded wafer

In order to evaluate the thermal stability and the stress existing on the structure that was bonded on Silicon wafers, photoreflectance measurements were performed on the material for varying temperatures. Photoreflectance can provide an estimate of the residual stress in a semiconductor material. [20] The result is summarized in the following figure.

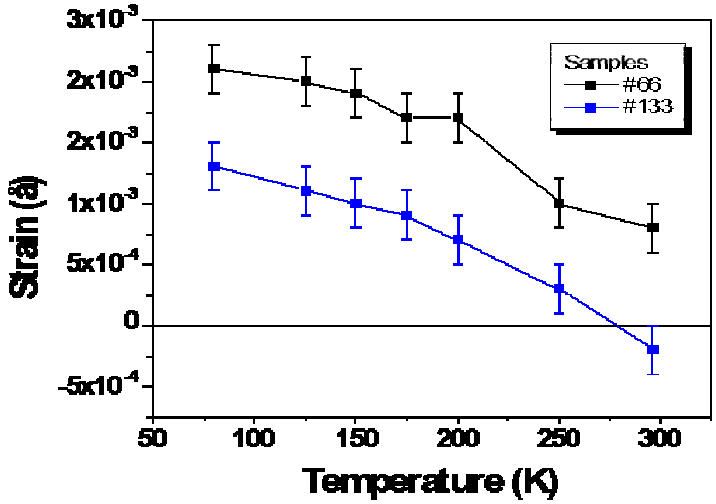

Figure 4.6: Biaxial strainin the GaAs/Si layer vs Temperature. An epitaxially grown GaAs on Si (#66) is used for comparison with the GaAs/SOG/Si sample (#133)

Finally it is important to find out whether there is plastic deformation resulting from the thermal cycling of such a bonded material. The following figure gives the reflectance spectra in room temperature after cycling down to 75K and back.

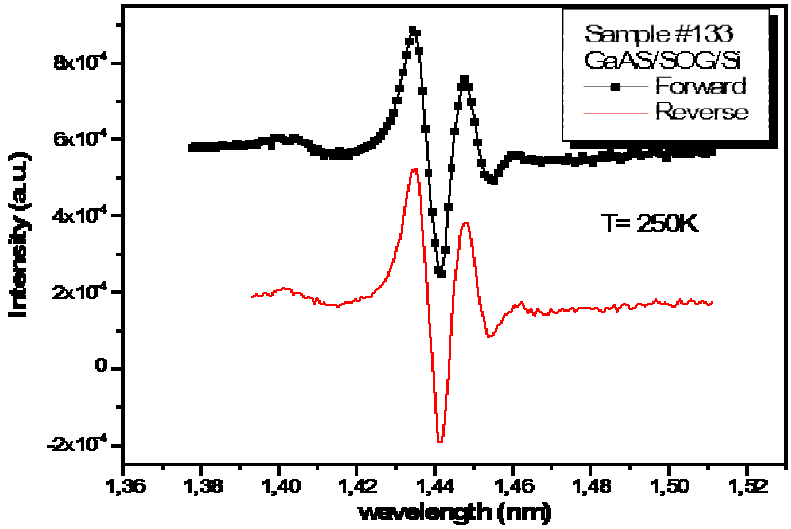

Figure 4.7Reflectance spectra after cycling. Spectra are exactly the same indicating that no plastic deformation occurs.

The same conclusion was reached by measuring the bowing of the bonded GaAs/SOG/Si wafer as the temperature was varied from room temperature to 200 °C.

Chapter: 5 .Laser performance

This chapter is dedicated to presenting measurements of electrical and optical characteristics of the fabricated laser diodes. The first section, entitled "Cleaved lasers" is about laser diodes fabricated with cleaved mirrors. Comparison to the theoretical model will be presented there and basic structure characteristics such as absorption coefficient and injection efficiency will be deduced from optical measurements. The second section presents etched laser performance on GaAs substrates and the third one discusses etched lasers fabricated on bonded material. Throughout this chapter, connection to theoretical models and physical effects is done wherever possible.

All lasers fabricated for this project where operated with uncoated mirrors. This means that the mirror reflectivity was approximately 30%. This also resulted in 50% of the emitted optical power to come out from the rear mirror. All results presented are for single mirror output.

Cleaved mirrors that were measured were 50μm wide. The broad area lasers were selected for practical reasons, since narrower ridges require extra steps to create a bonding pad. Finally, all measurements were performed for pulsed operation. Usually the current pulse applied to the devices was 500nsec with a repetition rate of 10KHz. This was done to avoid heating effects that strongly depend on the packaging of the laser diode. The same structure could operate in continuous wave if mounted on a heat sink but this was beyond the scope of this project.

Section: 5.1 . Parameters fine tuning

5.1.1 .Quantum well number

One of the parameters that had to be fine tuned experimentally was the number of quantum wells (QW's) inside the waveguide structure. More quantum wells means higher transparency current. This is obviously a drawback if one designs a laser diode. However there exist a number of reasons to increase the quantum well number as much as possible.

The laser device to be used should be 250μm long. This is rather short compared to typical semiconductor lasers. Given the fact that a small cavity results in higher threshold gain, one may face the situation where a single quantum well cannot provide the gain necessary to obtain laser operation. Furthermore, etched mirrors are expected to have worse reflectivity when compared to cleaved mirrors, this means that the feedback mechanism is diminished and even higher gain is necessary to overcome the increased losses. It was anyway, very interesting to acquire a set of experimental results that were not available in the literature for the effects of the quantum well number on the laser diode's performance. The most interesting reason was the fact that the same structure had to be used to create photodetectors; more quantum wells lead to higher photocurrent for those devices.

For the above reasons, a set of samples with 2, 4, 8, 16 and 32 QW structures were fabricated and processed into cleaved laser devices. Threshold current density was

measured for different device lengths in each structure so that an estimated threshold current could be obtained for the final 250μm x 10μm devices.

5.1.2 . Graded index layers

Following the theoretical discussion on waveguides it is evident that graded index cladding layers improve the optical mode distribution inside the core of the waveguide. [21] To be specific, if step index layers are used, the optical mode is not so intense at the center of the core as compared to the same structure with graded cladding layers. This translates to higher threshold for the step like structure. Besides the laser diode behavior there is another issue to be considered before introducing graded layers. The photodetector response may be altered by these layers since photogenerated carriers will face a different potential in order to escape from the core of the device and reach the biased electrodes.

In order to decide which is the best solution, structures with and without graded layers were fabricated and characterized using laser diodes and photodetectors. The part concerning laser diodes is presented here whereas the part concerning photodetectors will be discussed in the following chapter.

Section: 5.2 . Cleaved Lasers, structure reference

Besides having a reference for the mirror quality, cleaved lasers offer a repeatable way to characterize structure performance. Some parameters regarding the structure design have to be checked and using cleaved lasers is the best way to make sure that the design of the structure actually provided optimum results. First of all, the number of quantum wells that has to be incorporated in the core region of the laser as well as graded layers that improve optical performance were checked, using cleaved laser fabrication. The following sections delve into details of these decisions.

One final note is in order here. Cleaved lasers could theoretically be fabricated on GaAs on Si structures. This was not possible in our case for a very simple reason. In order to cleave both materials, the cleavage planes of GaAs and Si had to be aligned at bond time. This alignment is critical since cleaving has to produce a crystallographic fracture of both materials in order to be optically smooth. This requires that bonding is done with accuracy in the order of tenths of a degree or even less. If the wafers are misaligned (i.e. tilted, rotated), and given the fact that Si is much thicker, the cleavage planes of Si would designate the cut direction and GaAs would break in a rough surface unable to reflect light properly.

5.2.1 . Quantum well numbers

Cleaved lasers were prepared for different quantum well numbers. For each structure, a number of lengths was measured. The results are shown here. Measurements were performed in pulsed conditions using a calibrated optical power meter with a large area photodetector coupled directly to the mirror of the device. This way, almost all of

the light emitted from the mirror is measured.

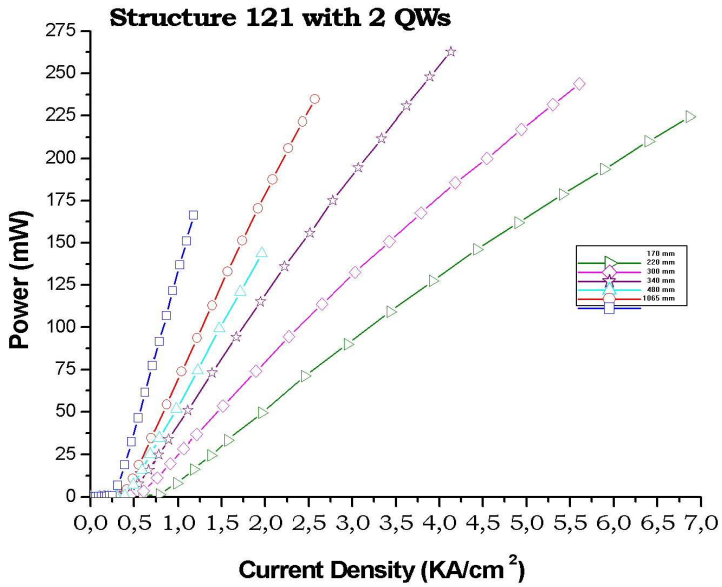

Figure 5.1: 2QW structure, Power vs J diagram

For structure 121 with 2 Qws (Fig. 5.1) one can see a threshold current density that is in the order of 0.5KA/cm^2.

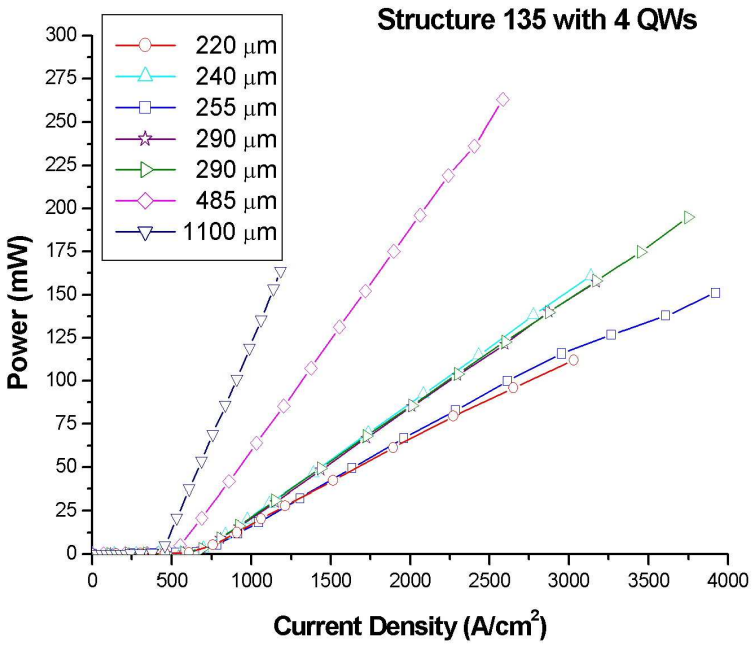

Figure 5.2: 4QW's structure, Power vs J diagram

Respectively for structure 135 with 4 Qws, (Fig. 5.2) the threshold current is somewhat more compared to the 2QW case ranging from 0.5 to 0.7KA/cm^2

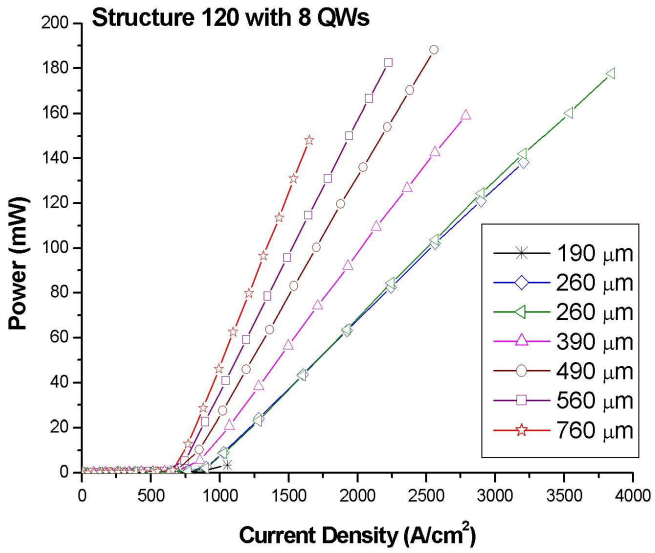

Figure 5.3: 8 QW's strucutre emitted power vs J diagram

For structure 120, containing 8 Qws, (Fig.5.3) the threshold current density is increasing at a level between 0.7 to 1 KA/cm^2.

Finally, one can observe a sudden increase in threshold current density for structure 122 with 16 QWs (Fig.5.4) know ranging from 1.2 to 1.4 KA/cm^2

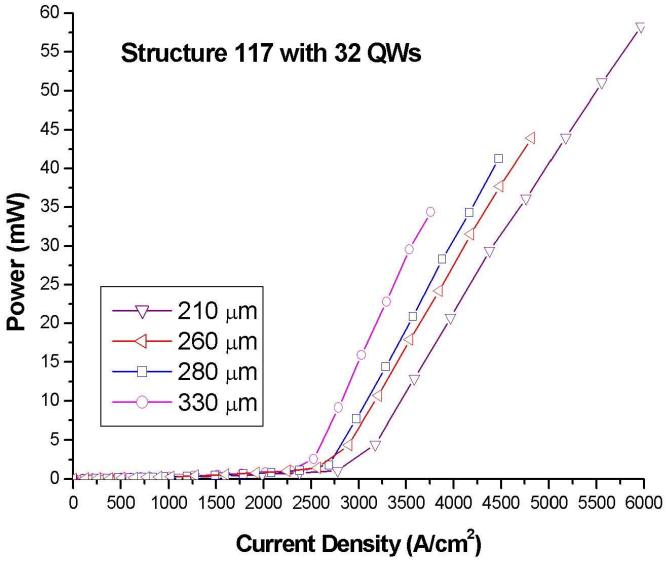

Figure 5.5: 32 QW's emitted power vs J diagram

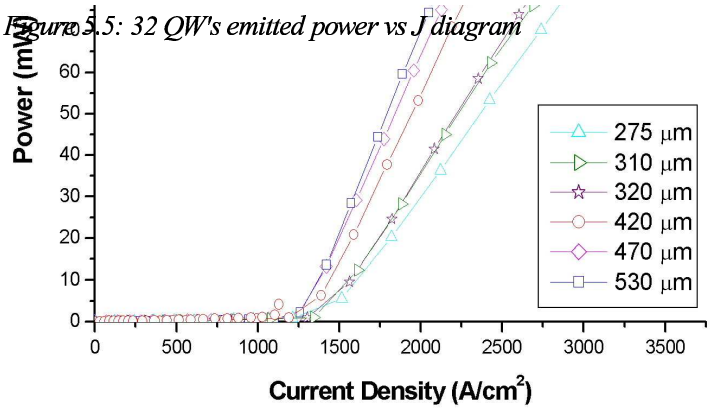

Figure 5.4: 16 QW's strucutre emitted power vs J diagram

As expected, the 32 QW structure (Fig. 5.5) exhibits a threshold current density in the range of 2.5KA/cm^2.

In order to set an upper limit to the number of quantum wells we should take into account that the final devices should operate using a maximum dc current of 40mA, with 40mA modulation current capability (Si circuits). The maximum dc current corresponds to 1.6KA/cm^2. This decision should take into account that etched lasers will definitely have worse performance because the mirrors will be worse compared to the cleaved devices. Allowing a safety factor of 2 in the threshold current needed one should select the device with less than 0.8KA/cm^2 threshold current density. This is the reason for selecting 4 QW's to be used for the final structure. Although 8 QW structure is at the limit of this selection criterion, the safest selection was used.

5.2.2 .Separate confinement vs Graded Index

Another issue that should be clarified is whether the difference between a step like waveguide and a graded index one provides significant difference in threshold current operation. Graded layers are expected to help carrier extraction in photodetectors made from the same material but the following figure is conclusive in favor of graded index layers. The difference in threshold is 50% which is rather important. Furthermore increased efficiency is obvious from the different slope of the Power vs current curve.

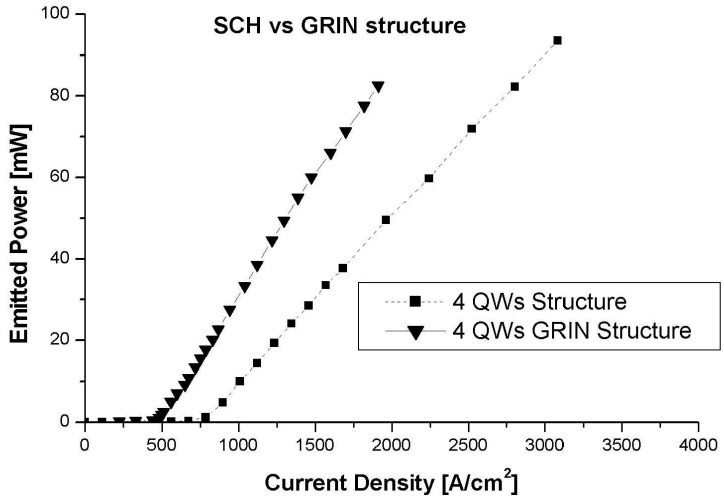

Figure 5.6: Difference between the performance of laser diodes fabricated by a simple separate confinement and a graded index structure. (GRIN)

5.2.3 .Parameters specified using cleaved lasers

Just to summarize, from the cleaved laser measurements it was decided that 4QW, GRIN structures should be used for the final interconnect devices. It was expected that etched lasers would have better than twice the threshold current density compared to cleaved devices. Compared to threshold densities for cleaved lasers in the literature, the performance of these devices is not considered good. The reason is that optimization is not done for the lasers alone but the fact that the same structure should operate as a photodetector as well, is taken into account.

Section: 5.3 . Etched Lasers, process reference

The next step was to fabricate etched device from the chosen structure. The idea is to fabricate such devices on bonded material but this section refers to devices fabricated on GaAs wafers. The idea is to isolate any problems coming from the etched mirrors and at the same time obtain a comparison device to investigate problems that could rise due to the complex substrate in the final implementation.

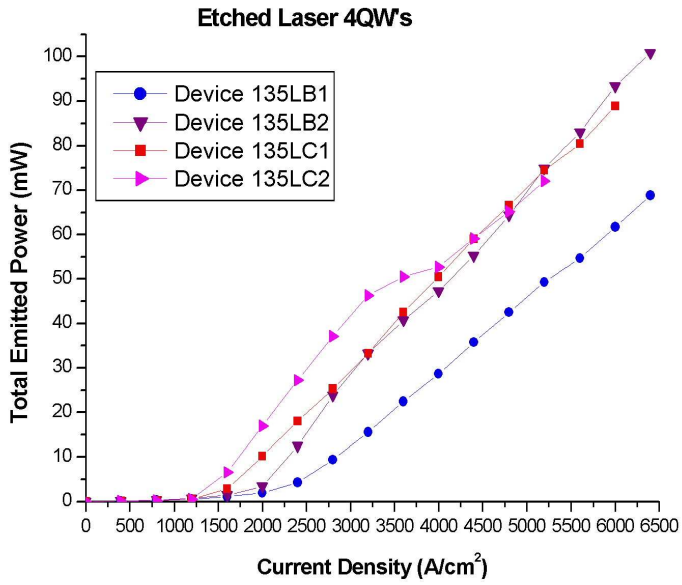

Figure 5.7:Etched mirrors device performance

As can be seen from fig. 5.7 the threshold current densities obtained from etched mirror devices are ranging from 1.4KA/cm^2 to 2 KA/cm^2. Thus, our selection to use 4 QW's is justified. If 8 QW's were used, the threshold current density would definitely be higher.

Comparing etched lasers to cleaved ones is useful to extract some conclusions.

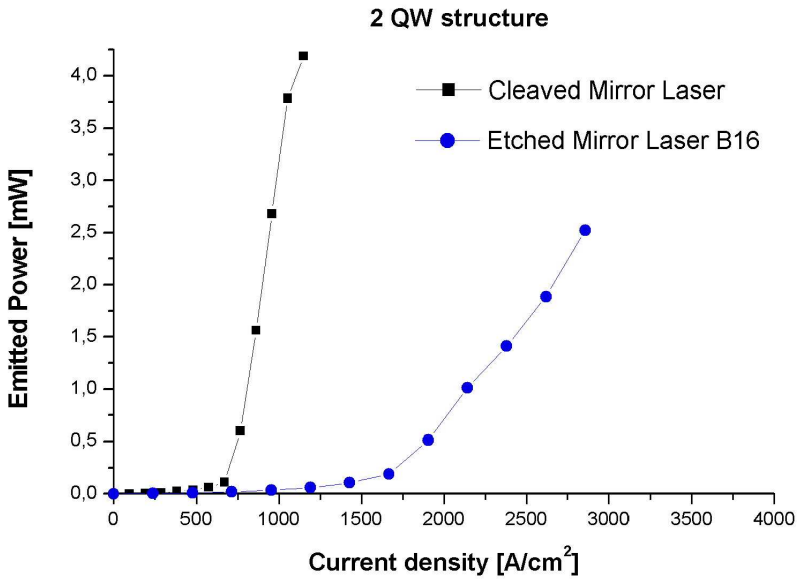

Figure 5.8: 2 QW's structure, comparison of cleaved and etched devices.

As one can see from fig. 5.8, in the 2 QW structure the threshold current for etched

devices is more than 2 times higher. The slope (efficiency) is also smaller as expected.

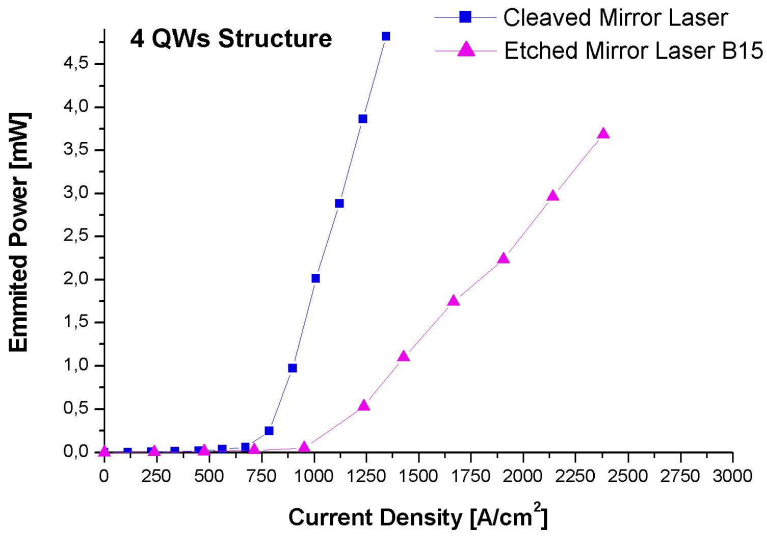

Figure 5.9: 4 QW structure. Comparison of cleaved and etched laser diode.

Fig. 5.9 shows one of the best results obtained from the etched lasers fabricated on 4 QW's structure. The threshold density for the etched device is only 1.5 times the one for the corresponding cleaved device. Assuming that the gain is linear with injected current, an estimation of the etched mirror reflectivity can be obtained.

The reflectivity calculated this way is approximately 17% half that of a perfect mirror.

Section: 5.4 . Final devices (GaAs bonded on silicon)

The final step is to fabricate devices on bonded material and compare them to the etched lasers fabricated on GaAs substrate. The extra difficulty coming from the complicated process may result in devices that operate poorly.

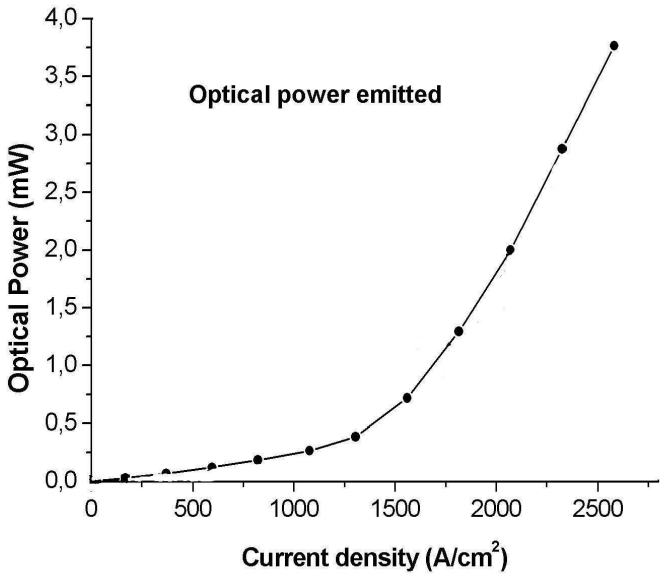

Figure 5.10: Etched Laser fabricated on Bonded substrate

As seen in fig.5.10, the threshold current density is comparable to that of device fabricated on GaAs wafers. This is an indication that fabrication process can be successfully applied to GaAs on Si bonded material.

Section: 5.5 .Conclusions on Laser diodes

Step by step fabrication of laser diodes has successfully addressed the issues that were important to achieve operating laser diodes on the bonded material. Lasers that can operate with current less than 40mA have been demonstrated and the reasoning for the choice of material parameters was presented. The next step is to look into photodetectors and waveguides in order to have a general idea of the interconnect.

Chapter: 6 .Photodiode performance

Through the following sections, a full characterization of photodiodes will be presented. Several types of photodiode devices were fabricated and measured (Edge illuminated, top illuminated). These device data helped us to determine the extend of possible photodetector specifications that can be achieved on a laser diode structure. It was chosen to split this chapter based not on the fabrication method but rather on optical signal response and wavelength dependent response, so that theoretical concepts may be discussed in depth.

Section: 6.1 . Photocurrent

As already discussed in the theoretical analysis of a photodiode, there is a direct relation between the current flowing through the pin structure at reverse bias, with the light intensity impinging on the device.

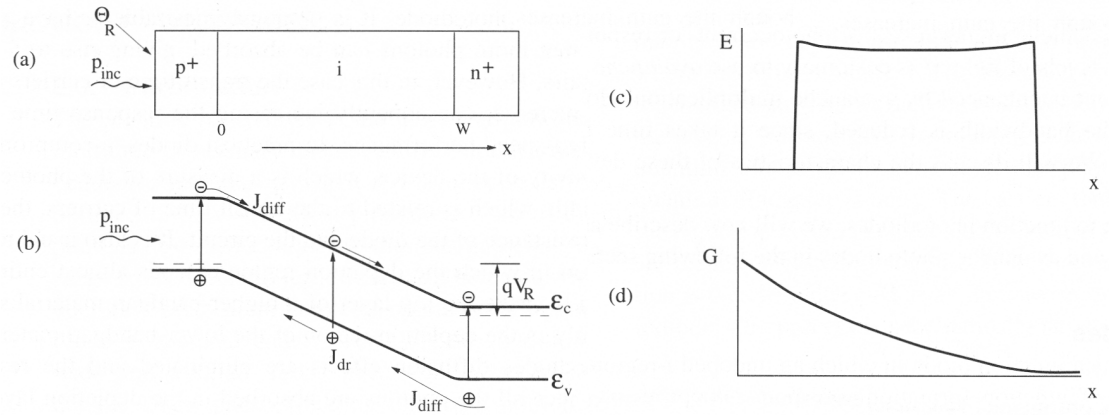

Figure 6.1: Structure of a pin photodiode (a), respective band diagram (b), electric field across the structure (c) and carrier generation rate for top illumination (d) Reprinted from [3]

Compared to typical photodiodes, our structure has a number of differences that could result in drastic differences of response. First of all, light is not coming from top as usual but it is coming from the edge of the diode. This device actually works much like a waveguide with non negligible absorption. Furthermore, the absorbing layer is not bulk material but the quantum well system that is incorporated in the structure. The cladding layers made by AlGaAs material have a much higher band gap and therefore do not absorb light at all. This means that photogenerated carriers are created only inside the quantum wells and have to escape the potential well to reach the respective electrodes.

Non-guided photodiode devices were initially characterized using top illumination. A white light source was used. The white beam was passed through a monochromator and the output was focused on the photodiode under test. The photocurrent current was measured using a lock-in amplifier and variable reverse bias voltage. There are two important issues to be considered. First is the reverse bias necessary to obtain a sufficient photocurrent. This is both in terms of carrier extraction efficiency, as well as Stark shift [22] in the quantum wells that enhances the absorption.

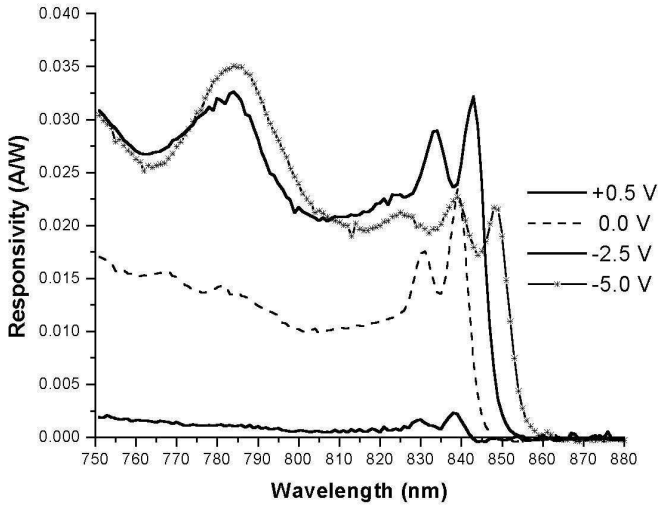

Figure 6.2: Responsivity vs λ for different reverse bias. Observe the absorption edge shift due to quantum confined stark effect.

From fig.6.2 the following can be deduced: First of all, carrier extraction from the quantum wells is accomplished at small reverse bias. This is obvious since the responsivity is high even for zero bias. Furthermore, the edge of the absorption red shifts with reverse bias. This is attributed to the quantum confined stark effect. As the quantum well states are perturbed by the electric field within the junction, the electron-hole state energy distance reduces.

The reverse break down voltage was measured and found to be -25Volts for all devices. It appears that this breakdown is not coming from the material but rather from surface effects. This means that if the photodiode is operated at -5Volts (which is compatible with CMOS voltage levels) it can function without any carrier multiplication (avalanche effect) this is necessary to obtain linear response with the impinging optical power.

It is also expected that the responsivity of an edge illuminated photodiode will be quite different from that of a top illuminated one. The reason is simple to understand. When top illumination is used, light interacts with the QW's only as it passes perpendicular to them. This means that only a small amount of light will be absorbed therefore only a small amount of carriers can be created. (This is actually referred to as external quantum efficiency) On the contrary, when edge illumination is used, light is waveguided. It therefore interacts with the quantum wells along the whole device length. Making a large device will provide more photocurrent. Taking into account the fact that the photodiodes were designed to be 150μm long, a significant percentage of light will be absorbed.

As one can see in fig. 6.3, the edge of the absorption is more gradual compared to fig

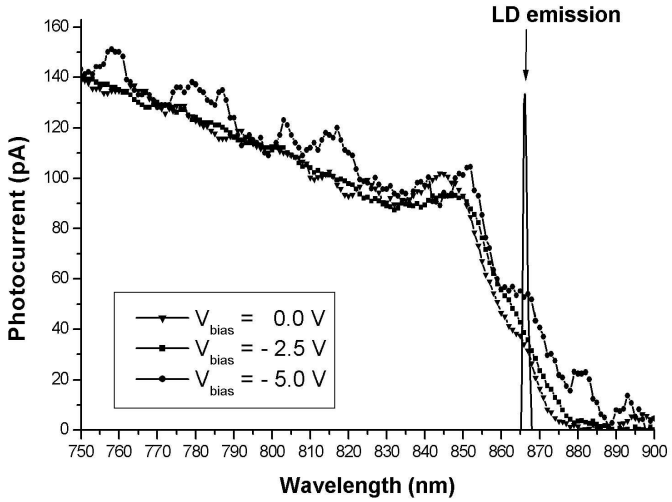

Figure 6.3: Edge illumination photocurrent vs λ

6.2. This is explained by the fact that the long interaction distance absorbs more light especially when the absorption coefficient is low (as is at the edge of the absorption spectra). Another thing to note is the fact that responsivity is not calculated for this case. The reason is that there is no way to calculate the optical power coupled into the photodiode. The edge of the photodiode's waveguide is a thin slit, 50μm x 1μm large and it is extremely difficult to focus into this area. Therefore some of the beam is actually wasted, impinging outside this area. This explains why the photo current measured is small, compared to the top illuminated photodiodes.

Another task is to characterize the responsivity vs quantum well number. Theoretically it is expected that the photo-current, thus the responsivity, will vary linearly with the number of quantum wells. This is true according to our comparative measurements.

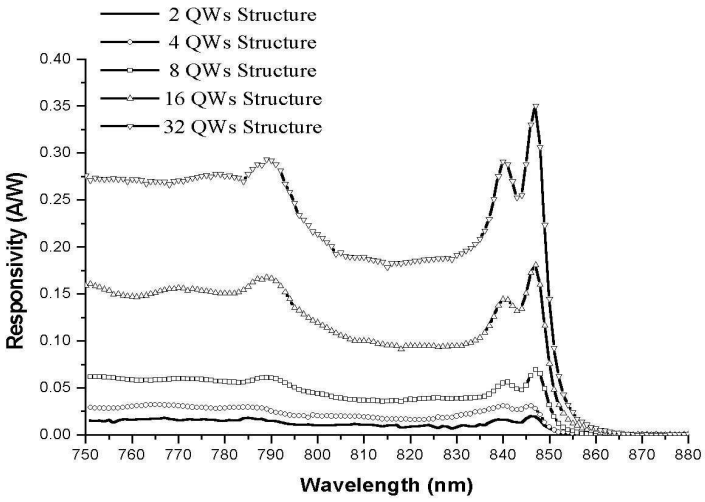

Figure 6.4: Responsivity of top illuminated photodiodes with different Quantum Well numbers. Uncoated photodiodes

Finally, it is important to find out how fast the photodiode can respond to incoming light pulses. There are two limiting factors for the photodiode's speed. First is the transit time of the carriers inside the intrinsic area, then there is the circuit analysis of the photodiode system which provides an RC constant. Both can be theoretically calculated if we take into account the capacitance of the photodiode as well as the transit time of carriers inside the intrinsic region. The I region is approximately 0.5μm taking into account the cladding layers. Since the absorption is only taking place within the quantum wells, the absorption area is actually much smaller but lets keep this conservative estimate. Given the fact that under reverse bias, carriers are traveling at saturation velocity (order of 10^5m/sec) , a simple calculation of the transit time gives a transit time in the order of a few psec.

Moreover there is a matter of RC constant of the circuit. The capacitance of the diode, times the resistance of the driving circuit should give a time constant at which the device will respond. This is the reason why we usually read photodiodes using a trans-impedance amplifier. This category of amplifiers has a small input resistance. (Typically 50Ω). If we assume that the input resistance of the amplifier is kept small, measuring the capacitance is all that is left to calculate an estimate of the response speed.

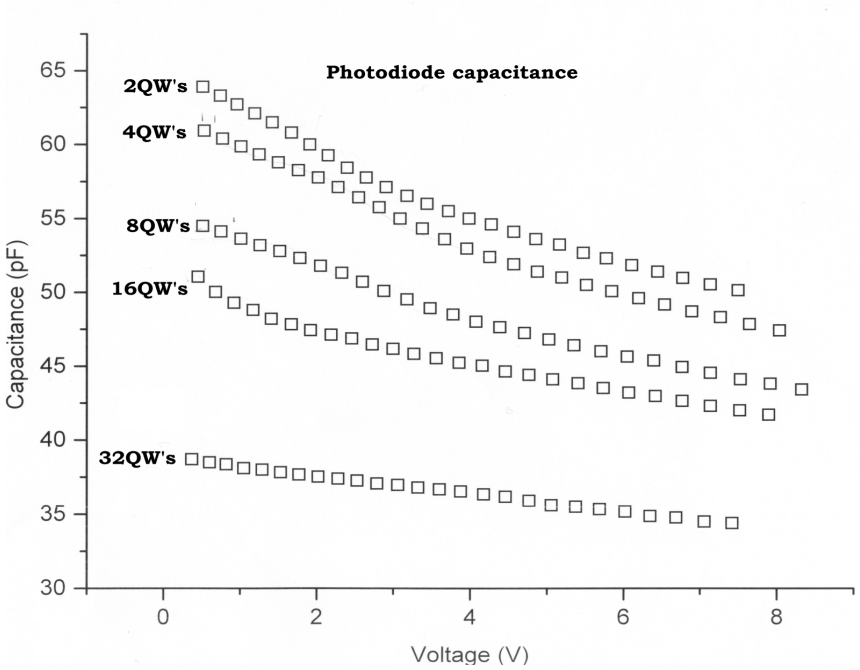

Figure 6.5: Photodiode capacitance vs Reverse bias for different QW numbers

Thus a gross estimate of the capacitance is 50pF which provides a response time of 2.5nsec. This corresponds to a modulation frequency of 400MHz. We can see that the limiting factor is not transit time but rather device capacitance. It is difficult to create a driving circuit with less input impedance. A solution could be a smaller device (which would result in less capacitance and would increase the response speed. Just to get an idea fig.6.1 corresponds to devices that are 50μm wide and 150μm long. If the width is

reduced to 10μm (as much as the laser devices) then the response would increase five-fold, exceeding GHz operation. The other approach is to increase the intrinsic layer width which will reduce the capacitance but increase the transit time. The optimum design for a photodiode is to have a transit time which is ½ that of the RC constant of the circuit.

Measuring directly the response of a photodiode is not an easy task. This was not done in the frame of this thesis. Just to take an idea you need an ultrafast pulse (a fsec laser or an optical heterodyning system, either of them emitting at the wavelength of interest.) as well as a set of very fast electronics to read the device output.

Section: 6.2 . Wavelength issues

As one can see in fig.6.3, the emission wavelength of a laser diode - fabricated from the same material - is depicted. As expected, this is at the edge of the absorption spectra. This means that in the final optical interconnect schema, the photodiode device is operating at this wavelength and with the respective responsivity. As already discussed, the emission wavelength in a laser diode is determined by the counteracting processes of band filling and band gap renormalization. (Thermal effects could play a crucial role here but we shall ignore them since laser diodes in our application are supposed to work in pulsed conditions). It is therefore not known a priori whether the emission wavelength will be above or below the band edge. It is good news to finally obtain an emission wavelength that is within the absorption edge of the material. In the final chapter, we shall evaluate the performance of the complete optical interconnect.

Chapter: 7 .Waveguides

The final yet equally important part of an integrated optical interconnect is the waveguide necessary to transfer optical signals throughout the topography of a wafer. Waveguides are by nature difficult to characterize since they are passive elements neither emitting nor detecting any kind of signal. Some ideas and potential problems will be presented but no direct measurement of the absorption in the waveguides that were created was performed.

Section: 7.1 . Light wave guiding

As discussed earlier a waveguide was introduced into the structure to create the laser diodes. The easiest way to create waveguides without adding more complexity was to create ridge waveguides out of the same material. The drawback is that the core of the waveguide contains quantum wells that absorb in the wavelength of interest. This problem is bound to limit the performance of the waveguides. There are two ways to remedy for this situation. The first is to create waveguides from a different material. The second solution is to bias the waveguides with a small forward voltage.

Making a waveguide from scratch is difficult for two reasons. To start with, more steps are necessary to deposit the materials and pattern them. Furthermore there is a design problem that has to be addressed. The semiconductor material has a refractive index which is rather large. In order to make a waveguide on top of this material, there have to be at least two materials deposited, one that will act as a cladding layer isolating the core of the waveguide from the semiconductor and then the core itself. A possible choice of materials is SiO_2 for a cladding layer (n=1.5) and then a Si_3N_4 core with an index of 2. Depositing these layers is not easy especially if thickness of a few μm is needed for each layer.

Section: 7.2 . Absorption

As already mentioned, absorption in a waveguide is coming from the interaction of light with the core and cladding layers. Cladding layers are not a problem in our case since they are made of AlGaAs material which is transparent in the emission wavelength of the laser devices. The core however has a set of quantum wells that are absorbing. The good thing is that at wavelength of interest the absorption is small, the bad thing is that it exists.

One possible approach is to avoid the waveguide at all. For small distances, one could make laser diodes emitting in free space and a photodetector at a distance, looking into the beam emitted from the LD. This is called free space optical interconnect and it is enough to provide a proof of concept for the entire project.

Another approach is to bias the waveguide with a small forward dc voltage. This will screen the built-in junction potential and blue-shift the absorption edge. Given the fact that the absorption edge tail is exponential, a small blue shift can dramatically reduce the absorption thus providing a usable waveguide. If one goes back to fig.6.2 there can be quite a drastic improvement of the absorption using this technique. Since no current

flows through the waveguide there is no power dissipation which is an important parameter to consider.

Section: 7.3 . Coupling

Finally there is an important issue concerning light coupling into and out off the waveguides.

When light impinges on a refractive index discontinuity, part of it reflects. This is how the mirrors on a semiconductor laser are created. Since the waveguide used is made of semiconductor, it is expected that it will have the same reflectivity. If 30% of the light is reflected at the input of the waveguide and another 30% is reflected at the output, what finally reaches the photodiode at the end of the waveguide is only 49% of the initial optical signal. Things get worse as coupling of the laser output into the waveguide is done through a small gap (10μm). The fact that light coming out of the laser diode is not focused on the waveguide but rather expands, makes the percentage even smaller. The same thing happens at the end of the waveguide looking at the photodiode. Finally, only ~10% of the light is expected to reach the photodiode. This is obviously a waste of signal in a real life system. The problem gets worse if one takes into account the coherence effects that can alter the behavior of the system.

A drastic improvement in this situation can be obtained if a dielectric waveguide is added to the system. The insertion losses are much smaller since the refractive index is around 2 and the angle of acceptance as well as the core thickness in such a waveguide can be made much larger. Absorption is also eliminated this way. These would result in very high signal transfer percentage thus better operation of the system.

Chapter: 8 .Evaluation and Conclusions

One has to overview what was done, whether the objectives of the project were met and to what extend, what could be done to improve performance and whether time and effort were worth spending or not. The first section of what follows is devoted to evaluating the results presented so far. Section three gives some ideas about future work and finally, conclusions are drawn taking into account a general overview of the projects accomplishments in section four.

Section: 8.1 . Optical interconnection evaluation

The final test of the entire project is to measure an operating optical link. Could devices be processed on Si? Is the laser operating? Is light coupled into the waveguide? Is the photodiode able to provide enough photo current to feed the signal into the Silicon circuitry? All these questions are addressed in the following figure.

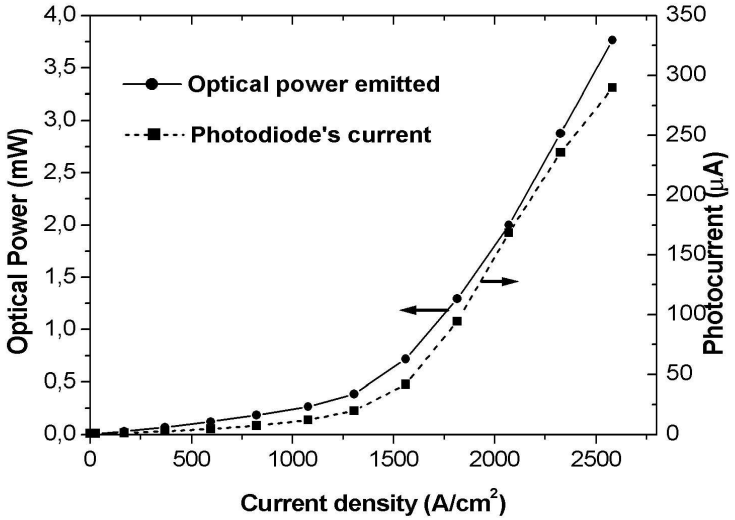

Figure 8.1: An optical interconnect at operation. Both laser emission power and the corresponding photodiode response are depicted.

As one can see, the photodiode current is directly proportional to the emitted optical power. This is a proof of concept for the optical interconnection scheme. The current from the photodiode is in the order of hundreds of μA which means that even if a lossy waveguide was between the emitting and detecting device, there would be significant photo current. The estimated responsivity of the photodiode is around 0.40 A/W

One important note concerning the goals of this project is the current necessary to make the laser diode operate. A simple calculation provides a threshold current approximately 30mA. This is close to the maximum dc current the MOSFET driver can provide.

Section: 8.2 . Future improvements

A number of improvements are suggested for further development of this innovative technology.

As far as bonding is concerned, it is important to reduce the SOG thickness. The typical thickness in this project was 1μm but much less can be obtained. This will improve many aspects of the optical interconnection, reduce cracking of the GaAs material and improve thermal stability of operating devices.

Furthermore, Vertical cavity surface emitting lasers (VCSELs) or even ring lasers could be used instead of edge emitting devices. Those devices are considered state of the art in terms of threshold current and efficiency. VCSELs are nayway the only devices that could meet the high density and low power requirements neede for Si circuit optical interconnections. Finally, bottom conductive layer could be reduced so that better cooling is achieved in laser diodes.

As far as the planar optical link is concerned, a dielectric waveguide would improve the performance of the interconnect and allow long distance communication which is the ultimate goal of this project. Another feature that could be optimized is the dimensions of the laser diode. The 10μm ridge width that was used in this study is large. Devices with ridge width around 5μm would perform much better reducing the current consumption significantly. The same apply for laser device length. Know that the reflectivity of RIE etched mirrors is well documented, the optimum could be selected to obtain a device operating at small currents and providing enough optical power.

Another possibility is to incorporate high reflective and anti-reflective coatings that can be used to improve threshold current and coupling efficiency as needed. This would allow low current density operation for laser diodes which is good for thermal stability (even cw operation could be obtained) and better external quantum efficiency for photodetectors. Of course the price one would pay is increased complexity to implement any of the above.

Finally, short cavity edge emitting laser diodes should be used to reduce the threshold current. Advanced schemes witch incorporate **photonic bandgap materials**[i] may improve the overall efficiency of the planar optical links.

Section: 8.3 . Conclusions

The idea of a Silicon MOSFET compatible process that could provide optoelectronic devices using bonding is viable. This is one of the solutions able to boost circuit performance without switching to different materials that have orders of magnitude higher production cost compared to Silicon. The fact that wafer scale integration is possible is appealing for such a hybrid technology to be adapted in real life applications were optical signals are needed.

Analog power applications could benefit from such solutions and highly integrated optical link chips could surface. As the information age is already here, more and more data need to circulate and electrical signals are not able to withstand the pressure. Optical solutions are already implemented for long haul communications, maybe light is able to provide a solution for small scale communications as well.

i PBG's are periodic refractive index structure that provide 2D or even 3D Bragg reflection of light.

This work has delved into the problems of implementing such a technology, provided a process flow and a starting point using the low temperature bonding technology. Whether this will ever be implemented I do not know. It probably depends on alternative solutions that may be proposed by researchers.

One thing is for sure:

New approaches are necessary to increase circuit density, complexity and speed of operation.

Chapter: 9 .Related Literature

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Chapter: 10 .List of publications resulting from this work – G. Deligeorgis

Publications in Journals

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3. *Molecular beam epitaxy of GaAs/AlGaAs epitaxial structures for integrated optoelectronic devices on Si using GaAs-Si wafer bonding"*, Z. Hatzopoulos, D. Cengher, [redacted], M. Androulidaki, E. Aperathitis, G. Halkias and A. Georgakilas, J. Crystal Growth 227-228, pp. 193-196 (2001).
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5. *"Fabrication of GaAs laser diodes on Si using low temperature bonding of MBE grown GaAs wafers with Si wafers"*, D. Cengher, Z. Hatzopoulos, S. Gallis, [redacted], E. Aperathitis, M. Androulidaki, M. Alexe, V. Dragoi, E. D. Kyriakis-Bitzaros, G. Halkias and A. Georgakilas, J. Cryst. Growth, in print.

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2. *"A technology for GaAs-based optoelectronic integrated circuits",* D. Cengher, E. Aperathitis, M. Androulidaki, [redacted], M. Cengher, K. Amimer, Z. Hatzopoulos and A. Georgakilas, CAS 2000 Proceedings, *"2000 Int. Semiconductor Conf., October 10-14, 2000, Sinaia, Romania"*, pp. 155-158 (IEEE, Piscataway, NJ,

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3. *"III-V material and device aspects for the monolithic integration of GaAs devices on Si using GaAs/Si low temperature wafer bonding",* A. Georgakilas, M. Alexe, [redacted], D. Cengher, E. Aperathitis, M. Androulidaki, S. Gallis, Z. Hatzopoulos and G. Halkias, invited paper in CAS 2001 Proceedings, "2001 Int. Semiconductor Conf., October 9-13, 2001, Sinaia, Romania", pp. 239-244 (IEEE, Piscataway, NJ, 2001 – IEEE Catalog. No. 01TH8547).
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Chapter: 11 .Appendix A

Structure and samples used through this project

Structure 1 Wafer 50

Layer	Al content x	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
p cladding layer	0.45	0.7	undoped
p conf. layer	0.26	0.29	undoped
spacer	0.20	0.0050	undoped
OW 1	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW2	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
n conf. layer	0.26	0.29	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.30	$5\ 10^{17}$
GaAs buffer layer	0.00		

Structure 2 Wafer 53

Layer	AI content x	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$> 2\ 10^{17}$
p cladding layer	0.45	0.7	$5\ 10^{17}$
p conf. layer	0.26	0.29	undoped
spacer	0.20	0.0050	undoped
OW 1	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW2	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW3	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW4	0.00	0.0080	un doped
spacer	0.20	0.0050	undoped
n conf. layer	0.26	0.29	undoped
n cladding laver 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.30	$5\ 10^{17}$
GaAs buffer laver	0.00		

Structue 3 Wafer 54

Layer	Al content [x]	Thickness [μm]	Doping [cm-3]
p+ contact laver	0.00	0.15	$> 2\ 10^{17}$
p cladding layer	0.45	0.7	$5\ 10^{17}$
p conf. laver	0.26	0.29	undoped
spacer	0.20	0.0050	undoped
OW 1	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW3	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
QW4	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW5	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW6	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW7	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
OW8	0.00	0.0080	undoped
spacer	0.20	0.0050	undoped
n conf. layer	0.26	0.29	undoped
n cladding laver 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.30	$5\ 10^{17}$
GaAs buffer laver	0.00		

Structure 4 Wafer 65

Layer	Al content	Thickness	Doping
p+ contact layer	0.00	0.15	> 2 10^{18}
p graded layer	0.00->0.45 linear	0.1	5 10^{17}
p cladding layer	0.45	0.6	1 10^{17}
P conf. Layer	0.26	0.24	undoped
p graded conf. layer	0.26->0.2 linear	0.05	undoped
Spacer	0.20	0.0050	undoped
QW1	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
n graded conf. layer	0.2->0.26 linear	0.05	undoped
n conf. Layer	0.26	0.24	undoped
n cladding layer 1	0.45	0.35 4 / \'	1 10^{17}
n cladding layer 2	0.45	1.30	5 10^{17}
n+ graded layer	0.45->0.0 linear	0.1	2 10^{18}
GaAs buffer layer	0.00		

Structure 4a Wafer 70, 71, 73, 74, 75, 76

Layer	Al content x	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
P graded layer	0.00->0.45 linear	0.1	$5\ 10^{17}$
P cladding layer	0.45	0.6	$1\ 10^{17}$
p conf. Layer	0.26	0.24	undoped
p graded conf.	0.26->0.2 linear	0.05	undoped
Spacer	0.20	0.0050	undoped
QW 1	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
n graded conf.	0.2->0.26 linear	0.05	undoped
n conf. Layer	0.26	0.24	undoped
cladding layer1	0.45	0.25	$1\ 10^{17}$
n cladding layer 2	0.45	1.30	$5\ 10^{17}$
n+ graded layer	0.45->0.0 linear	0.1	$2\ 10^{18}$
GaAs buffer layer	0.00		

Structure 5 Wafer 71 (8QW's), 72 (16QW's)

Layer	Al content x	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$>210^{18}$
p graded layer	0.00->0.45 linear	0.1	$5\ 10^{17}$
P cladding layer	0.45	0.6	$1\ 10^{17}$
p conf. Layer	0.26	0.24	undoped
p graded conf. layer	0.26->0.2 linear	0.05	undoped
Spacer	0.20	0.0050	undoped
QW I	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW5	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW6	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW7	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW8	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
n graded conf. layer	0.2->0.26 linear	0.05	undoped
n conf. layer	0.26	0.24	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.30	$5\ 10^{17}$
n+ graded layer	0.45->0.0 linear	0.1	$2\ 10^{18}$
GaAs buffer layer	0.00		

Structure 8 Wafers: 121 (2QW's), 114+193 (4QW's), 115+120 (8QW's), 116+122 (16QW's)171 (32QW's)

Layer	Al content x	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
p+ cladding layer	0.45	0.1	$1\ 10^{18}$
P cladding layer	0.45	0.6	$1\ 10^{17}$
P conf. Layer	0.26	0.19	undoped
p graded conf. layer	0.26->0.2 linear	0.10	undoped
Spacer	0.20	0.0050	undoped
QW1	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
n graded conf. layer	0.2->0.26 linear	0.10	undoped
n conf. Layer	0.26	0.19	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.20	$5\ 10^{17}$
n+ cladding layer	0.45	0.20	$1\ 10^{18}$
GaAs buffer layer	0.00		

Structure 11 Wafer 136

Layer	Al content	Thickness	Doping
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
p+ cladding layer	0.45	0.1	$1\ 10^{17}$
p cladding layer	0.45	0.6	$1\ 10^{17}$
p confinement layer	0.26	0.29	undoped
p barrier layer	0.45	0.0050	undoped
QW1	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	0.00	0.0080	undoped
n barrier layer	0.45	0.0050	undoped
n confinement layer	0.26	0.29	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.20	$5\ 10^{17}$
n+ cladding layer	0.45	0.20	$1\ 10^{18}$
GaAs buffer la er	0.00		

Structure 12 Wafer 137

Layer	Al content	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
p+ cladding layer	0.45	0.1	$1\ 10^{17}$
p cladding layer	0.45	0.6	$1\ 10^{17}$
p confinement layer	0.26	0.29	undoped
p barrier layer	0.35	0.0050	undoped
QW1	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	0.00	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	0.00	0.0080	undoped
n barrier layer	0.35	0.0050	undoped
n confinement layer	0.26	0.29	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.20	$5\ 10^{17}$
n+ cladding layer	0.45	0.20	$1\ 10^{18}$
GaAs buffer layer .	0.00		

Structure 13 Wafer 191 (2QW's), 192 (4QW's), 190 GaAs QW's

Layer	Al content	Thickness [μm]	Doping [cm-3]
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
p+ cladding layer	0.45	0.1	$1\ 10^{17}$
p cladding layer	0.45	0.6	$1\ 10^{17}$
p confinement	0.26	0.29	undoped
Spacer	0.20	0.0050	undoped
QW1	$In_{O.I}Ga_{O.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	$In_{O.I}Ga_{0.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	$In_{O.I}Ga_{0.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	$In_{O.I}Ga_{0.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
n confinement layer	0.26	0.29	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.20	$5\ 10^{17}$
n+ cladding layer	0:45	0.20	$1\ 10^{18}$
GaAs buffer layer	0.00		

Structure 14

Layer	Al content	Thickness	Doping
p+ contact layer	0.00	0.15	$> 2\ 10^{18}$
p+ cladding layer	0.45	0.1	$1\ 10^{17}$
p cladding layer	0.45	0.6	$1\ 10^{17}$
p confinement layer	0.26	0.29	undoped
p barrier layer	0.45	0.0050	undoped
QW1	$In_{0.1}Ga_{0.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW2	$In_{0.1}Ga_{0.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW3	$In_{0.1}Ga_{0.8}As$	0.0080	undoped
Spacer	0.20	0.0050	undoped
QW4	$In_{0.1}Ga_{0.8}As$	0.0080	undoped
n barrier layer	0.45	0.0050	undoped
n confinement layer	0.26	0.29	undoped
n cladding layer 1	0.45	0.35	10^{17}
n cladding layer 2	0.45	1.20	$5\ 10^{17}$
n+ cladding layer	0.45	0.20	$1\ 1O^{18}$
GaAs buffer layer	0.00		

Structure 15 Wafer 130 Reverse Structure

Layer	Al content x	Thickness [μm]	Doping [cm-3]
n+ GaAs butter	0.00	3.00	$2\ 10^{18}$
n+ graded layer	0.0->0.45 linear	0.10	$2\ 10^{18}$
n+ cladding	0.45	0.20	$2\ 10^{18}$
n cladding layer 2	0.45	1.20	$5\ 10^{17}$
n cladding layer 1	0.45	0.25	10^{17}
n graded layer	0.45->0.26 linear	0.10	10^{17}
n conf. Layer	0.26	0.19	Undoped
	0.26->0.2 linear	0.10	Undoped
Spacer	0.20	0.0050	Undoped
QW4	0.00	0.0080	Undoped
Spacer	0.20	0.0050	Undoped
QW3	0.00	0.0080	U ndoped
Spacer	0.20	0.0050	Undoped
QW2	0.00	0.0080	U ndoped
Spacer	0.20	0.0050	U ndoped
QW 1	0.00	0.0080	U ndoped
Spacer	0.20	0.0050	Undoped
p graded conf.	0.26->0.2 linear	0.10	Undoped
p con f. Layer	0.26	0.19	U ndoped
p cladding layer	0.45	0.6	$1\ 10^{17}$
p+ cladding layer	0.45	0.1	$1\ 10^{18}$
p+ graded layer	0.45->0.0 linear	0.10	$2\ 10^{17}$
p+ contact layer	0.00	0.25	$> 2\ 10^{18}$
GaAs buffer	0.00	0.10	U ndoped
AlAs	1.00	0.05	-
GaAs buffer	0.00	0.10	Undoped
Substrate	0.00		