Appendix C

Schematics

C.1 Codec overview

Fig. C.1 Codec Overview with JTAG controller.

Fig. C.2 Overview of the 4 Units.

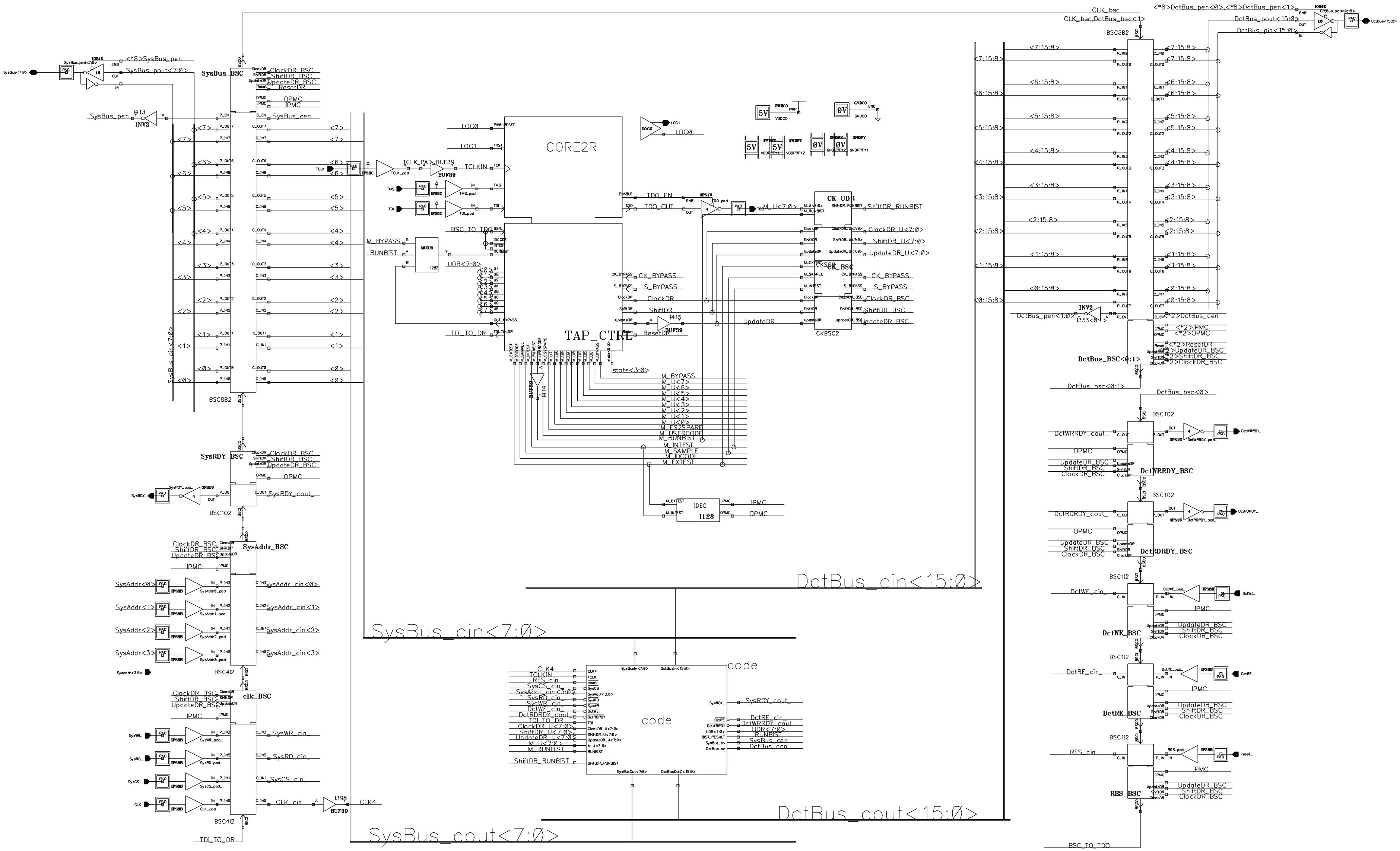

Fig. C.1: Codec Overview with JTAG controller.

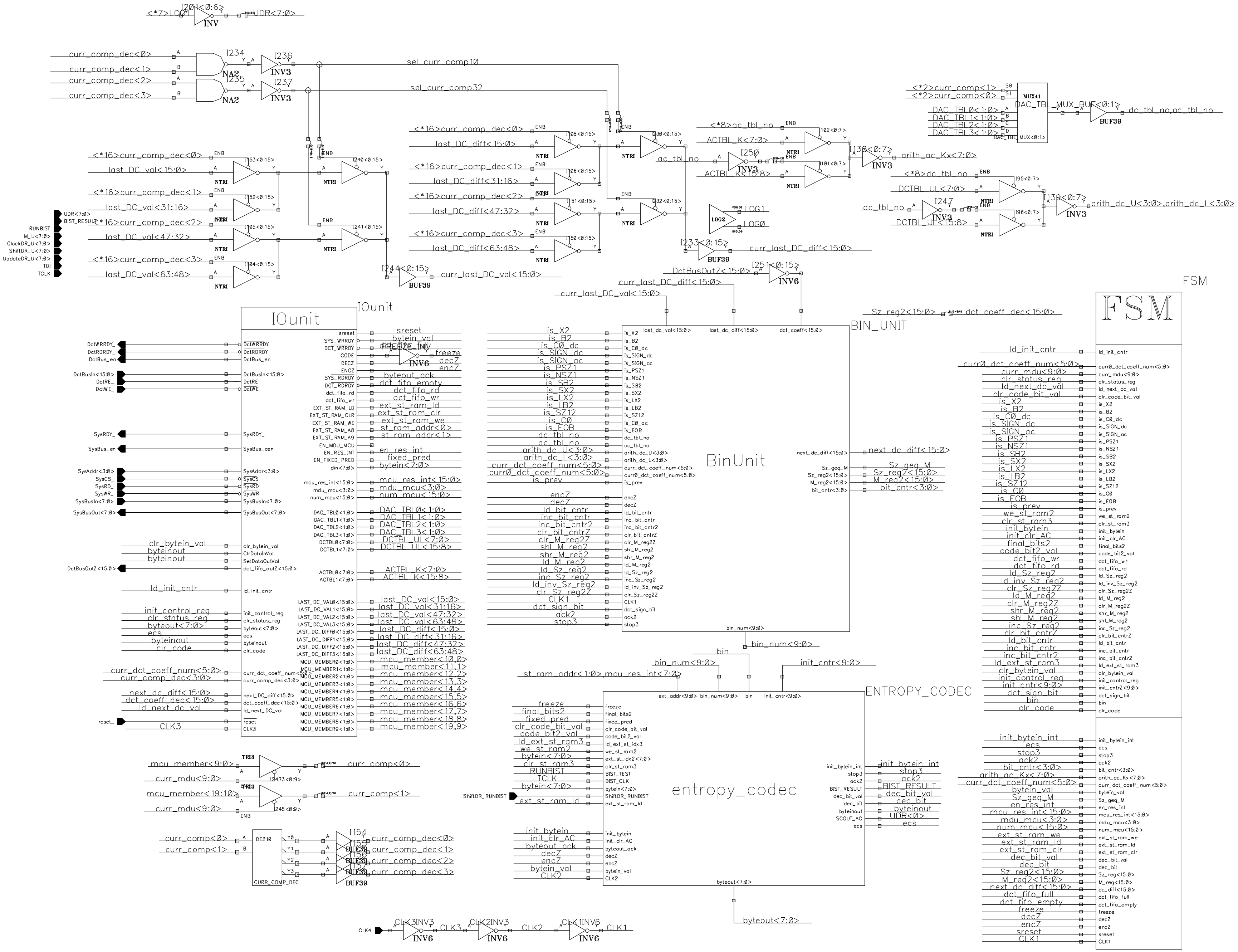

Fig. C.2: Overview of the 4 Units.

C.2 Global Control Unit

Fig. C.3 Global FSM.

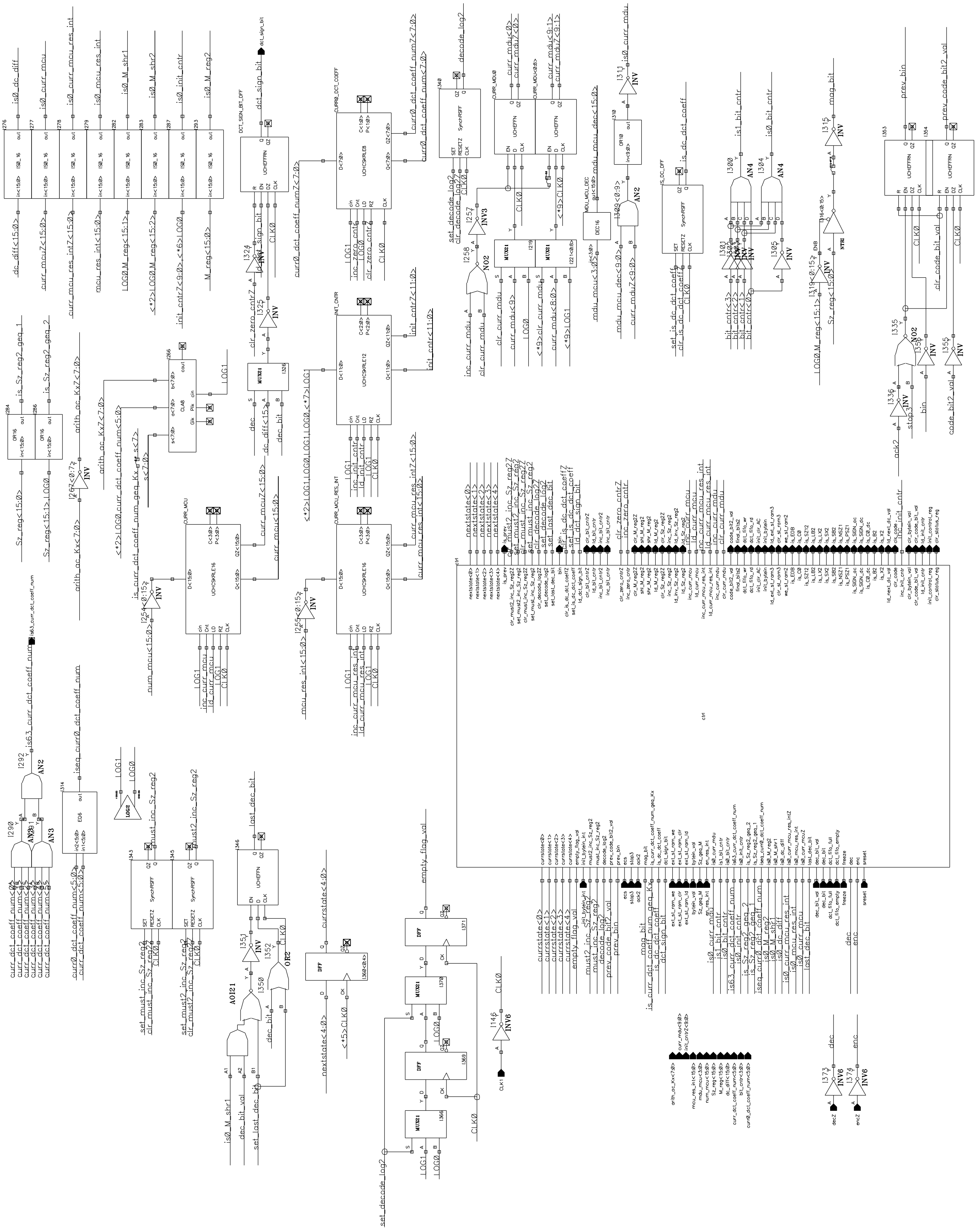

Fig. C.3: Global FSM

C.3 System and DCT bus Interface

Fig. C.4 I/O Interface.

Fig. C.5 System bus Interface.

Fig. C.6 Dct Bus Interface.

Fig. C.7 Register read demultiplexer.

Fig. C.8 System bus synchronization circuits.

Fig. C.9 Dct bus synchronization circuits.

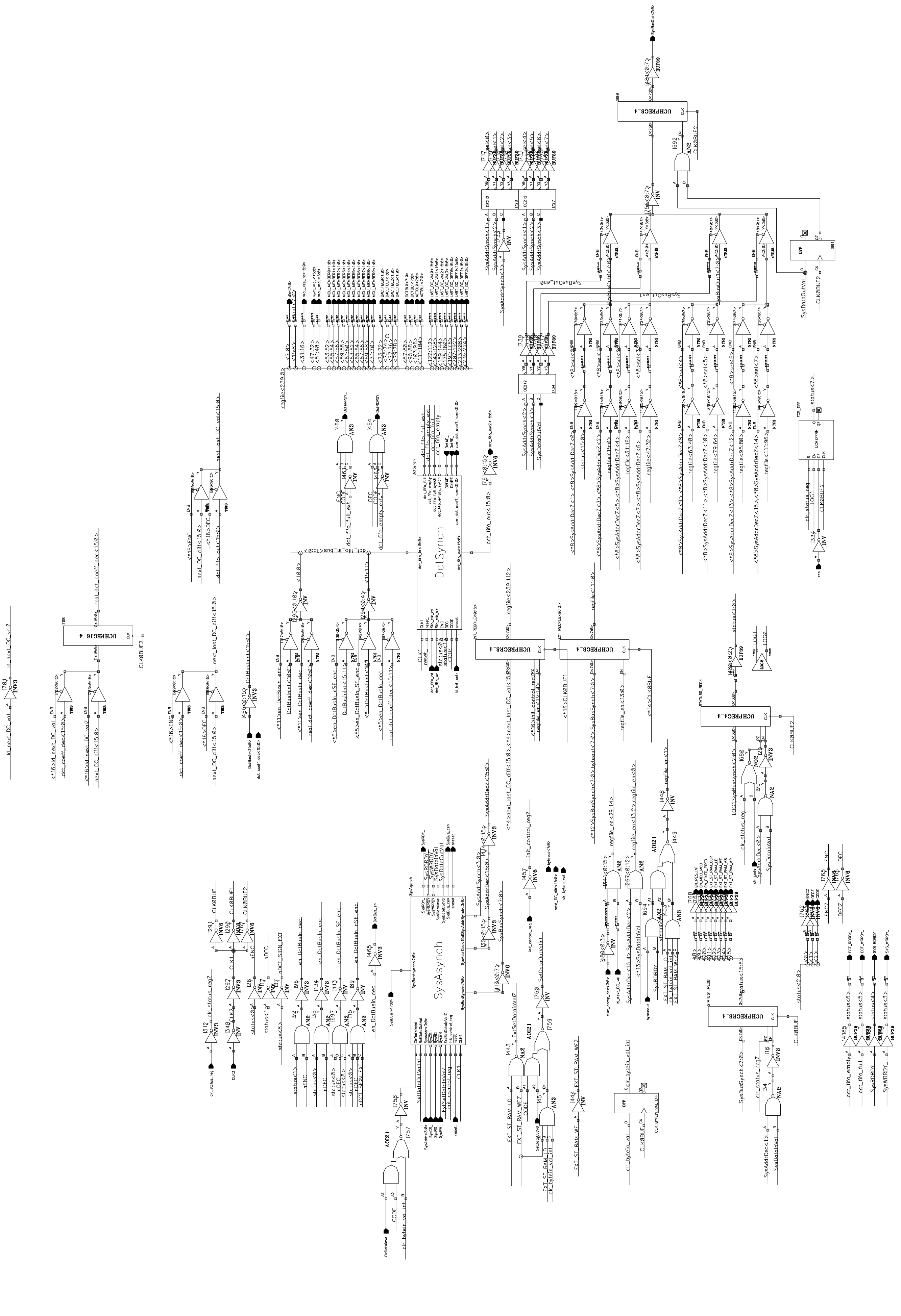

Fig. C.4: I/O Interface.

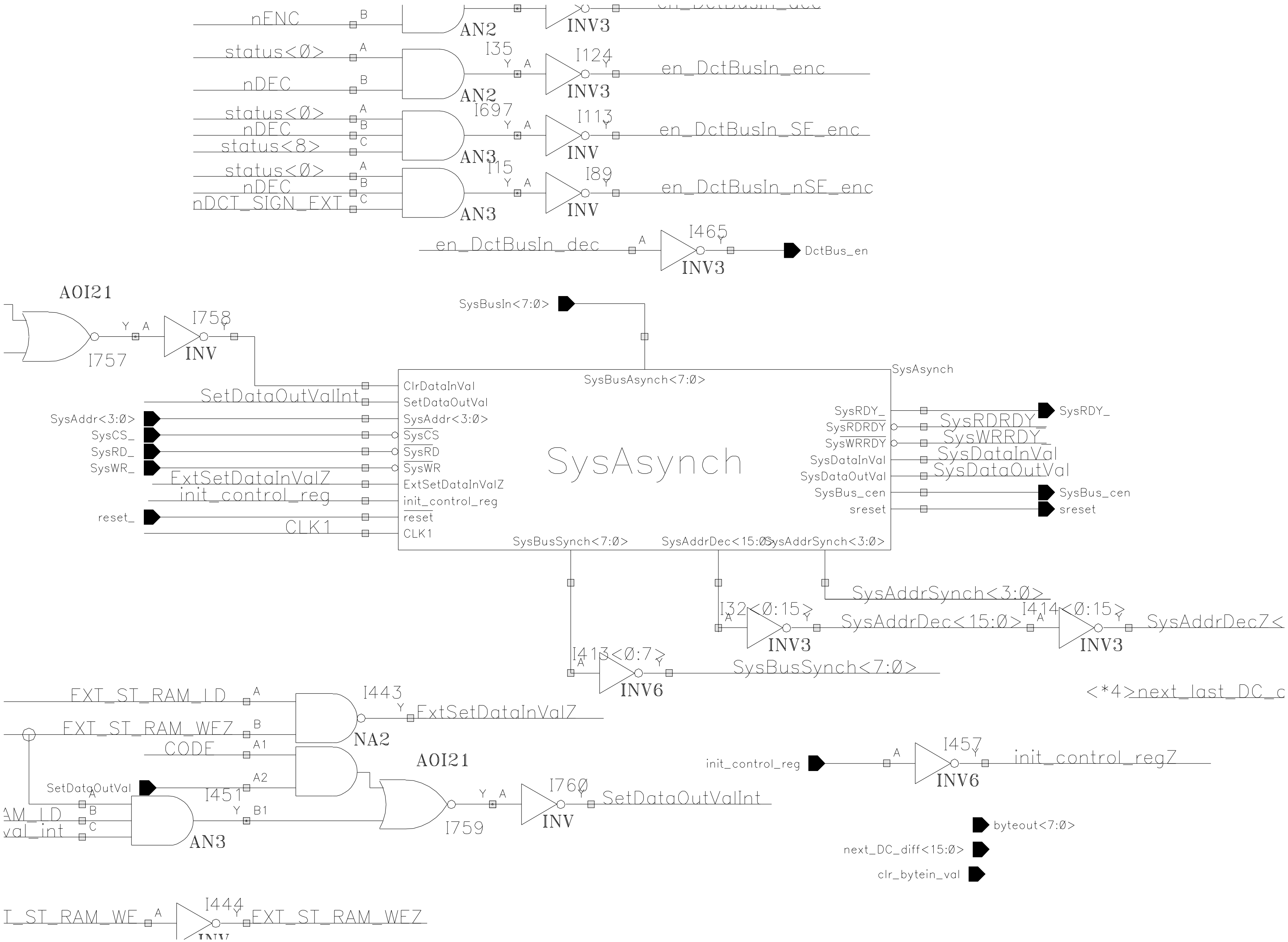

Fig. C.5: System bus Interface.

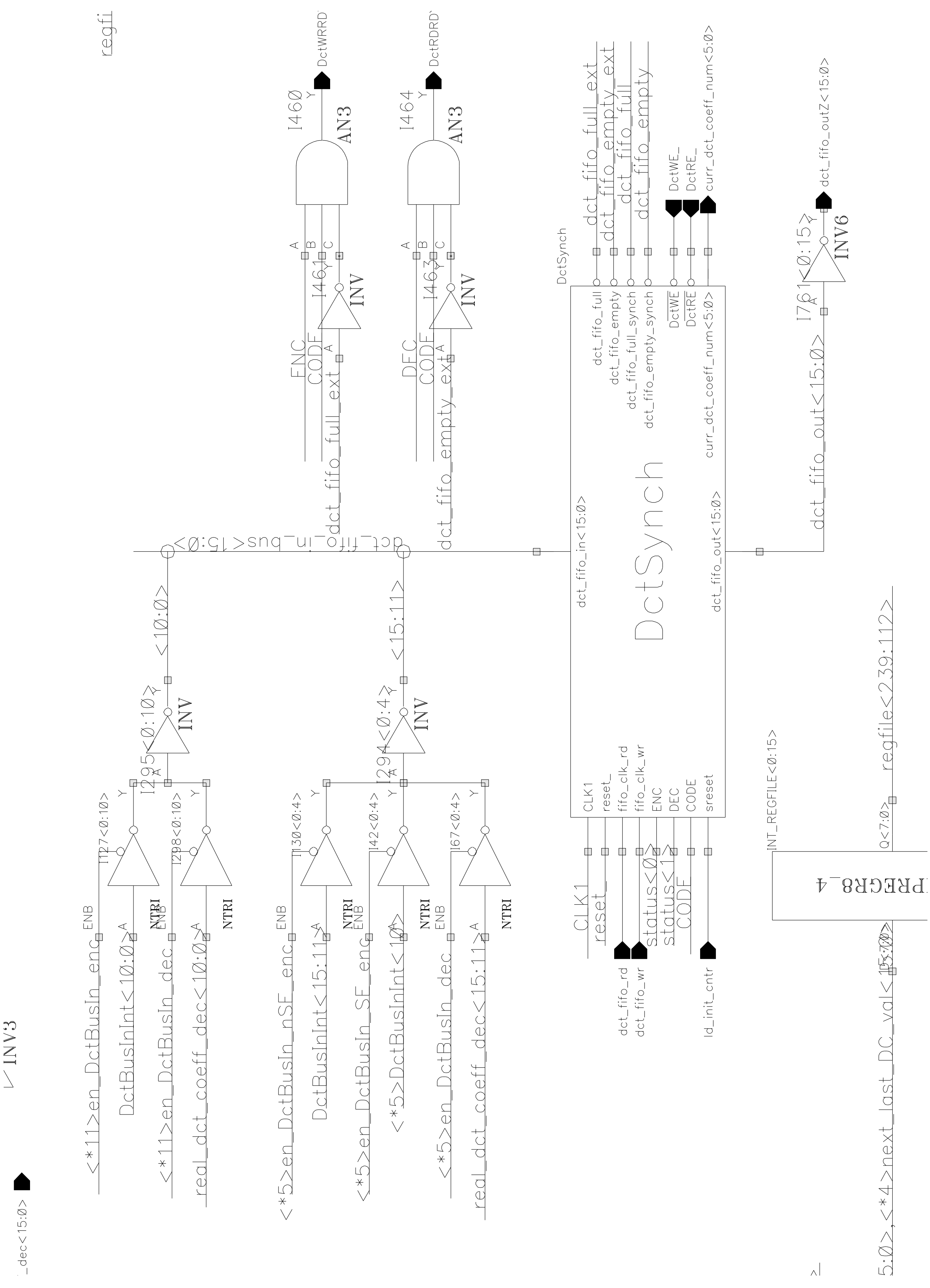

Fig. C.6: Dct Bus Interface.

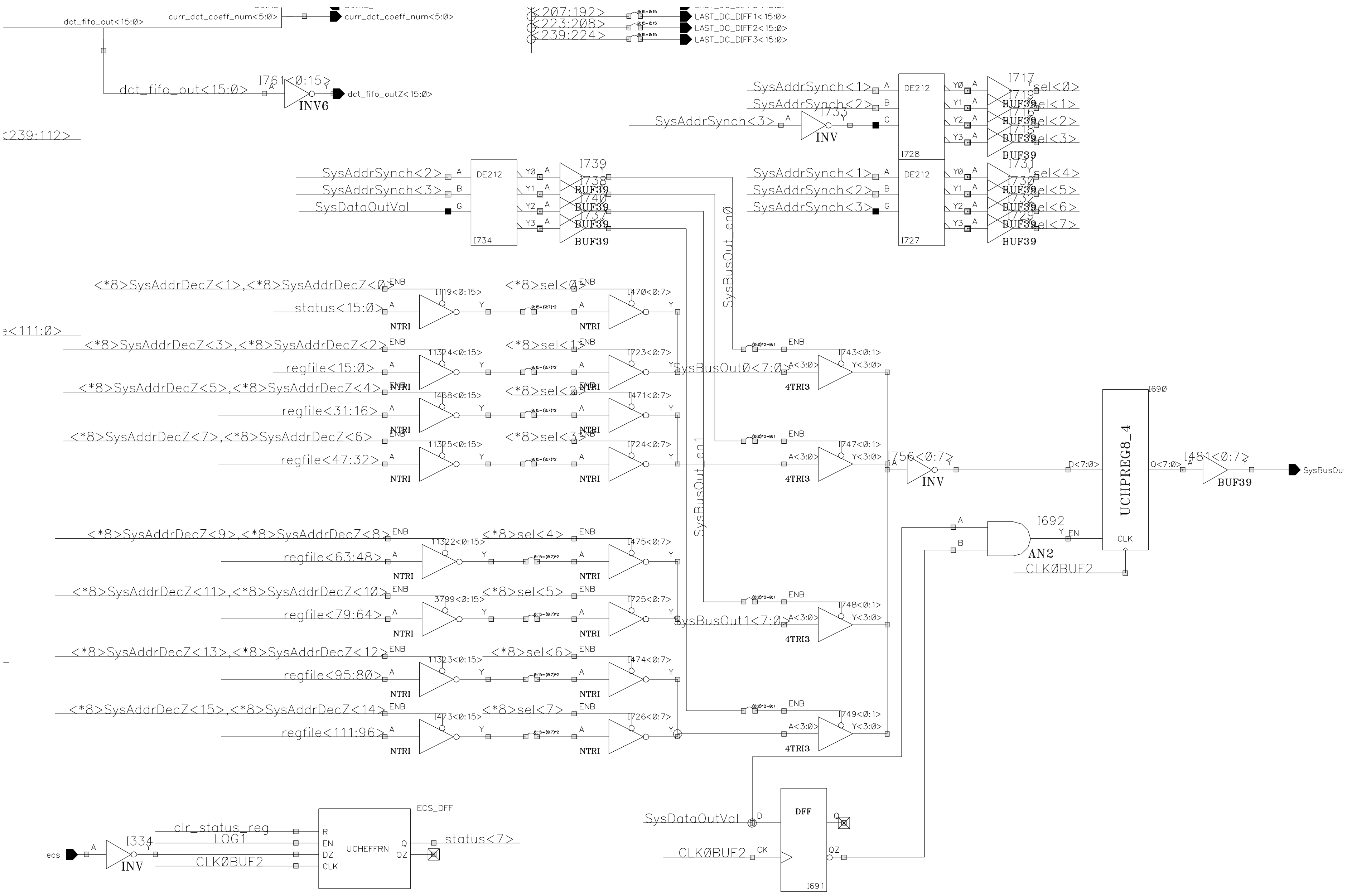

Fig. C.7: Register read demultiplexer.

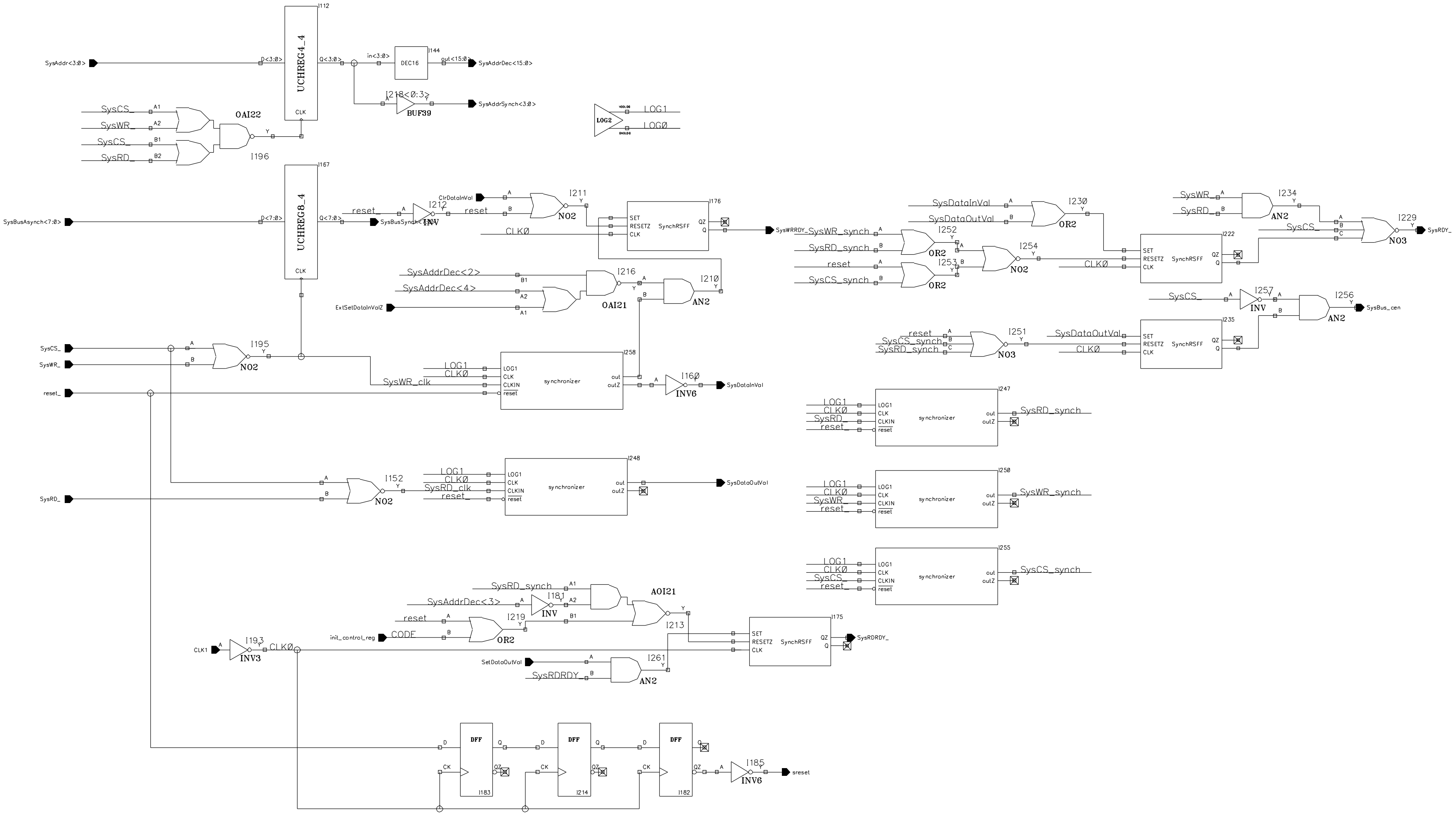

Fig. C.8: System bus synchronization circuits.

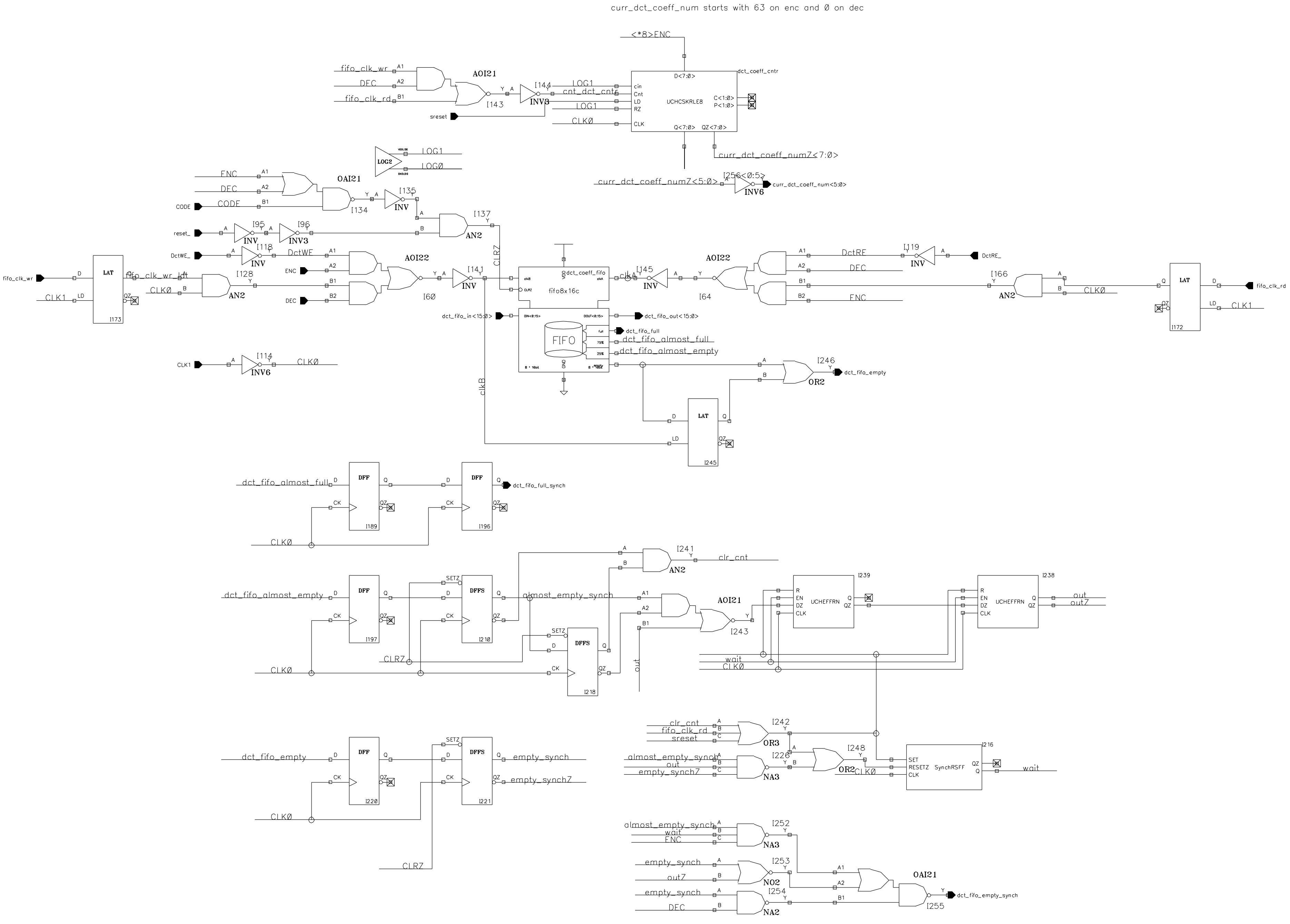

Fig. C.9: Dct bus synchronization circuits.

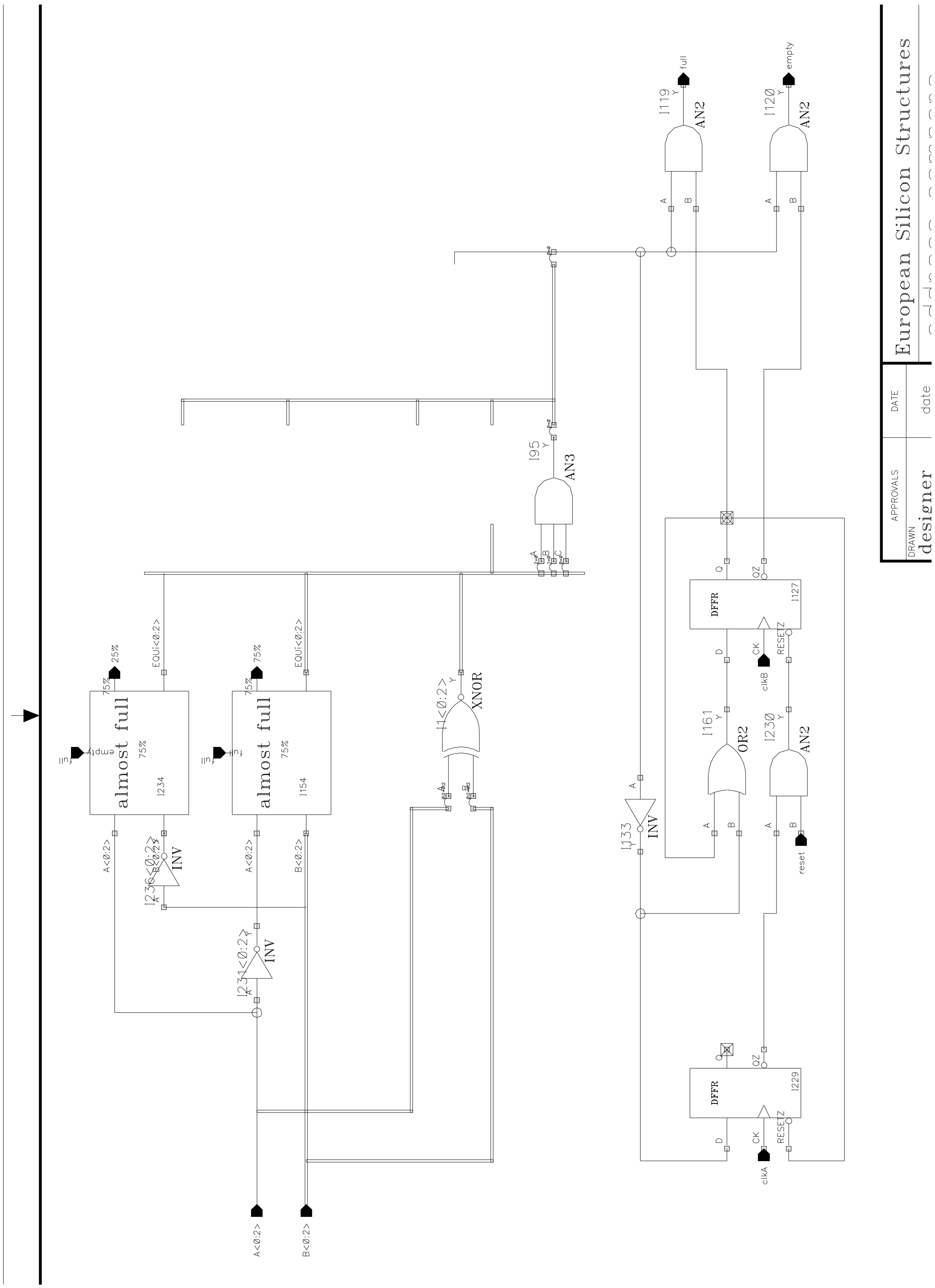

Fig. C.10: dctfifoflags.ps

C.4 Statistical Model Unit

Fig. C.11 Statistical Model Unit overview.

Fig. C.12 Context generation circuit.

Fig. C.13 DC-DIFF generation circuit.

Fig. C.14 LU and Kx conditional coding parameters.

Fig. C.15 Sz register.

Fig. C.16 M register.

Fig. C.17 Internal M register circuit.

Fig. C.18 Internal DC-DIFF circuit.

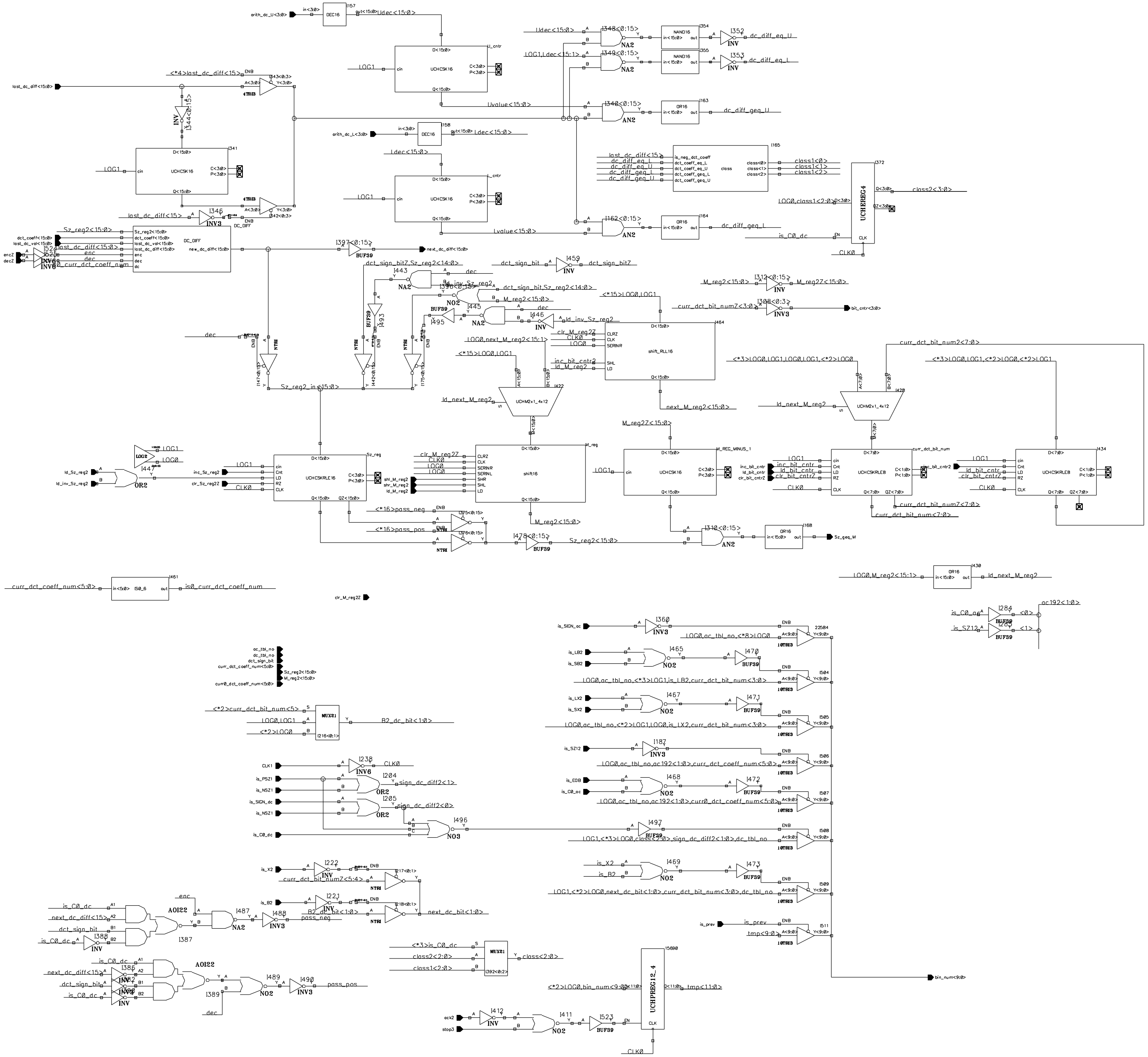

Fig. C.11: Statistical Model Unit overview.

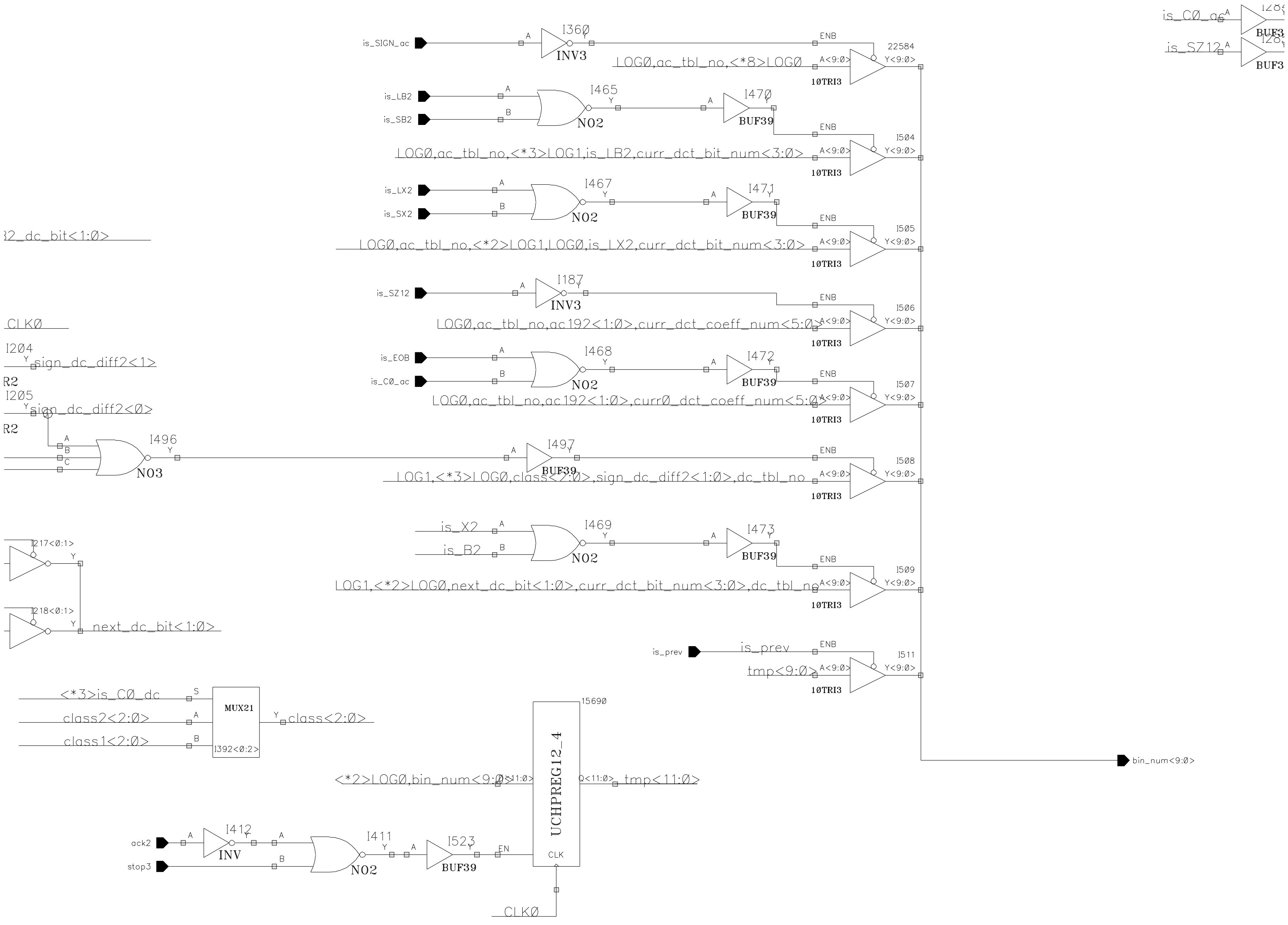

Fig. C.12: Context generation circuit.

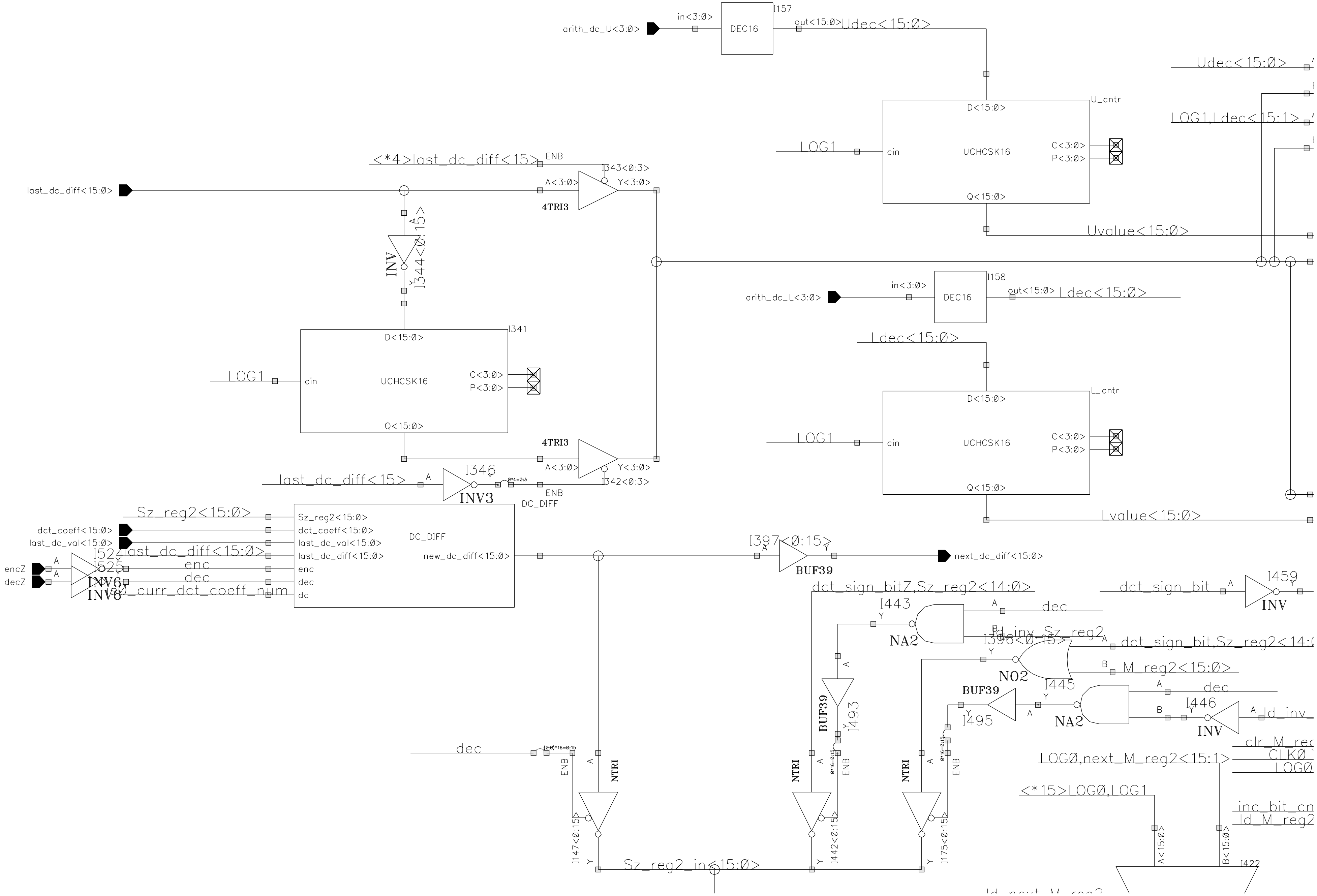

Fig. C.13: DC-DIFF generation circuit.

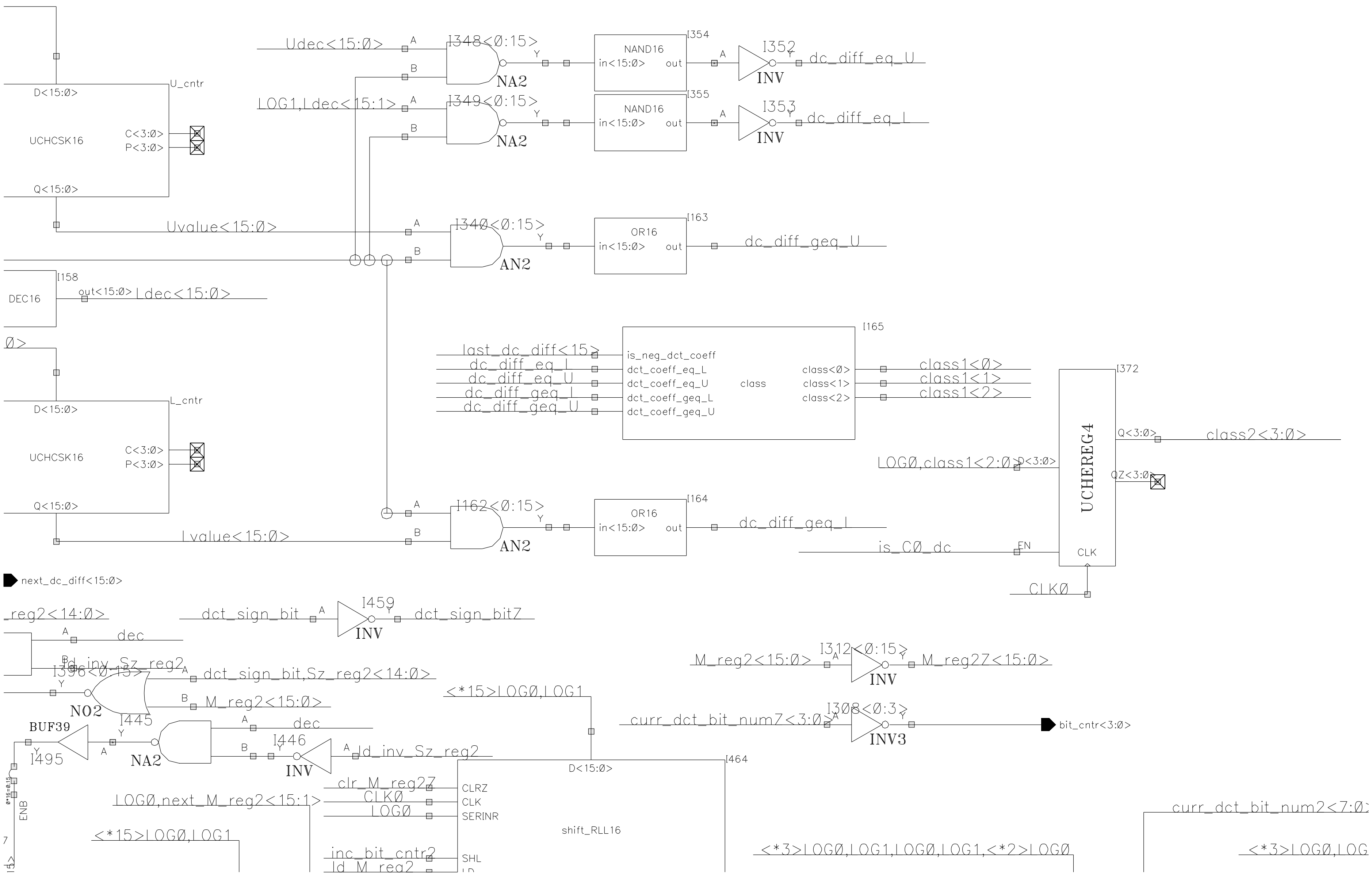

Fig. C.14: LU and Kx conditional coding parameters.

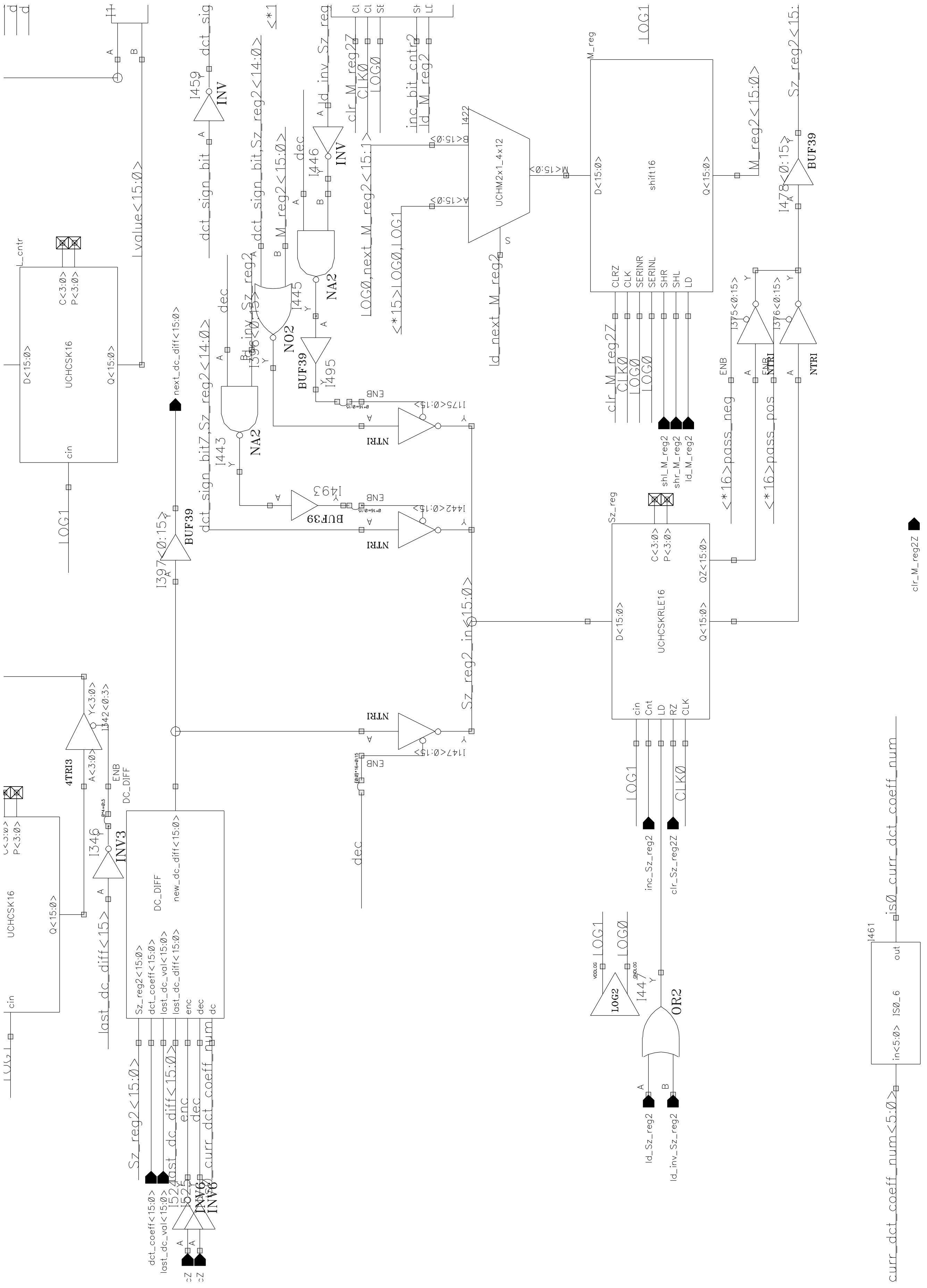

Fig. C.15: Sz register.

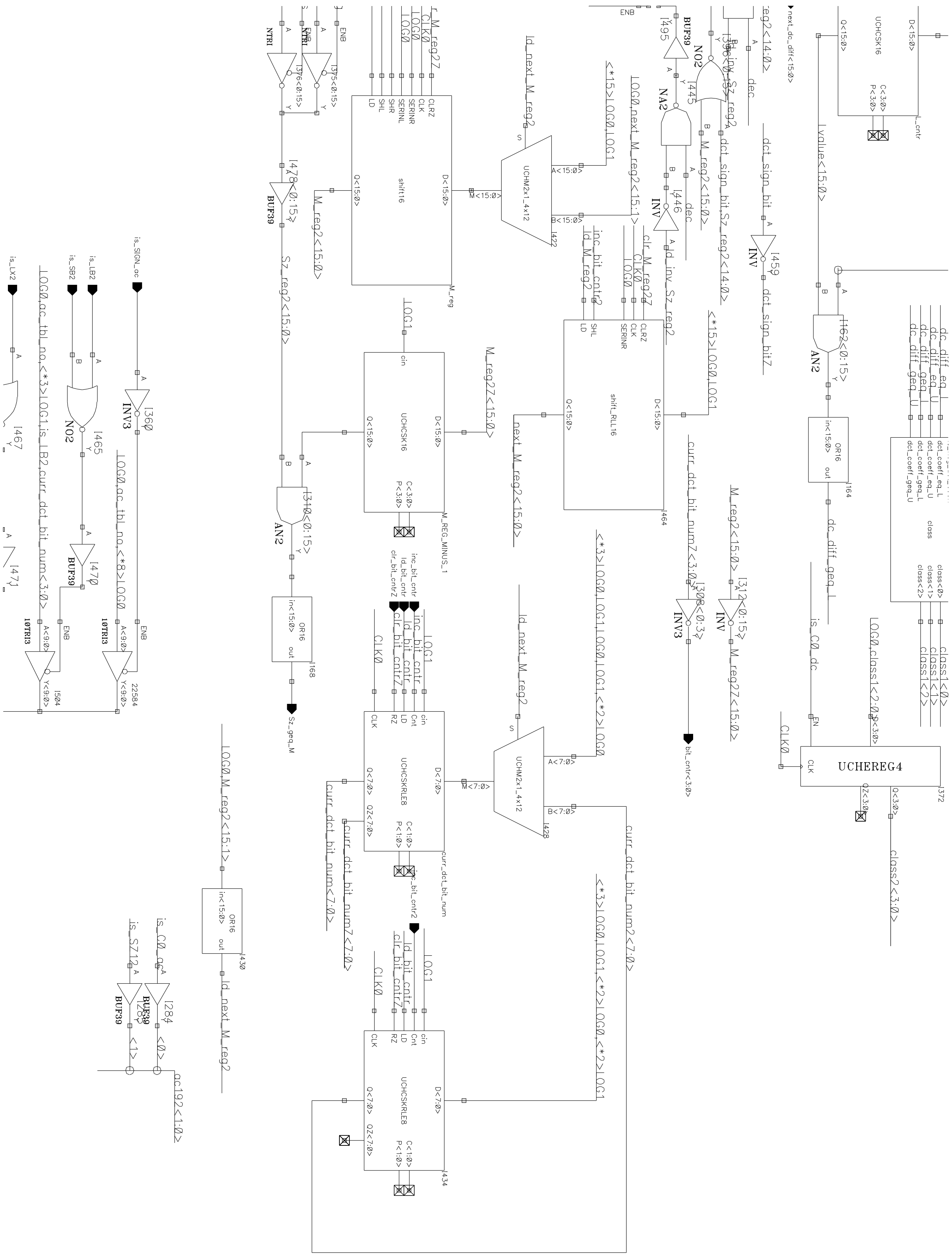

Fig. C.16: M register.

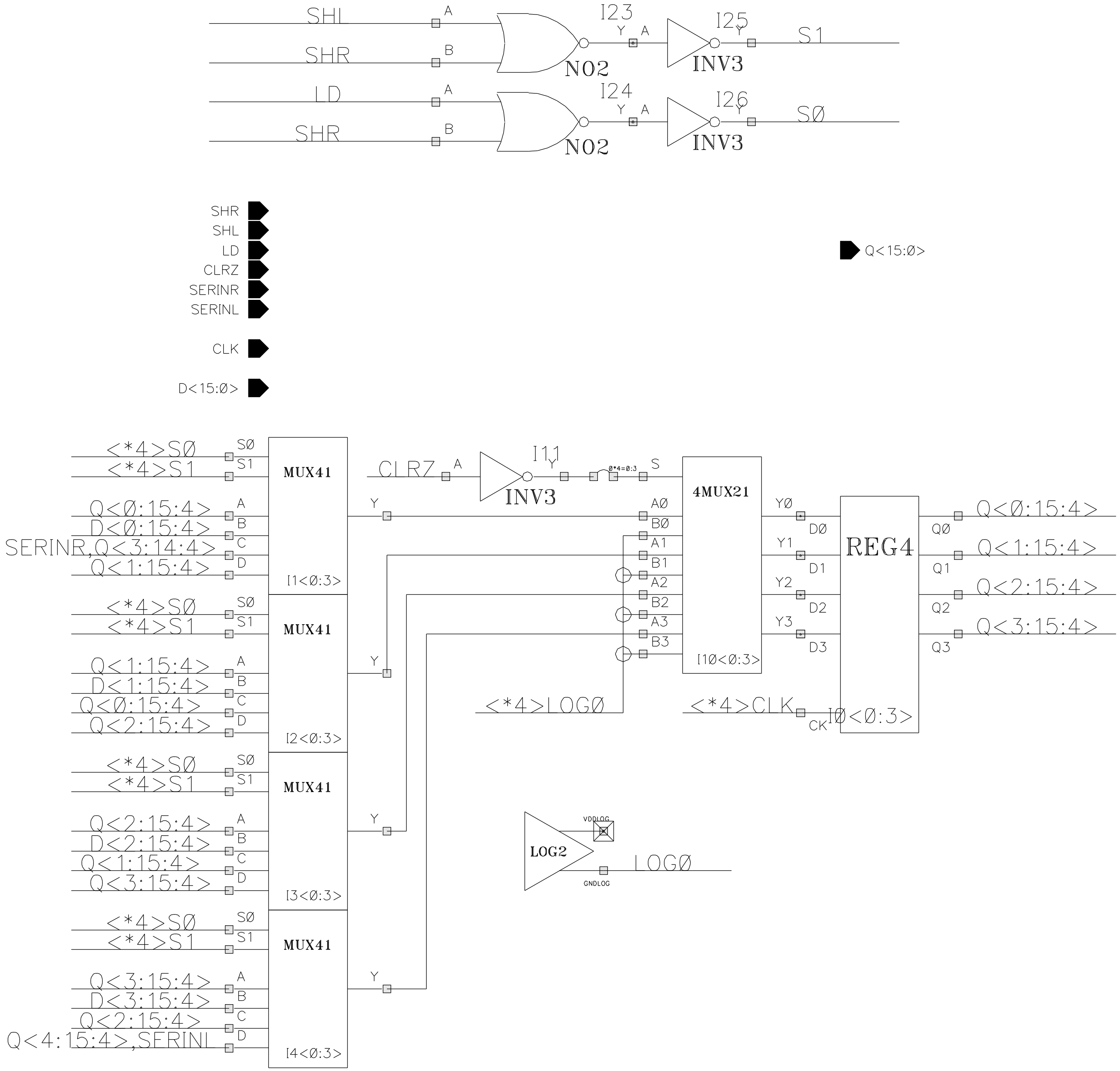

Fig. C.17: Internal M register circuit.

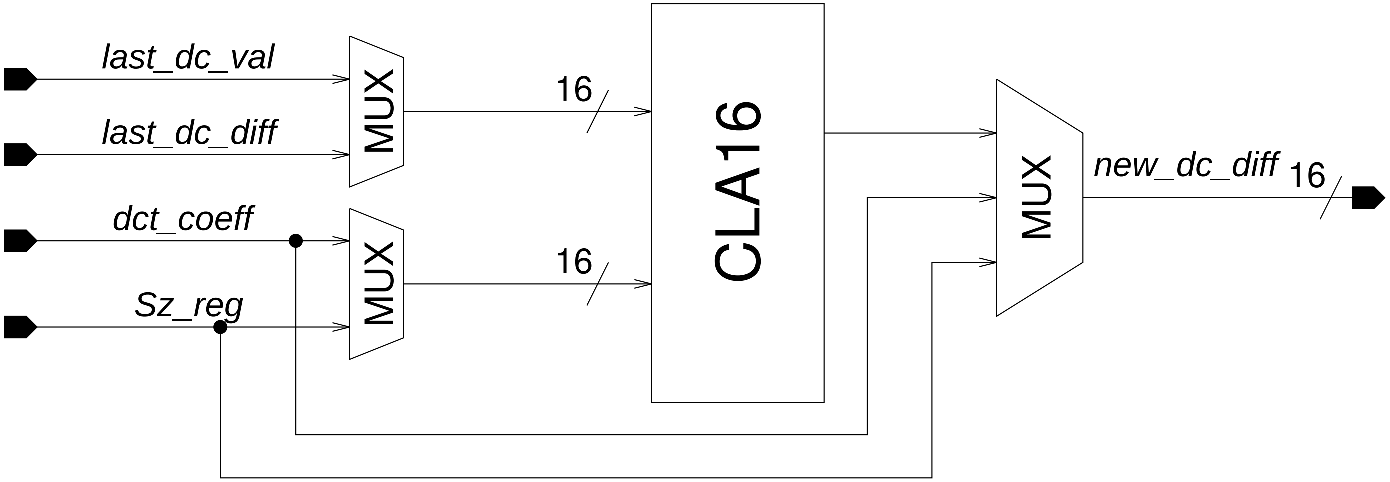

Fig. C.18: Internal DC-DIFF circuit.

C.5 Probability Estimation Unit

Fig. C.19: Probability estimation state machine overview.

Fig. C.20: Pipeline stages 3 and 4.

Fig. C.21: Probability estimation PLA.

Fig. C.22: Context area static RAM.

Fig. C.23: Probability estimation control unit.

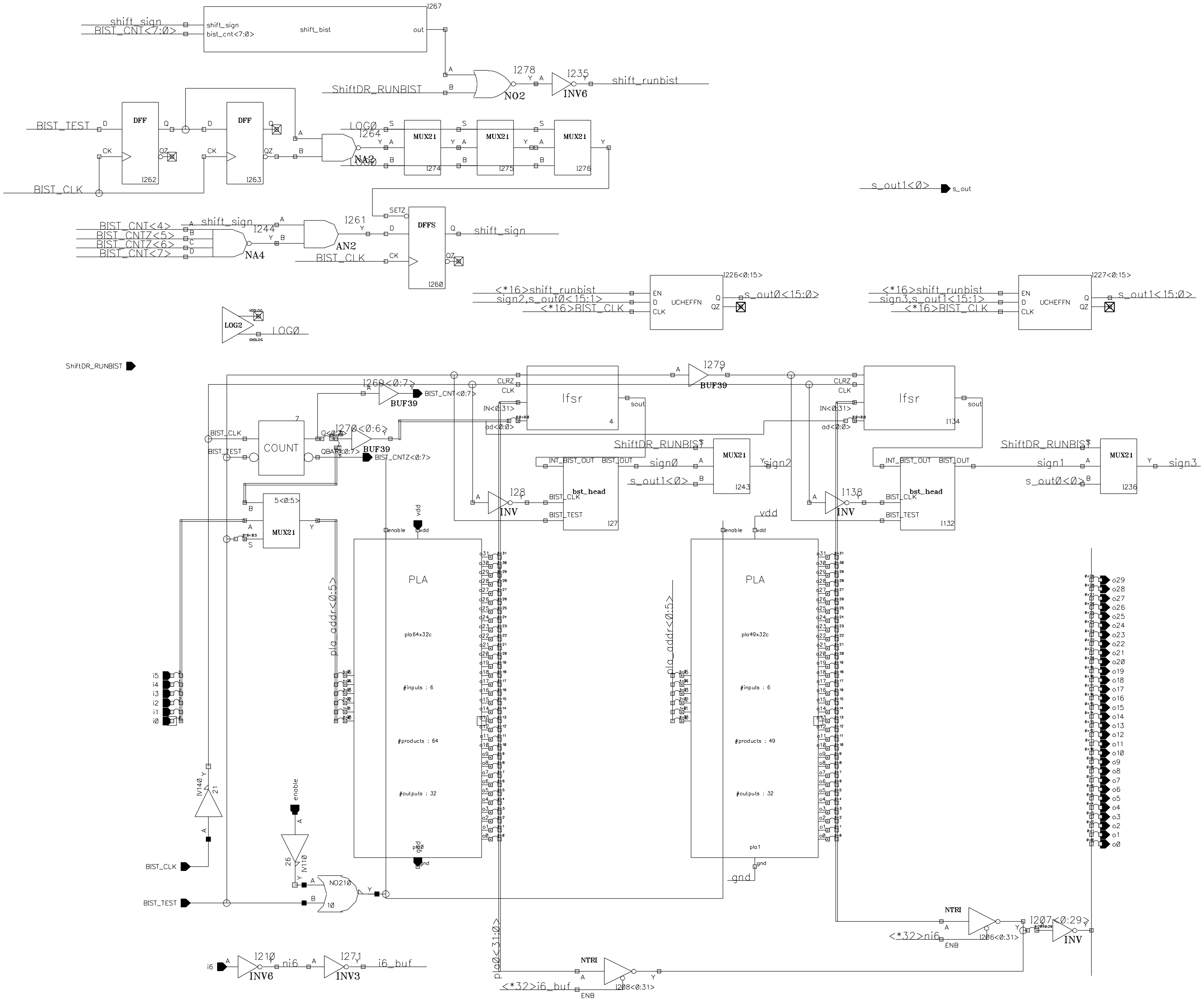

Fig. C.19: Probability estimation state machine overview.

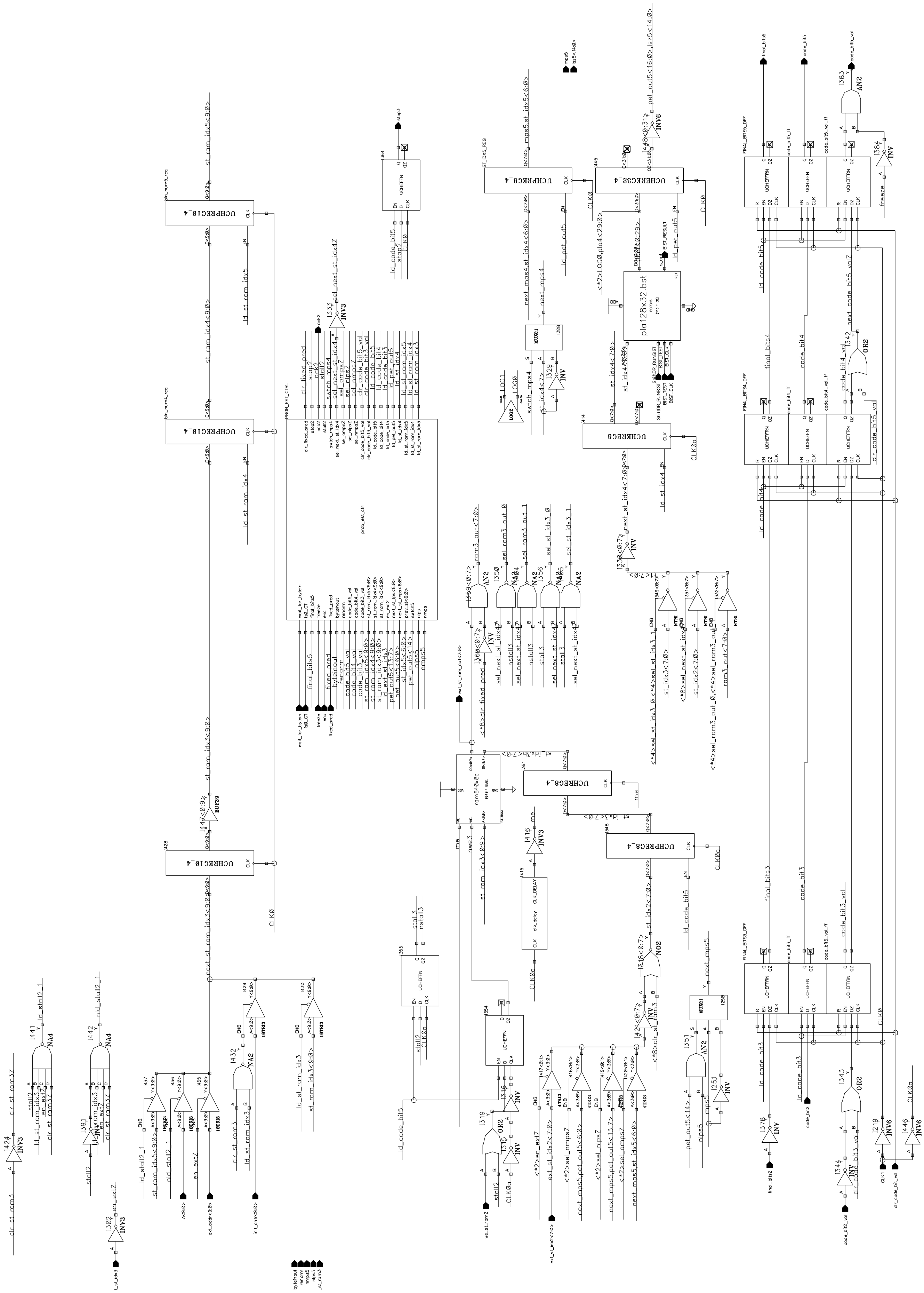

Fig. C.20: Pipeline stages 3 and 4.

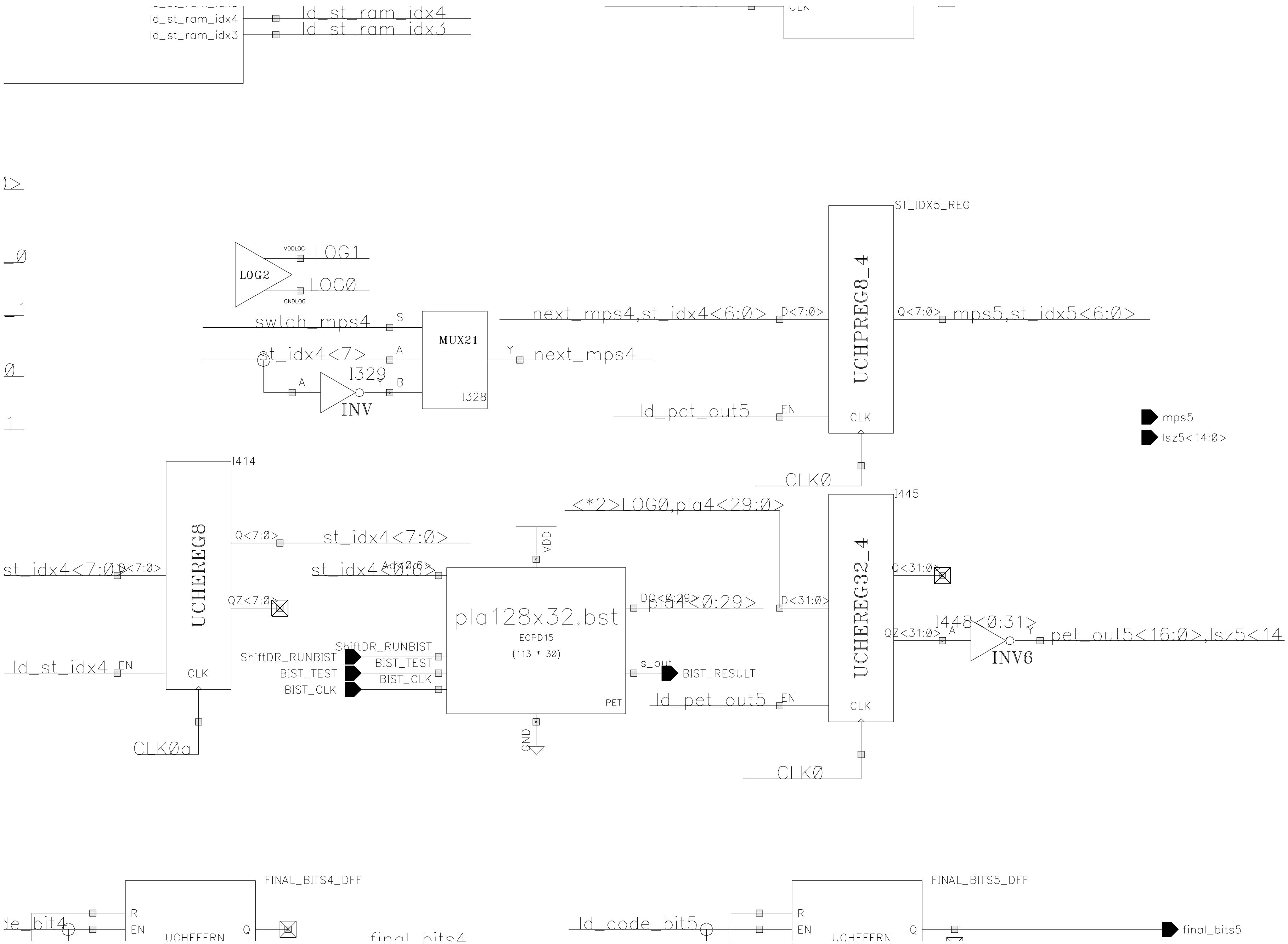

Fig. C.21: Probability estimation PLA.

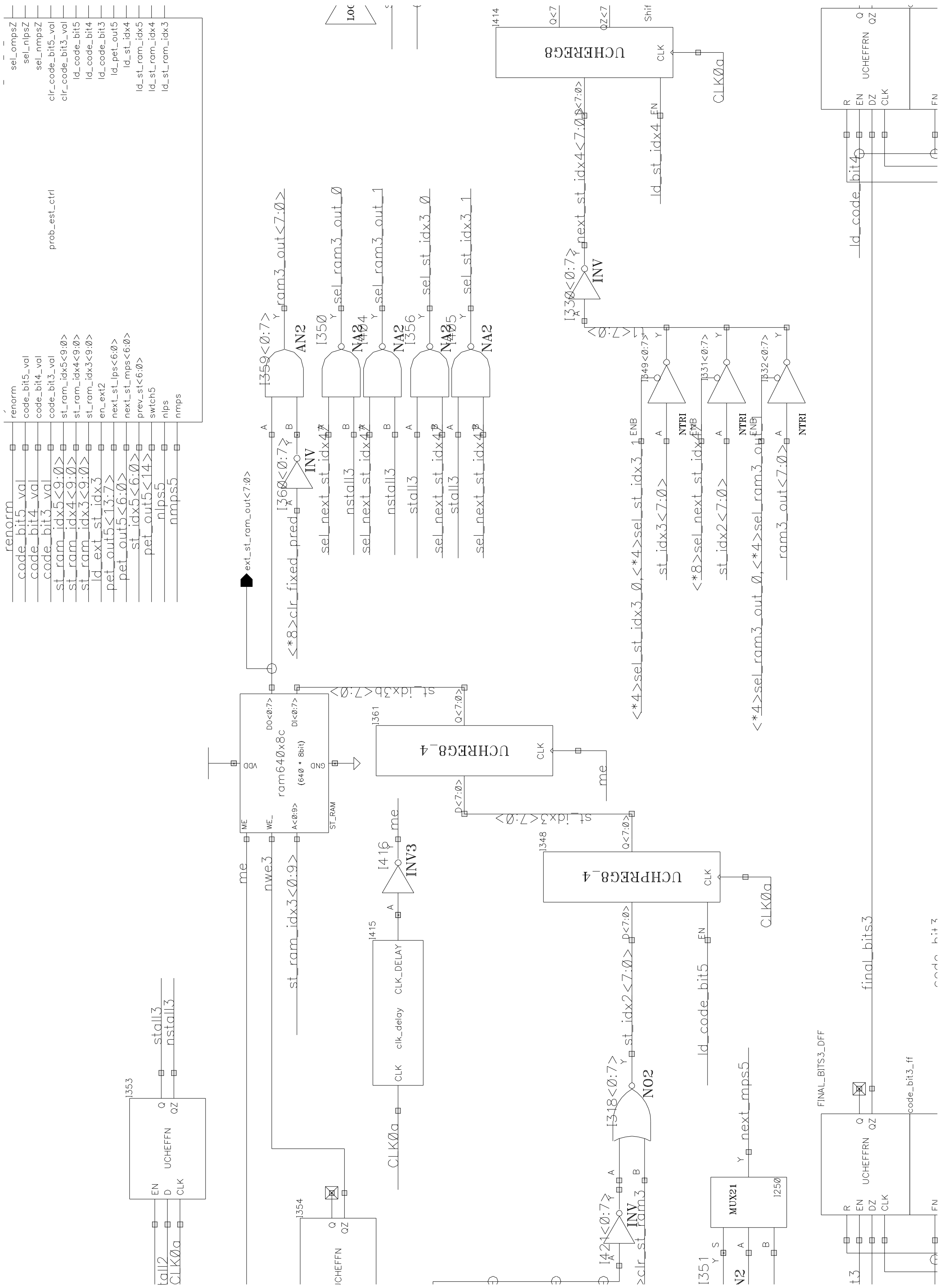

Fig. C.22: Context area static RAM.

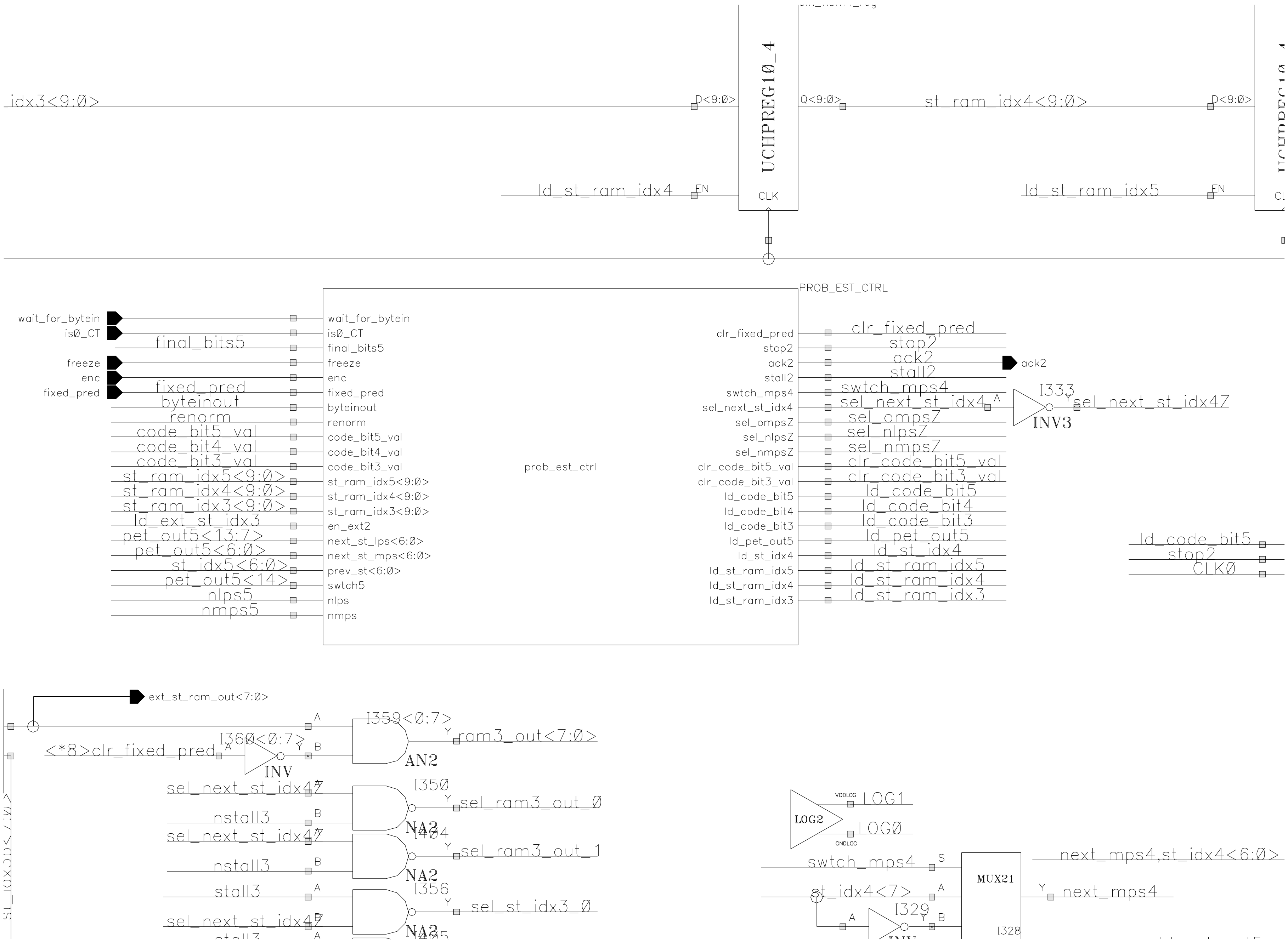

Fig. C.23: Probability estimation control unit.

C.6 Arithmetic Coding Unit

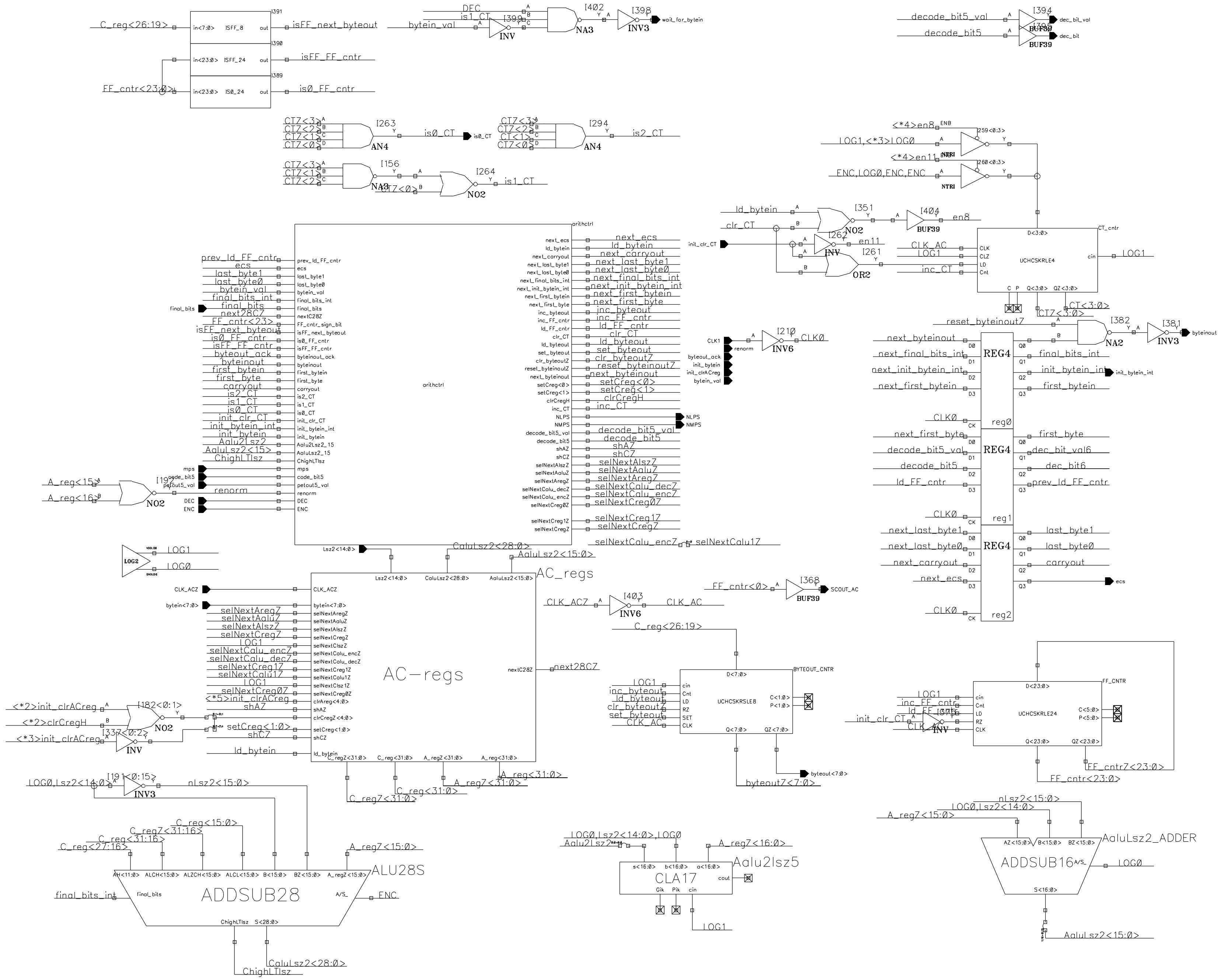

Fig. C.24: Arithmetic Coding Unit overview.

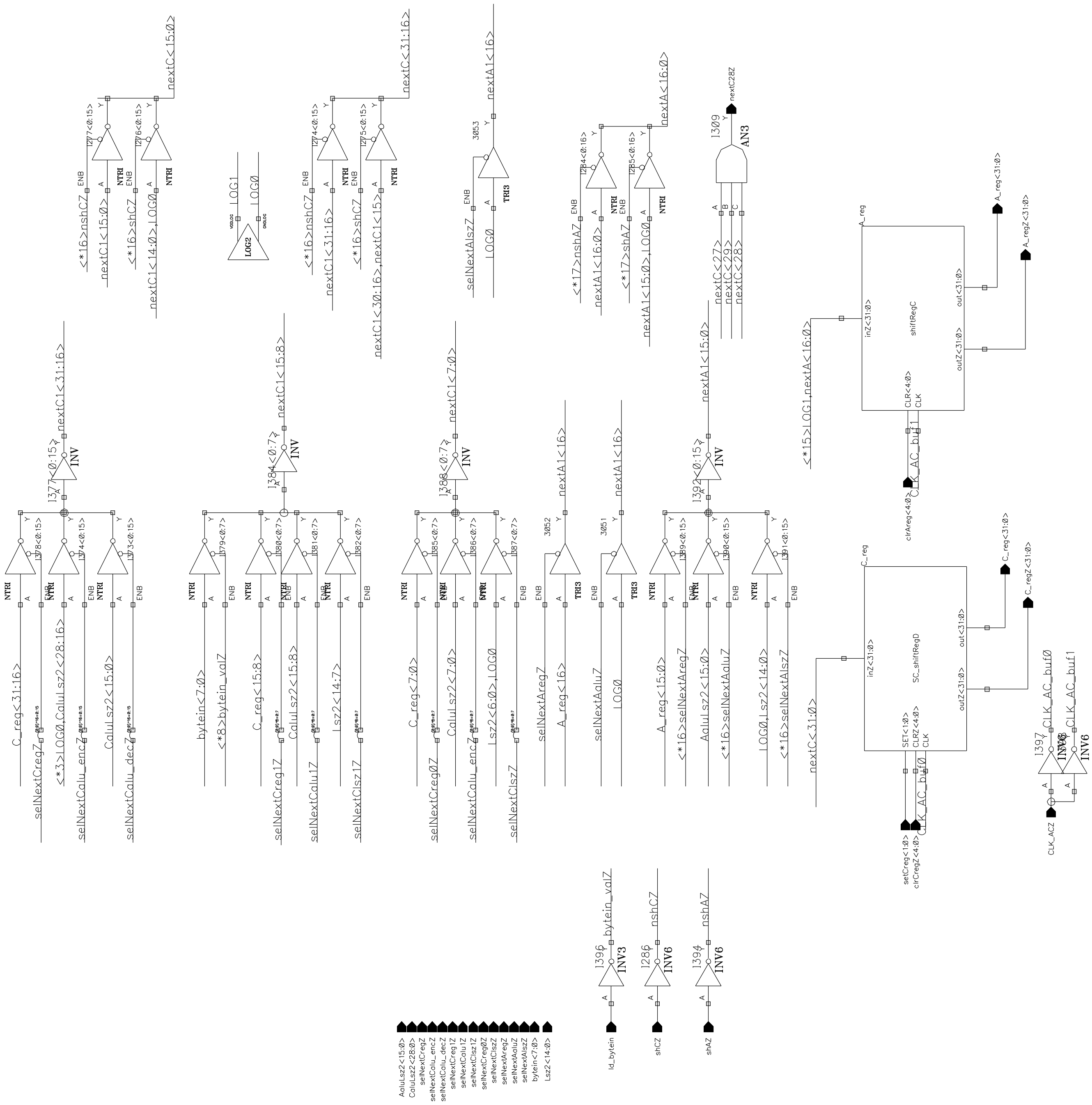

Fig. C.25: A and C registers.

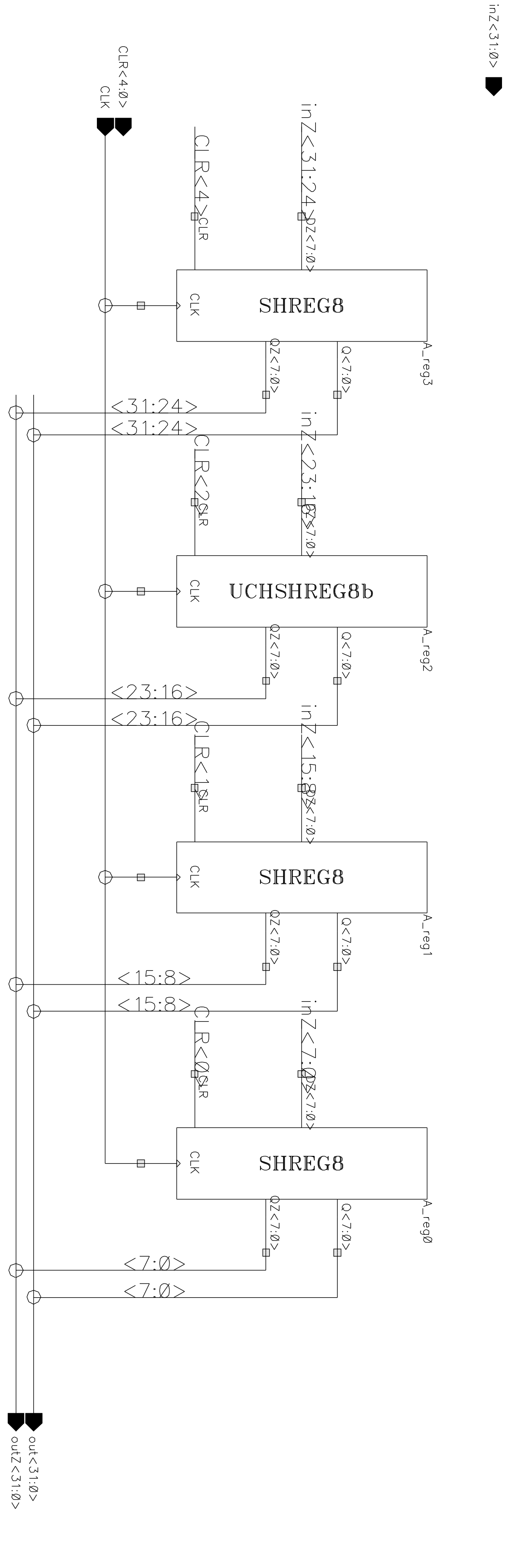

Fig. C.26: A register.

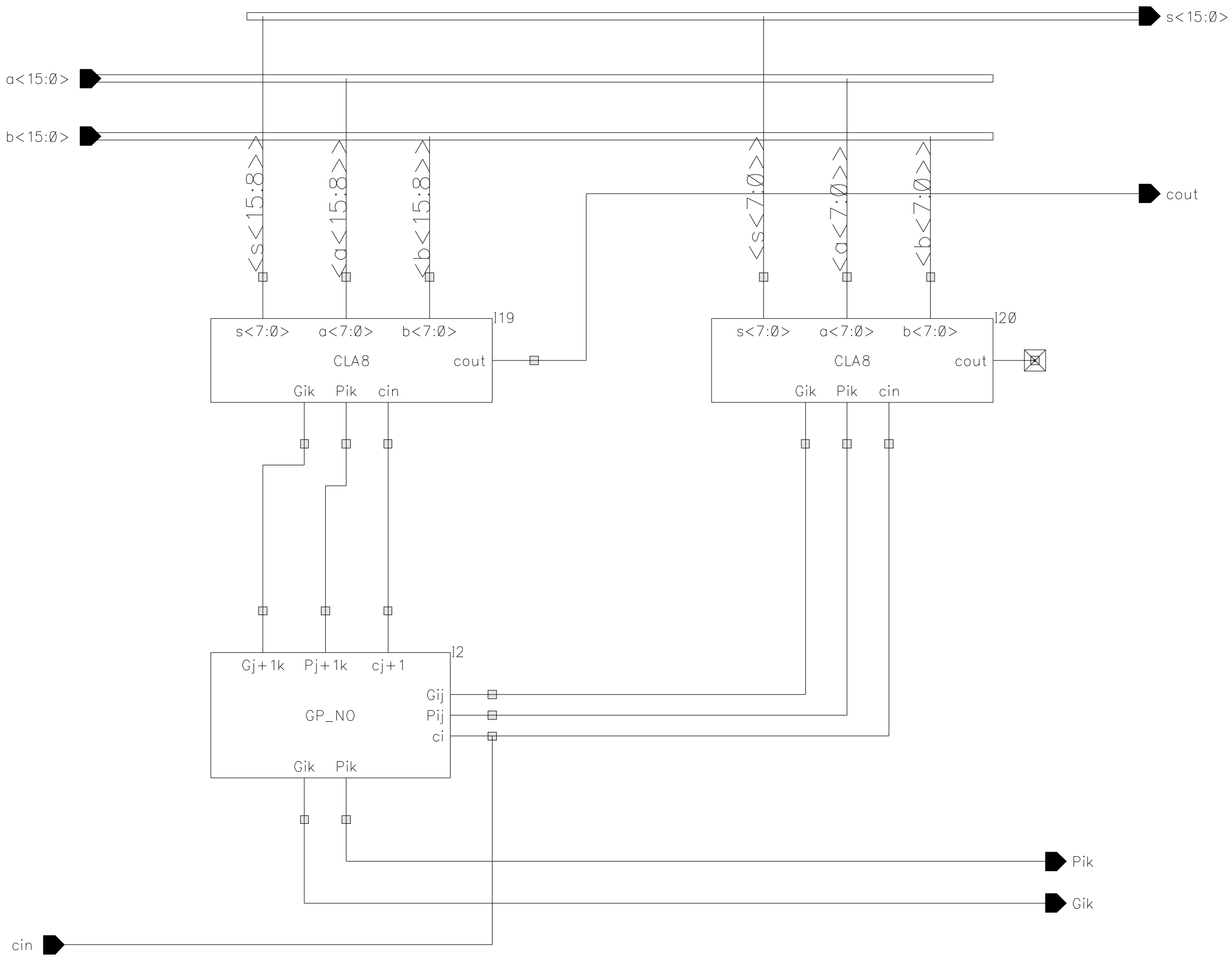

Fig. C.27: 16-bit CLA composed hierarchically from 8-bit CLA.

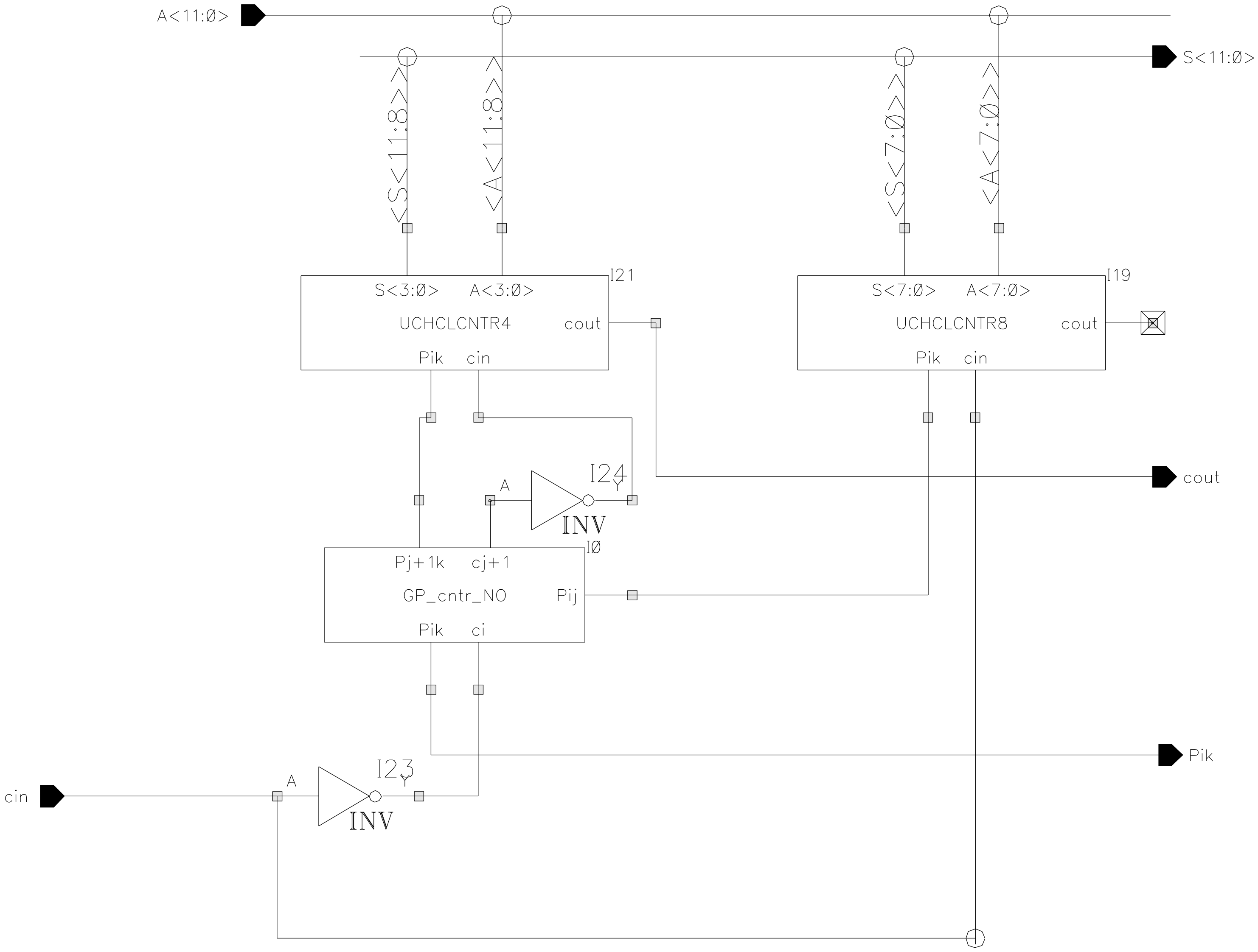

Fig. C.28: 12-bit counters designed as CL incrementor.

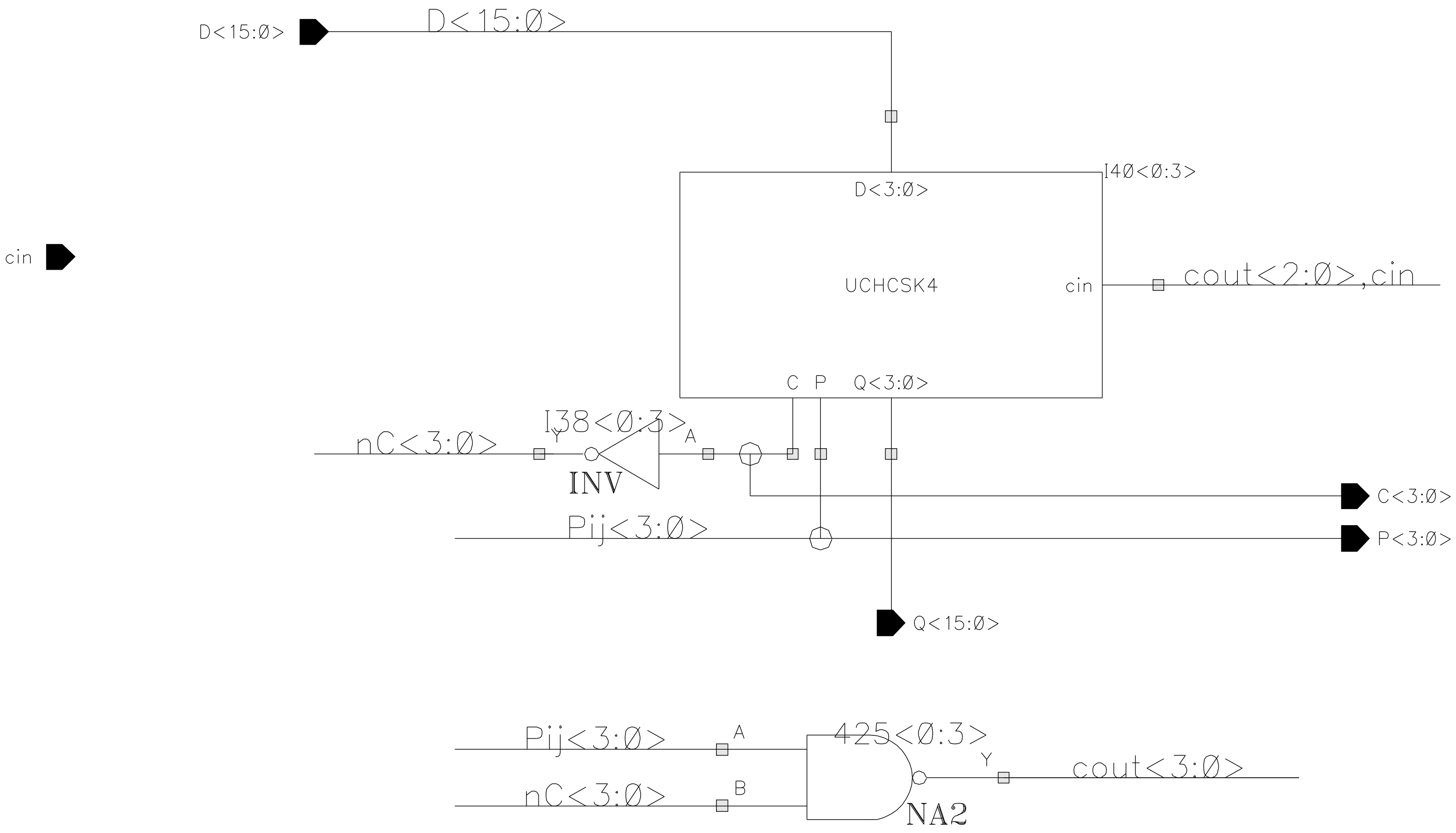

Fig. C.29: 16-bit Carry SKip Adder (CSKA) comprised from four 4-bit Carry Ripple Adders (CRA).

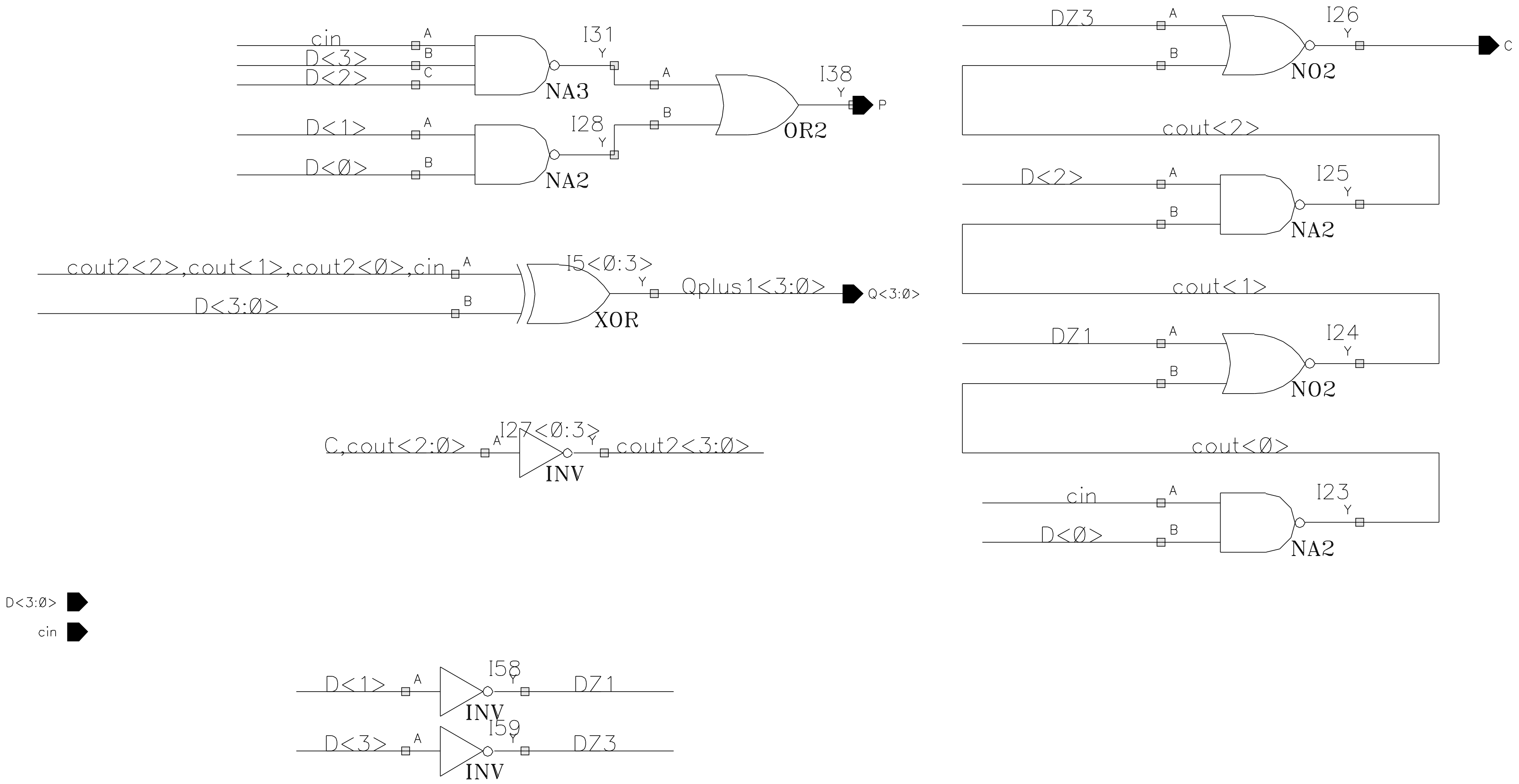

Fig. C.30: 4-bit Carry Ripple Adder used as building block in CSKA.

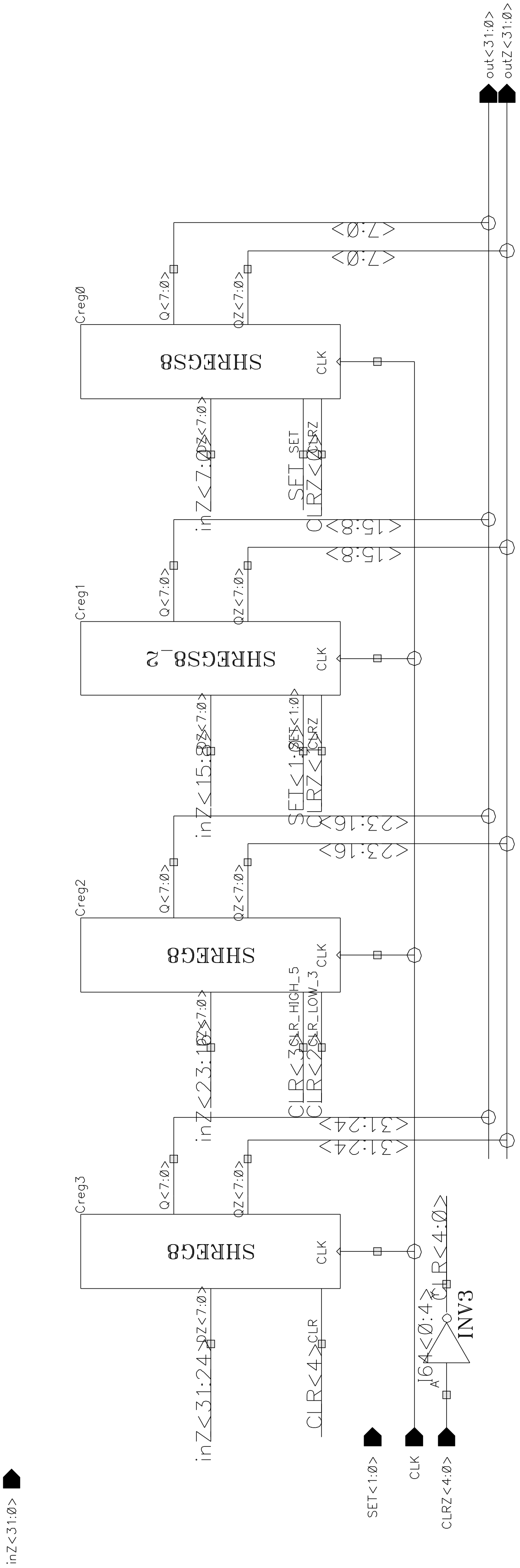

Fig. C.31: C register

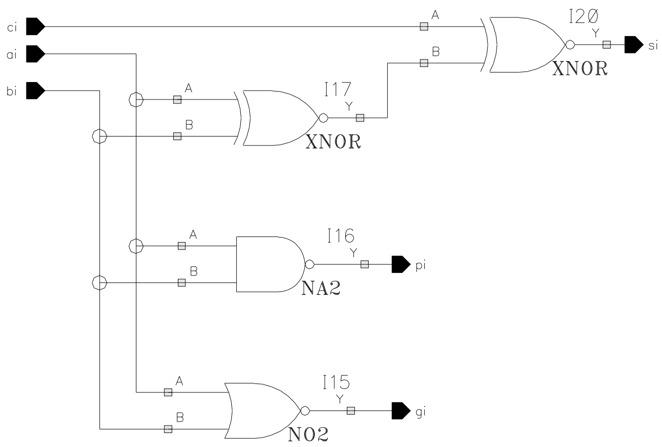

Fig. C.32: CLA A-type Adder cell.

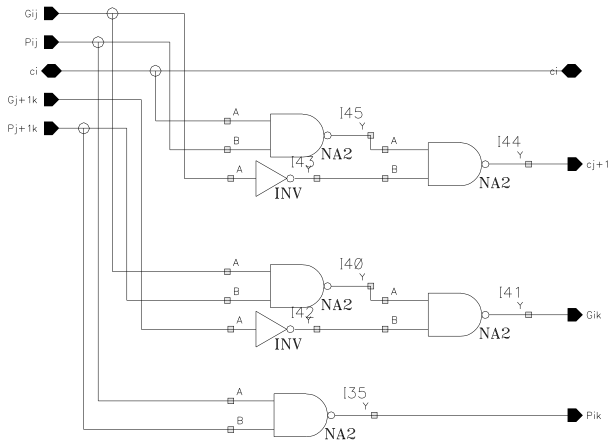

Fig. C.33: CLA B-type Adder cell.

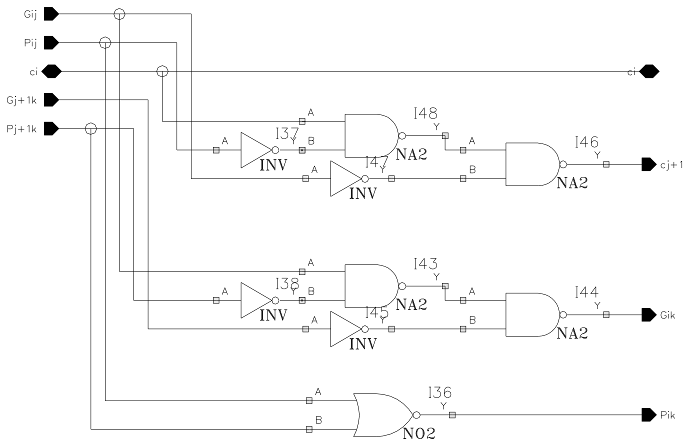

Fig. C.34: CLA alternative B-type Adder cell.

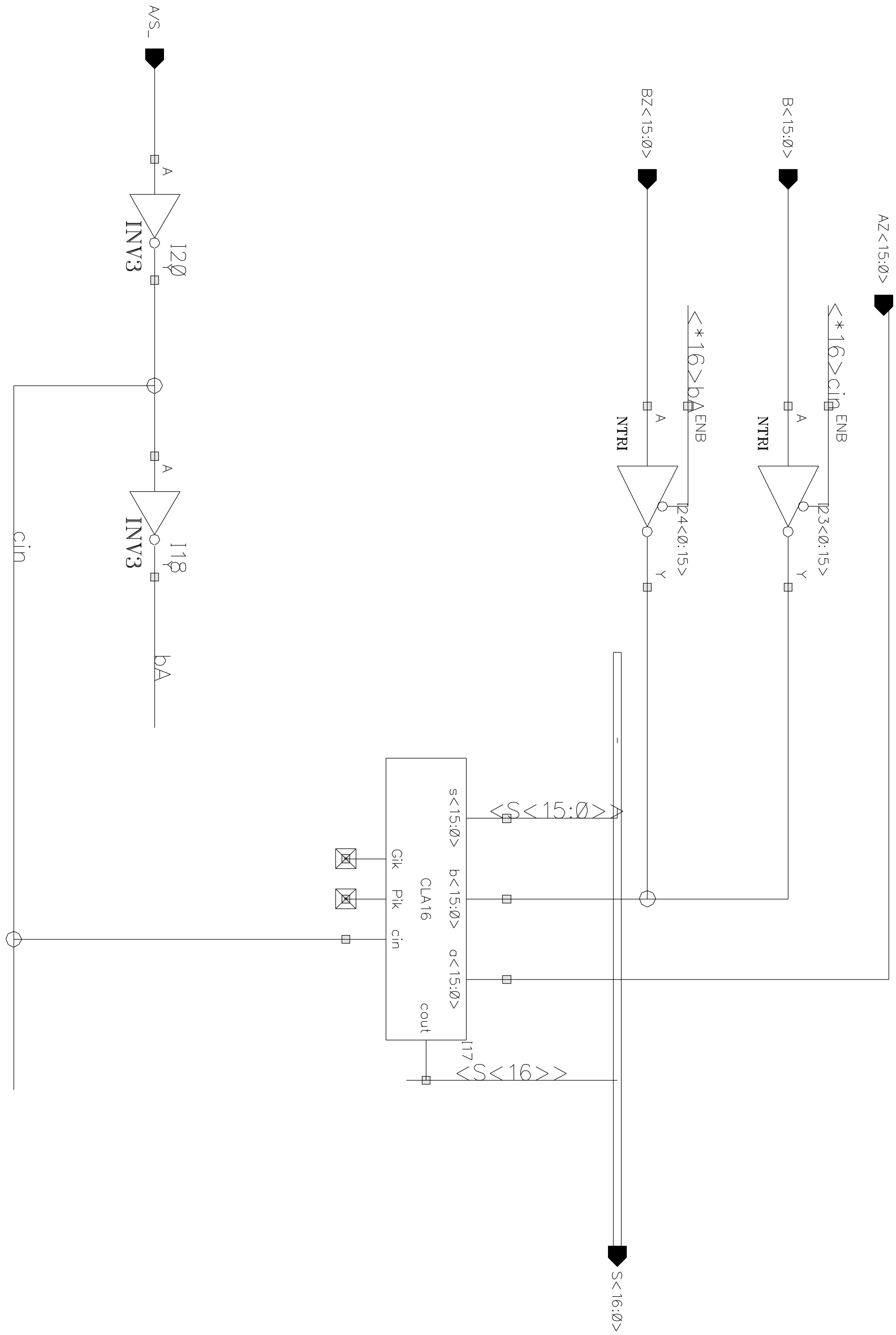

Fig. C.35: 16-bit CLA.

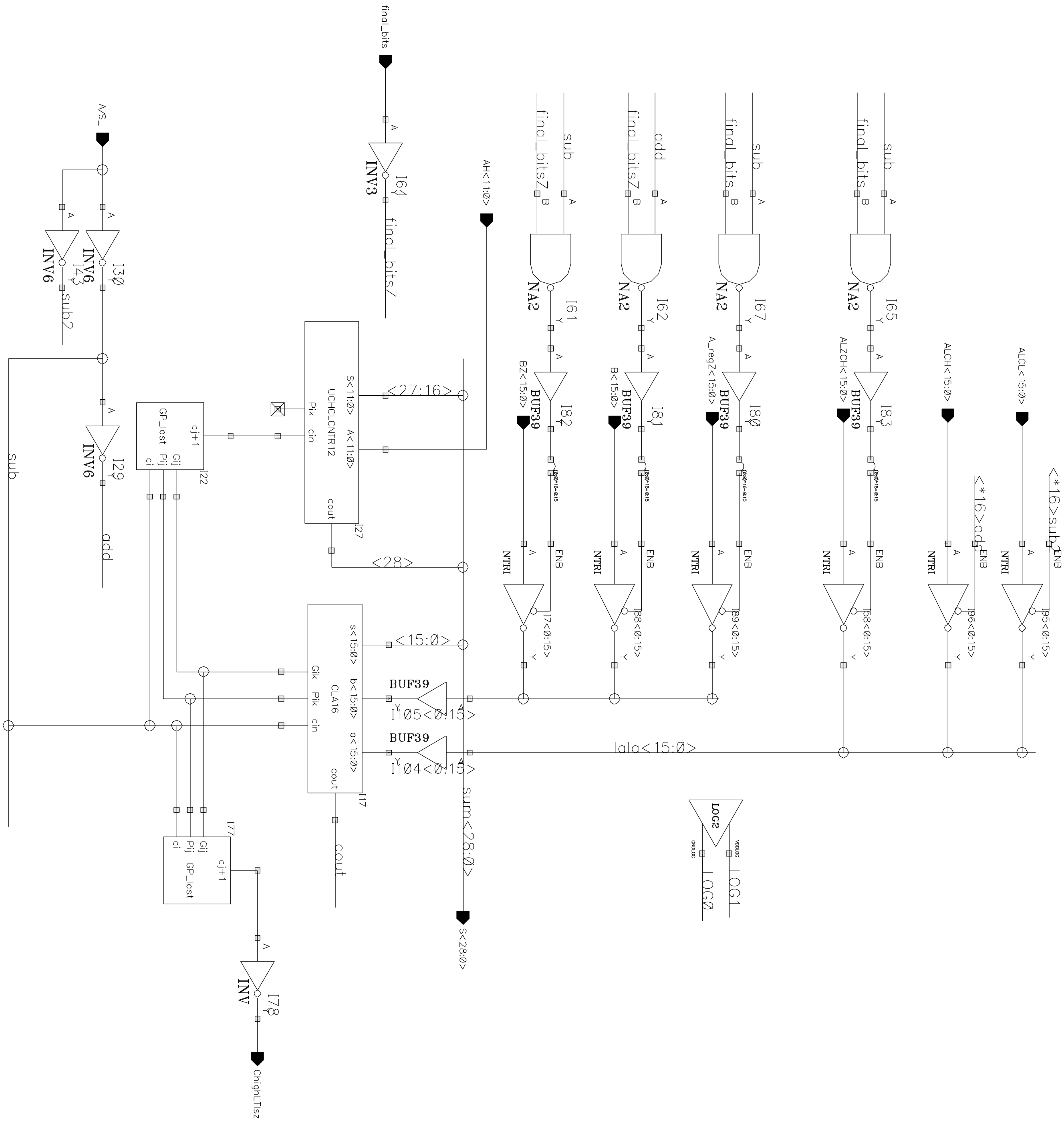

Fig. C.36: 28-bit CLA.